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Analysis and EOT Scaling on Top- and Double-Gate 2D CVD-Grown Monolayer MoS_2 FETs

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2D layered semiconductors have attracted considerable attention for beyond-Si complementary metal-oxide-semiconductor (CMOS) technologies. They can be prepared into ultrathin channel materials toward ultrascaled device architectures, including double-gate field-effect-transistors (DGFETs). This work presents an experimental analysis of DGFETs constructed from chemical vapor deposition (CVD)-grown monolayer (1L) molybdenum disulfide (MoS_2) with atomic layer deposition (ALD) of hafnium oxide (HfO_2) high-k gate dielectrics (top and bottom). This extends beyond previous studies of DGFETs based mostly on exfoliated (few-nm thick) MoS_2 flakes, and advances toward large-area wafer-scale processing. Here, significant improvements in performance are obtained with DGFETs (i.e., improvements in ON/OFF ratio, ON-state current, sub-threshold swing, etc.) compared to single top-gate FETs. In addition to multi-gate device architectures (e.g., DGFETs), the scaling of the equivalent oxide thickness (EOT) is crucial toward improved electrostatics required for next-generation transistors. However, the impact of EOT scaling on the characteristics of CVD-grown MoS_2 DGFETs remains largely unexplored. Thus, this work studies the impact of EOT scaling on subthreshold swing (SS) and gate hysteresis using current–voltage (*I–V*) measurements with varying sweep rates. The experimental analysis and results elucidate the basic mechanisms responsible for improvements in CVD-grown 1L-MoS_2 DGFETs compared to standard top-gate FETs.

1. Introduction

Following the discovery of graphene in 2004.[1] 2D semiconductors quickly gained interest toward electronic device technologies. Significant efforts have surged recently emphasizing the use of 2D semiconductors as the channel material in ultrascaled field-effect-transistors (FETs) to enable scaling beyond the limits of bulk semiconductors (i.e., silicon).[2–10] Transition metal dichalcogenides (TMDs) have been widely studied for beyond-Si FETs and CMOS technologies. While early studies focused on back-gated FETs constructed from individual flakes of MoS_2 exfoliated from bulk crystals (heavily doped silicon acting as global back gate),[11,12] new efforts must push toward the use of large-area CVD-grown materials and advanced multi-gate device architectures such as double-gate FETs,[13–15] FinFETs,[16] and gate-all-around (GAA) FETs.[17] Indeed, recent efforts have started to explore FETs using CVD-grown 1L-MoS_2, including individually back-gated, top-gated, and double-gate architectures. For example, recent work from Intel and other[3,17–22] has suggested that 2D TMDs offer a unique opportunity for scaling transistor gate lengths below 10 nm to support the continuation of Moore's Law. In fact, commonly cited semiconductor technology roadmaps such as the IEEE International roadmap for devices and systems (IRDS)[23] proposes the complete replacement of silicon by 2D semiconductors as the channel material by the "0.7 nm" node and beyond (2034 and beyond). It should be noted that in these advanced nodes the choice of insulating materials in the gate stack is equally important and stringent requirements are needed to ensure performance and reliability.[24] First, a scalable device technology requires a small equivalent oxide thickness (EOT) to support good gate control of channel electrostatics in short channel dimensions. At the same time, gate leakage (i.e., current flow across the gate insulator) should be kept at a minimum to maintain low power consumption, and traps (in the oxide and at the semiconductor/oxide interface) should be minimized to achieve good stability and reliability.[10] For modern FETs using 2D semiconducting channels, identifying suitable insulating materials remains a significant challenge and it is crucial to examine existing solutions based on their impact on performance and stability in advanced device architectures.[24] A few previous works have reported subthreshold swing and other performance metrics in double- and top-gate FETs, and recent efforts have studied

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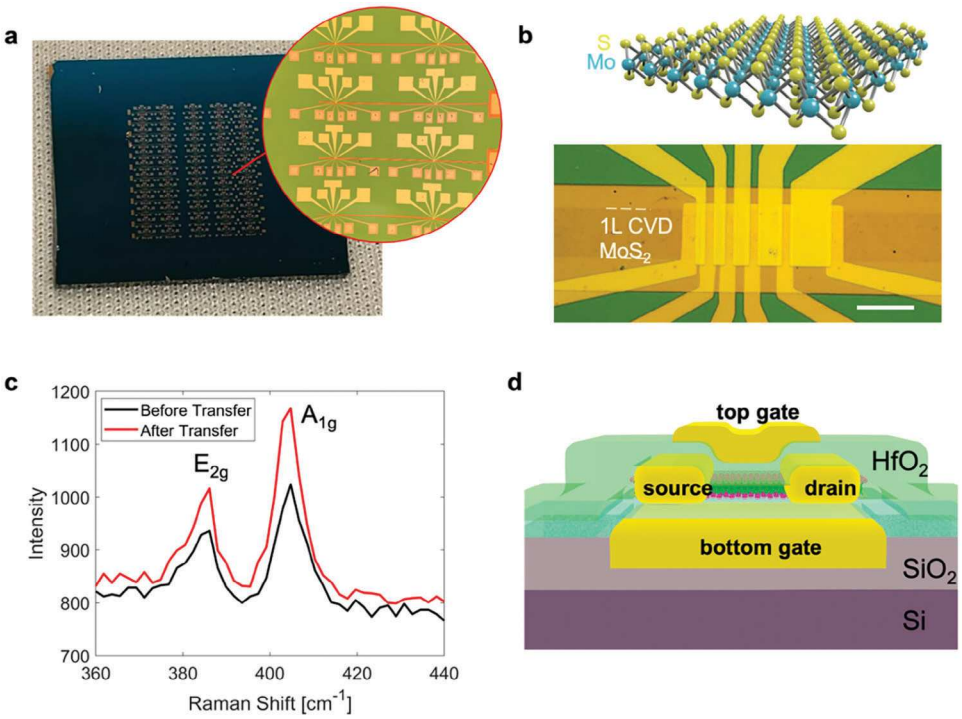

Figure 1. a) Optical image and micrograph of fully-fabricated double-gate monolayer MoS_2 field FETs in TLM test-structure configuration. b) Micrograph of the MoS_2 FET TLM structure with five different channel lengths ranging from 360 to 7000 nm, with back-gate extending entirely under the channel region, and top gates having minimal overlap over source/drain. c) Raman spectra of CVD-grown 1L-MoS_2 consistent before and after wet-transfer process. d) 3D cross-section schematic of the double-gated MoS_2 FETs.

gate hysteresis and stability in devices using advanced seeding methods for ALD of high-k gate oxides on MoS_2 devices[25] Nonetheless, the effect of EOT scaling on CVD-grown 1L-MoS_2 FETs comparing double-gate and single top-gate remains largely unexplored and is addressed in this work.

In this work, we present an experimental analysis on the performance of double-gate and top-gate FETs fabricated from CVD-grown monolayer (1L) molybdenum disulfide (MoS_2) with atomic-layer deposition (ALD) of hafnium oxide (HfO_2) high-k gate dielectrics (top and bottom). The analysis compares contact resistance and mobility between double-gate and top-gate device architectures based on extractions from transfer length method (TLM) test structures (i.e., FETs with various channel lengths but consistent contact and gating configurations),[8,14,26,27] as well as subthreshold swing and gate hysteresis. Importantly, the analysis of subthreshold swing and gate hysteresis is presented as a function of EOT to establish improvements in performance and stability as EOT is reduced to ≈ 1 nm as dictated by the semiconductor roadmaps for advanced CMOS nodes. We also note that in our electrical characterization of double-gate FETs, both top and bottom gates are biased in common mode configuration (i.e., held at the same voltage). However, to elucidate the effect of the back-gate biasing on device performance we also present data analysis from measurements in independent mode where top and bottom gates are individually biased at different voltages. Here, a reversal in the temperature-dependence of on-state current as a function of increasing back-gate bias indicates an improvement in contact-resistance and device performance in double-gate FETs resulting from electrostatic doping/modulation of Schottky junctions in the contact regions. Our measurements also reveal non-uniform gate hysteresis as a function of independent top- and bottom-gate bias, which may be crucial to characterizing and understanding charge trapping phenomena associated with gate hysteresis and to achieving stable and reliable operation of future MoS_2 FET technology.[28–30] Lastly, we analyze gate hysteresis using various voltage sweep rates on top-gate devices with two different oxide thicknesses to identify the impact of EOT scaling on device stability.

2. Results and Discussion

Figure 1a shows an optical image and micrograph of the fully-fabricated wafer that includes arrays of double-gate and top-gate CVD-grown 1L-MoS_2 FETs in a TLM test structure configuration. A description of the fabrication methods is given in the Experimental Section with more detailed schematics of the processing steps provided in the Supporting Information. A higher magnification image in the active channel region of an individual double-gate TLM structure is shown in Figure 1b with the atomistic model depicting the monolayer MoS_2 channel. In our fabrication process, a CVD-grown monolayer of MoS_2 is transferred from the growth substrate onto a Si/SiO_2 wafer prepared with the bottom gate stack (Figure S1, Supporting Information). To ensure the quality of the channel material we conduct Raman spectroscopy before and after transfer. Figure 1c shows the Raman spectra before and after transfer and confirms negligible degradation to the 1L-MoS_2 film during transfer. Figure 1d presents a 3D schematic diagram of the fully-fabricated double-gate CVD-grown 1L-MoS_2

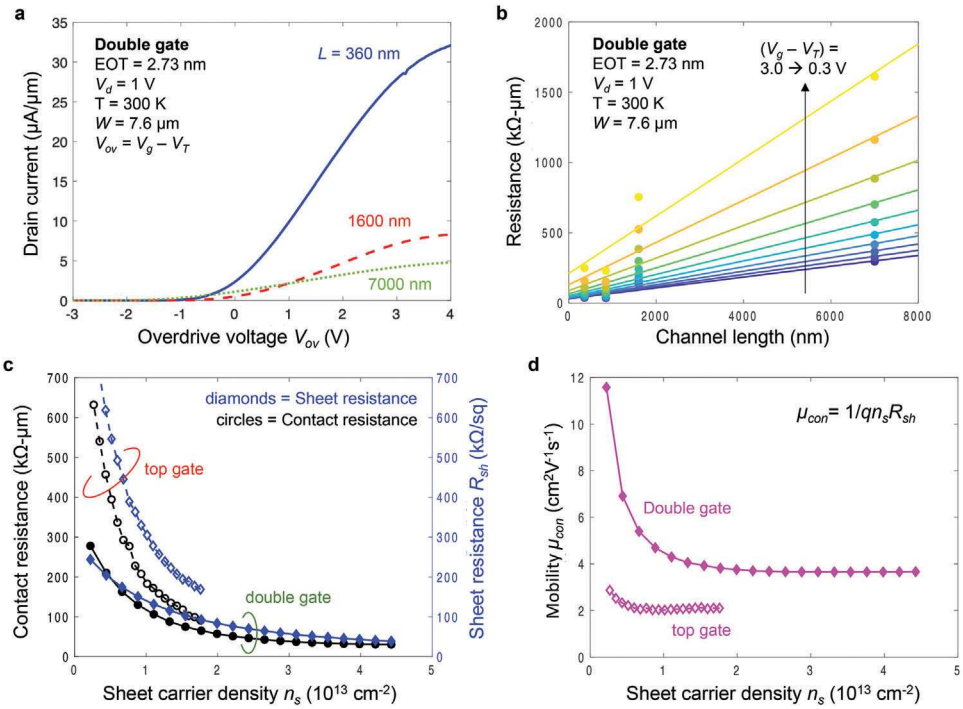

Figure 2. a) Drain current as a function of gate overdrive voltage $V_{ov} = (V_g - V_T)$ for double-gate MoS_2 FETs with three channel lengths (360, 1600, 7000 nm). b) Total resistance as a function of channel lengths with linear fits to experimental data at various V_{ov}. c) Extracted values for contact resistance (left y-axis) and channel sheet resistance (right y-axis) plotted as a function of sheet-carrier density (estimated from V_{ov}). The plot compares extractions from top-gate and double-gate MoS_2 FETs. d) Extractions of mobility as a function of sheet carrier density for top-gate and double-gate MoS_2 FETs.

FET. In this work, we also refer to single top-gate FETs which were fabricated with an identical process except without the bottom gate stack. Schematic diagrams for the top-gate FETs, compared against the double-gate devices, are provided in the Supporting Information (Figure S3, Supporting Information).

The performance of double-gate and top-gate FETs are first compared based on extractions of contact resistance and mobility using the transfer length method.[26] Here, both the double-gate and top-gate FETs have the same bi-layer top-gate stack with EOT = 2.73 nm (1 nm Al_2O_3/10 nm HfO_2), and double-gate FETs have an additional bottom-gate stack with a 10 nm HfO_2 gate dielectric. We measure drain-current (I_d) as a function of gate voltage (V_g) for devices with various channel lengths ranging from L = 7000 nm down to 360 nm. The channel width W = 7.6 µm is the same for all devices. **Figure 2a** plots the current–voltage (I–V) characteristics where drain current is normalized to channel width (units of µA µm^{-1}). The x-axis plots the overdrive voltage $V_{ov} = (V_g - V_T)$, which is used to ensure the same on-state conditions in our extractions from all device measurements. Thus, for different L we can extract and plot total resistance $R = V_d/I_d$ at various V_{ov} as shown in Figure 2b (each line corresponds to different V_{ov} ranging from 0.3 to 3 V). Contact resistance (R_c) and sheet resistance (R_{sh}) are respectively extracted from the extrapolated y-axis intercept and slope of a linear fit to the data points for each V_{ov}. Next, by estimating sheet carrier density as $n_s = C_{ins}V_{ov}/q$, where $C_{ins} = \epsilon_{ins}/t_{ins}$ is the oxide/insulator capacitance per unit area above threshold, we plot R_c and R_{sh} as a function of n_s as shown in Figure 2c. While Figure 2a,b only show measurements from double-gated FETs (for clarity), Figure 2c shows extractions for both double-gate (solid lines with symbols) compared against top-gate (dashed-lines with symbols). The data shows that double-gate FETs achieve better contact resistance compared to top-gated FETs, reaching values as low as ≈30 kΩ-µm. These values are not optimal (IRDS specifies 220 Ω-µm for the 0.7 nm node), but they are comparable to other reported CVD-grown 1L-MoS_2 FETs, and there is room for improvement based on advanced contact engineering strategies.[8,27,31,32] From sheet resistance we can obtain the mobility as $\mu_{con} = (qn_sR_{sh})^{-1}$ which is plotted as a function of n_s in Figure 2d. The extracted μ_{con} are smaller compared to theoretical values and to values reported on exfoliated samples (better crystallinity), but similar to previous reports on CVD-grown 1L-MoS_2 samples.[33] Nonetheless, these values can be improved with optimized growth recipes and/or using transfer-free methods.[34] We also demonstrate improvements on charge transport properties and device performance in double-gate FETs compared to top-gate FETs. This is discussed below based on temperature-dependent measurements of on-state current at different top- and bottom-gate biasing (see Figure 4). Overall, the CVD-grown 1L-MoS_2 double-gate FETs perform better than top-gated FETs in terms of contact and sheet resistance, mobility, and on-state current; This is attributed to the effect of bottom-gate bias on the Schottky junctions at the source/drain contact regions.

To further elucidate the effect of the bottom-gate biasing on device performance we also analyze data from measurements in independent mode where top and bottom gates are individually biased at different voltages. These measurements were conducted over a wide temperature range to provide a better understanding

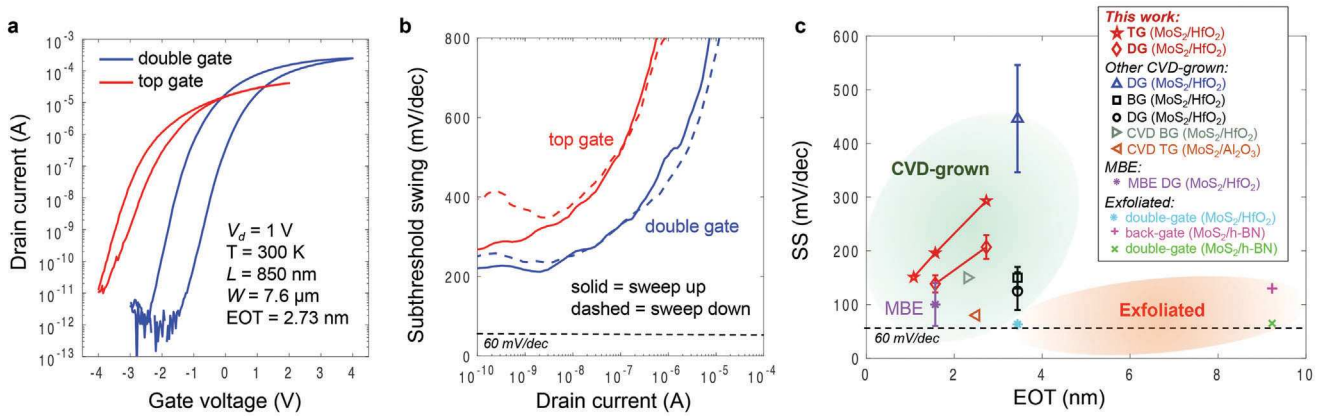

Figure 4. a) Dual-sweep drain current vs gate voltage characteristics comparing top-gate and double-gate MoS_2 FETs. b) Subthreshold swing vs drain current for both the top-gate and double-gate MoS_2 FETs. c) EOT scaling plot of subthreshold swing (SS) benchmarking our results (both top-gate and double-gate MoS_2 FETs) against previous reports on CVD-grown,[15,40–42] MBE[13] and exfoliated samples.[40,43] EOT scaling and double-gate architecture achieves improvements in SS. Each symbol/color combination indicates a different device measurement. DG = double gate, BG = bottom gate only, TG = top gate only.

of charge injection and charge transport in the double-gate FETs under the effect of independent bottom and top-gate bias.[35–37] **Figure 3a** plots drain-to-source current (I_{ds}) as a function of top-gate voltage ($V_{g,top}$) at different fixed bottom-gate voltages ($V_{g,bot}$) ranging from −3 to 3 V in steps of 0.6 V, and at a temperature of 300 K. Similarly, Figure 3b plots I_{ds} versus $V_{g,top}$ at fixed $V_{g,bot}$ and at a temperature of 77 K. For each combination of temperature and $V_{g,bot}$ we extract on-state current (I_{on}) at a fixed top-gate overdrive voltage $V_{ov,top} = V_{g,top} - V_T = 1.6$ V. The on-state current is plotted in Figure 3c as a function of temperature and for different $V_{g,bot}$. We observe a reversal in the temperature-dependence of I_{on} as $V_{g,bot}$ is increased from −3 V up to 3 V. For $V_{g,bot} = -3$ V the on-state current increases with increasing temperature, whereas for $V_{g,bot} = 3$ V the on-state current decreases with increasing temperature. This is indicative of a transition in the dominant/limiting charge injection and transport mechanism in the double-gate FET with increasing bottom-gate bias. We note that the bottom-gate extends under the source/drain regions (see Figure 1), therefore $V_{g,bot}$ can modulate the MoS_2 energy bands (through electrostatic doping) and consequently the Schottky barriers formed at the contacts. For negative $V_{g,bot}$, large energy barriers exist at the Schottky junctions between source/drain contacts and the MoS_2 channel and these are further enhanced by the electrostatic doping resulting from $V_{g,bot}$. Thus, the injection of charge carriers, in this case electrons into the conduction band, is limited by thermionic emission over the barrier and increasing temperatures leads to more charge carrier injection and therefore more on-state current as evidenced by the experimental results of I_{on}. On the other hand, for large positive $V_{g,bot}$ the electrostatic doping effect results in narrower energy barriers at the Schottky contacts, lessening the limitation of thermionic emission as more electrons can tunnel through these barriers into the conduction band. As a result we obtain larger I_{on}. This also results in the aforementioned reversal in the temperature dependence on I_{on}. Now, the dominant mechanism limiting charge flow is scattering in the channel region which generally intensifies with increasing temperature (e.g., more phonon scattering) translating to a reduction in I_{on} with temperature. Overall, the electrostatic doping effect of $V_{g,bot}$ improves device performance in double-gate FETs compared to single top-gate devices, in addition to other more well-known improvements related to better gate control of the channel electrostatics.

Within the same set of experiments on double-gate FETs with independent top and bottom-gate bias we characterize gate hysteresis using dual-sweep (sweep up and down) measurements of $V_{g,top}$ at fixed bottom gate voltages. These are plotted in Figure 3d (room temperature), where we show the current on a logarithmic scale to better observe hysteresis and the subthreshold region. For clarity, we only show the data for three different values of $V_{g,bot}$, and a plot of the full range of biases is provided in the Supporting Information (Figure S2, Supporting Information). Interestingly, for a fixed $V_{g,top}$ or corresponding I_{ds}, the bottom-gate bias has a significant impact on the magnitude of gate hysteresis. Similar effects were reported previously on graphene FETs[38] based on carrier-defect energy decoupling.[39] Here we define gate hysteresis as the shift in $V_{g,top}$ during sweep down versus sweep up to achieve the same value of I_{ds}. When extracted for all different values of $V_{g,top}$ and over a large range of I_{ds}, regions of large and small hysteresis are identified as illustrated by the contour plot shown in Figure 3e. We note that this observation of bottom-gate bias dependence may be crucial to better understand charge trapping phenomena associated with gate hysteresis and to achieve stable and reliable operation of future MoS_2 FET technology.[38]

A closer look at the I_d versus V_g characteristics provides more evidence of improvements in double-gate FETs compared to single top-gate FETs, as shown in **Figure 4a**. The double-gate FET shows larger on-state current, larger ON/OFF ratio, and better (smaller) subthreshold swing. We note that both devices in this comparison have the exact same top gate stack with EOT = 2.73 nm. The double-gate FETs show larger hysteresis as a result of having two dielectric layers (top and bottom) that can contribute to charge trapping effects (in contrast, single top-gate FET only has one gate dielectric on top). Nonetheless, a key advantage of a double-gate architecture is the improvement in gate control of the channel electrostatics and can be quantified by the

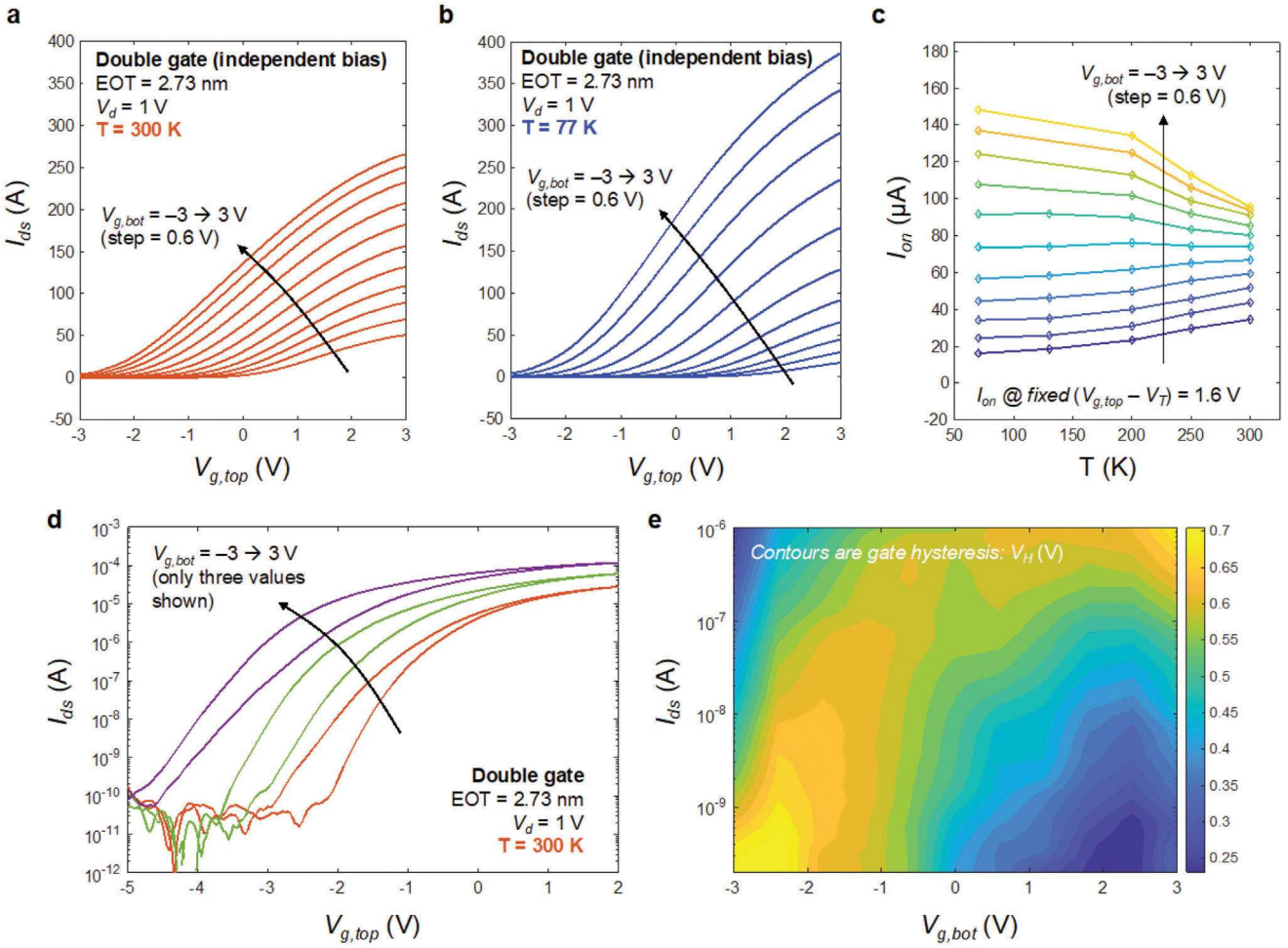

Figure 3. a) Drain-to-source current (I_{ds}) vs top-gate voltage ($V_{g,top}$) at various fixed bottom-gate voltages ($V_{g,bot}$) stepped from –3 to 3 V in steps of 0.6 V measured at room temperature (300 K). **(b)** I_{ds} vs $V_{g,top}$ at various fixed $V_{g,bot}$ measured at 77 K. c) Extractions of on-state current (I_{on}) at fixed overdrive voltage as a function of temperature for various $V_{g,bot}$. Increasing $V_{g,bot}$ improves I_{on} and also results in a reversal of the temperature-dependence of I_{on}. d) Log-scale plot of I_{ds} vs $V_{g,top}$ at room temperature including dual gate-sweep data showing gate hysteresis (for simplicity only three values of $V_{g,bot}$ are shown). e) Contour plot of gate hysteresis (V_H) extracted as a function of $V_{g,bot}$ and I_{ds}.

subthreshold swing (SS). In Figure 4b we plot SS as a function of drain current for sweep-up and sweep-down comparing double-gate and top-gate FETs. The double-gate FET results in better (smaller) SS over the full range of I_d which extends more than 5 orders of magnitude in the subthreshold region. For EOT = 2.73 nm we achieve a minimum SS of ≈300 mV dec^{-1} in the top-gate FET and ≈200 mV dec^{-1} in the double-gate FET (1.5× improvement). These numbers are larger than the ideal 60 mV dec– at room temperature (300 K), but are comparable to other reports on CVD-grown 1L-MoS_2 FETs with ALD gate dielectrics. Additional plots of I_d-V_g and SS-I_d characteristics are shown for devices with varying EOT in the supporting information (Figure S4, Supporting Information).

For benchmarking purposes, Figure 4c compares our results in top-gate and double-gate FETs against previous reports including CVD,[15,40–42] molecular beam epitaxy (MBE)[13] and mechanically exfoliated MoS_2,[40,43] in double-gate, top-gate, and back-gate FETs. Moreover, the results are shown as a function of EOT to establish the impact of EOT scaling on performance. EOT scaling potentially leads to improved gate control, reduction of short channel effect, improved threshold voltage control, enhanced carrier transport, and suppression of charge-trapping effects and associated phenomena. Ultimately, EOT scaling can help make the most of 2D channel materials toward ultra-scaling of MOSFET technology. Our double-gate FETs with EOT scaling down to ≈1.5 nm and top-gate FETs with EOT scaling down to ≈1 nm show significant improvements in SS down to ≈ 120 mV dec^{-1}. We emphasize that this is one of the best subthreshold swing performances reported on 1L-MoS_2 FETs, other than in MBE and exfoliated samples. The fact that MBE and mechanical exfoliation can achieve reduced defect density suggests that the quality/crystallinity of the channel plays a significant role in subthreshold swing performance together with the gate dielectric and interface quality. Nonetheless, mechanical exfoliation is not a scalable process (can only achieve small isolated flakes) and MBE is more costly, difficult to scale to large wafer-size, and incompatible with direct growth on amorphous substrates.[44] We also include results from FETs fabricated on CVD-grown monolayer

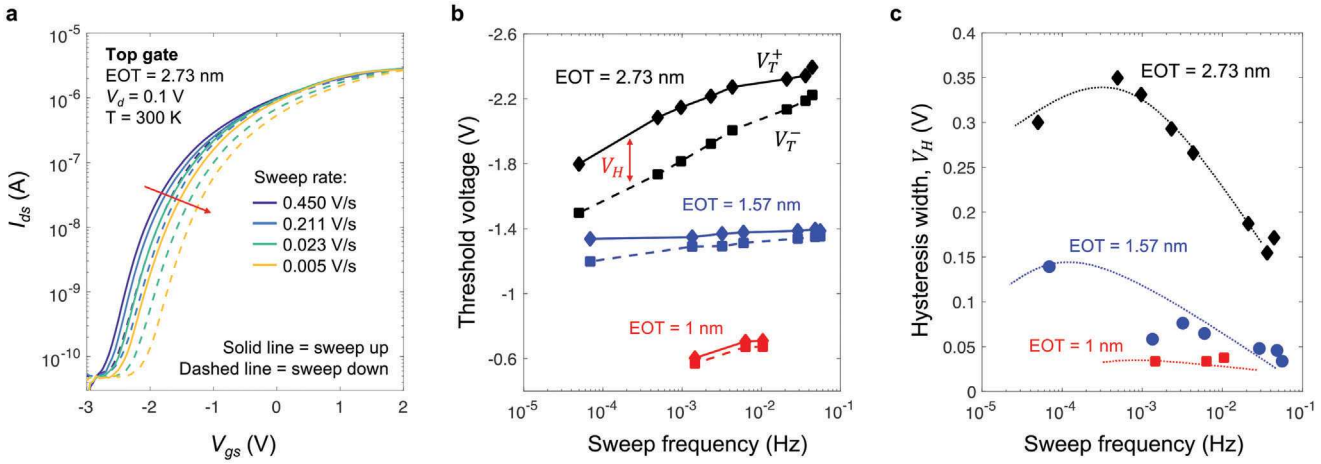

Figure 5. a) Drain-to-source current (I_{ds}) vs gate-to-source voltage (V_{gs}) for top-gate MoS_2 FET (EOT = 2.73 nm) measured at room temperature using various sweep-rates. b) Extractions of threshold voltage (from both positive and negative sweep characteristics, that is, V_T^+ and V_T^-) plotted as a function of sweep frequency for top-gate MoS_2 FETs with EOT = 2.73, 1.57, and 1 nm. c) Gate hysteresis width $V_H = V_T^- - V_T^+$ plotted as a function of sweep frequency for EOT = 2.73, 1.57, and 1 nm. Dotted lines are guides, and do not represent any specific fitting to the data.

MoS_2 directly on SiO_2 (i.e., no transfer)[42] showing improvement in SS (≈80 mV dec^{-1}), but limited to high-temperature processing.

Also included in this plot are bottom- and double-gate FETs prepared by mechanical exfoliation of MoS_2 and mechanical exfoliation (and stacking) of hexagonal boron nitride (h-BN) as the gate dielectric.[43] As a crystalline insulator, h-BN has the potential to provide well-defined van der Waals (vdW) interfaces with 2D semiconductors.[24] In this regard, previous work has reported interface trap densities (D_{it}) as low as ≈10^9 $cm^{-2}eV^{-1}$ in h-BN/MoS_2.[45] This can result in nearly ideal SS as well as significant enhancement of channel mobility resulting from the suppression of trap-induced charged-impurity scattering effects. Nonetheless, limitations in bandgap and dielectric properties can impact EOT scalability for h-BN and high leakage is expected for small EOT≈1 nm.[46] As a result, most previous demonstrations are based on thick exfoliated h-BN samples (EOT > 8 in Figure 4c). Thus, h-BN is considered a promising insulator for 2D-material-based devices that do not require extreme scaling. Nevertheless, mechanical exfoliation is not considered a scalable process and large-area CVD-grown h-BN requires further optimization to achieve comparable defect densities. Interestingly, the existence of native defects in CVD-grown h-BN films has led to significant efforts toward h-BN resistive-switching memory based on recoverable soft breakdown phenomena.[47,48]

As noted for the *I–V* characteristics in both double-gate and top-gate MoS_2 FETs (Figures 3d, 4a) measured using dual voltage sweeps (i.e., sweep up and sweep down), charge-trapping effects are evident as gate hysteresis (i.e., voltage shift in the sweep up vs sweep down measurements). Careful examination of charge trapping effects is crucial to understand the long-term reliability/stability and performance of 2D MoS_2 FETs. Previous work on MoS_2 FETs has used measurements of gate hysteresis in their I_d-V_g characteristics to map out the oxide traps with widely distributed time constants.[29,30] By varying the voltage sweep range as well as the sweep rate, extractions of gate hysteresis were used to obtain the density and energy distribution of oxide traps and to explain the hysteresis dynamics in relation to positive and negative bias-temperature instability (PBTI, NBTI). However, the impact of EOT scaling on gate hysteresis in CVD-grown 1L MoS_2 FETs remains largely unexplored. Nonetheless, it is anticipated that by reducing the physical thickness of the gate oxide (i.e., reducing EOT), the oxide capacitance increases, and the effect of trapped charge is lowered ($\Delta V \approx \Delta Q/C_{ox}$), so gate hysteresis will be smaller. To examine the EOT-dependence of gate hysteresis we have conducted a series of I_d-V_g dual sweeps with varying sweep rates on top-gated MoS_2 FETs with three different EOT. This allows to observe the effect of oxide traps with different time constants and provide a more conclusive comparison between devices of different EOT.

In **Figure 5a** we plot the I_d-V_g characteristics of top-gated MoS_2 FETs with EOT = 2.73 nm measured using dual voltage sweeps with varying sweep rates ranging from 0.45 to 0.005 V s^{-1}. Here, sweep rate is defined as V_{step}/t_{step} where V_{step} is the voltage step in the sweep and t_{step} is the time step. We note that gate hysteresis is smaller in these devices compared to earlier work using significantly larger EOT ≈ 10 nm (23.5 nm Al_2O_3).[29] In this work, the top-gate stack includes a 1 nm oxidized Al seeding layer and 10 nm HfO_2 dielectric layer (EOT = 2.73 nm) prepared by ALD. Other EOT (1.57 and 1 nm) are achieved with thinner HfO_2 (5 and 3 nm). The results in Figure 5a show that reducing the sweep rate (slower sweep) results in larger hysteresis, but also in an slight shift to more positive voltages for both sweep-up and sweep-down measurements. This positive shift is consistent with positive-bias-temperature instability (PBTI) attributed to charge build-up contributed by slow electron traps that become negatively charged (electron capture) for positive gate bias[29] A more quantitative analysis is obtained by extracting threshold voltage from sweep up (V_T^+) and from sweep down (V_T^-) measurements. The extractions of threshold voltage are plotted in Figure 5b as a function of sweep frequency defined as $f = 1/t_{sweep}$ where t_{sweep} is the total sweep time. The plot shows threshold voltage extractions for EOT = 2.73, 1.57, and 1 nm. From the extracted threshold voltages, the gate hysteresis width is calculated as

$V_H = V_T^- - V_T^+$. Figure 5c plots hysteresis width as a function of sweep frequency for all three different EOTs. The main observations are 1) gate hysteresis increases with reducing sweep frequency as more traps with slower time constants can contribute to charge trapping; 2) gate hysteresis peaks and then drops below a certain frequency ($f \approx 10^{-3}$ Hz) consistent with previous observations and models[49] This is evident for EOT = 2.73 nm, but further investigation is needed to confirm a peak in gate hysteresis for smaller EOT; 3) gate hysteresis is smaller for smaller EOT (appears to be directly proportional to EOT). These results provide initial insights to the impact of EOT scaling on gate hysteresis in CVD-grown 1L-MoS2 FETs with high-k ALD oxides. The results indicate favorable trends in EOT scalability in relation to gate hysteresis. Nonetheless, further studies with larger samples of EOT should provide a more complete picture on the relationship between EOT and V_H. Moreover, in addition to gate hysteresis, other considerations toward EOT scaling are crucial to ensure device performance and reliable 2D FET operation, such as gate leakage. In our experiments, we did not detect significant gate leakage for EOT = 2.73 and 1.57 nm, but we measured a gate current density of $\approx 1.5 \times 10^{-2}$ A cm^{-2} for EOT = 1 nm. This level of gate current density is near the low-power limit of 10^{-2} A cm^{-2} and consistent with previous work on MoS_2/HfO_2.[24,46]

3. Conclusion

We report a comprehensive analysis of FETs constructed from CVD-grown 1L-MoS_2 with HfO_2 gate dielectrics. This study compares top-gate against double-gate FETs (DGFETs), extending beyond most previous studies that used exfoliated (few-nm thick) MoS_2 flakes, instead focusing on large-area wafer-scale methods. We measure significant improvements in performance for double-gate FETs (larger ON/OFF ratio, larger ON-state current, smaller sub-threshold swing) compared to single top-gate FETs. Moreover, we quantify the impact of EOT scaling, crucial toward improved electrostatics required for next-generation nanoscale transistors, on subthreshold swing and gate hysteresis. This was previously unexplored for CVD-grown 1L-MoS_2 FETs, especially in double-gate device architectures that can facilitate ultra-scaling for future CMOS technology nodes. We also provide new insight about performance improvement in DGFETs attributed to improved electrostatic gate control (lower subthreshold swing) and improved charge-injection across source/drain contacts and the channel (larger I_{on}). Finally, we experimentally demonstrate a reduction in gate hysteresis with reduced EOT indicating favorable scaling trends with respect to MoS_2/HfO_2 gate-stack stability.

4. Experimental Section

Device Fabrication: CVD-grown monolayer MoS_2 was purchased from 6Carbon Technology (Shenzhen) and was transferred to a Si/SiO_2 substrate using a conventional wet-transfer method. In the case of double-gate FETs, the Si/SiO_2 substrate was initially prepared with a bottom gate stack using standard lithography, deposition, and liftoff (gate electrode), and ALD (HfO_2 gate dielectric). After transferring the CVD-grown 1L-MoS_2, the channel region was patterned by dry etching, and source and drain contacts (5 nm Ti/25 nm Au) were fabricated using photolithography, deposition, and liftoff. Here, different channel lengths are prepared (used in TLM experiments) as determined by different distances between source and drain contacts (360, 850, 1600, 3200, and 7000 nm). Next, a seeding layer (1 nm Al_2O_3) was used to improve subsequent ALD film adhesion and uniformity. To prepare the seeding layer, <1 nm Al was deposited by e-beam evaporation at a rate of 0.1 A s^{-1} and was treated thermally to convert into Al_2O_3. Then, ALD deposition of HfO_2 (3, 5 nm, or 10 nm) was done at 180 °C to achieve conformal deposition. An additional lithography step is then used to prepare the top gate by e-beam evaporation and lift-off. Finally, the bottom gate and source-drain pad regions are made accessible using a masked dry-etching step to remove the various ALD high-k dielectric layers. More details about the fabrication and a process flow diagram is included in the Supporting Information (Figure S1, Supporting Information).

Electrical Measurements: Electrical measurements were conducted on a Lakeshore CRX-VF cryogenic probe station combined with a Keysight b1500a semiconductor parameter analyzer. Temperature controlled I-V measurements were performed using various source measure units (SMUs) connected at a vacuum of 10^{-6} torr with ZN50R-CVT probes (uninterrupted variable temperature probes). All measurements with varying sweep rates were conducted using a Keithley 4200 semiconductor characterization system (SCS) using SMUs programmed with fixed timing parameters.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D semiconductors, double-gate, field-effect-transistor, molybdenum disulfide, MoS_2

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