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A Study on h-BN Resistive Switching Temporal Response

*Mirembe Musisi-Nkambwe, Sahra Afshari, Jing Xie, Hailey Warner, and Ivan Sanchez Esqueda**

Previous work that studied hexagonal boron nitride (h-BN) memristor DC resistive-switching characteristics is extended to include an experimental understanding of their dynamic behavior upon programming or synaptic weight update. The focus is on the temporal resistive switching response to driving stimulus (programming voltage pulses) effecting conductance updates during training in neural network crossbar implementations. Test arrays are fabricated at the wafer level, enabled by the transfer of CVD-grown few-layer (8 layer) or multi-layer (18 layer) h-BN films. A comprehensive study of their temporal response under various conditions–voltage pulse amplitude, edge rate (pulse rise/fall times), and temperature–provides new insights into the resistive switching process toward optimized devices and improvements in their implementation of artificial neural networks. The h-BN memristors can achieve multi-state operation through ultrafast pulsed switching (< 25 ns) with high energy efficiency (≈10 pJ pulse^{-1}).

1. Introduction

In overcoming the von-Neumann bottleneck there is growing interest in exploring the use of emerging resistive switching (RS) devices for in situ matrix computations (i.e., in-memory computing) and research shows promising potential for high throughput and ultralow power consumption.[1] To compete with commercial grade memories, emerging memory technology would need to challenge the switching speeds of SRAM,[2] the storage densities of DRAM[3] and the non-volatility of FLASH[4] memory–all while providing superior scalability and ability to work at further confined core voltages. A prospective synaptic device would additionally need to exhibit distinct resistive states (and high ON/OFF ratio), low switching voltage with controllable potentiation and relaxation abilities, high retention times (>10 years), and high switching endurance (>10^6 low resistance state to high resistance state (LRS-HRS) and > 10^6 HRS-LRS).[5,6] Emerging memories such as resistive random access memory (RRAM) have shown potential to meet these challenges[7] even pushing into other market segments such as automotive and industrial environments.[8] The most common RRAM categories are transition metal oxide (TMO)-based RRAM and CBRAM (conductive bridging RAM).[9–11] The oxide-based switching mechanism is due to the field-driven formation of a conducting path by oxygen vacancies migrating in the oxide layer forming hopping sites for current conduction. Conversely, the CBRAM conduction path formed through a solid electrolyte switching layer is due to the oxidation and dissolution of active metal electrodes and subsequent migration of the corresponding metallic ions. An area of development and barrier to widespread adoption of these devices is variability commonly attributed to the stochastic nature of the resistive switching process.[12,13]

Further emerging in this space is 2D material-based RRAM (or 2D RRAM) with potentially lower variability[13] faster switching times, and reduced programming voltages.[14–16] In many cases, 2D RRAM additionally has the potential to outperform traditional RRAM devices with more competitive switching power and switching speeds.[17–19] These atomically thin devices even exhibit RS behavior at the monolayer (i.e., switching layer reduced to a single atomically-thin sheet)[20] that provides significant improvements toward vertical memory integration over the aforementioned oxide-based RRAM[21,22] or CBRAM. The need for additional electroforming steps to prime the dielectric is also reduced.[13,21] A significant amount of work has been dedicated toward investigating the direct current (DC) performance of 2D RRAM[13,21,23,24] based on electrical characterization of discrete devices with planar metal-2D material-metal structures. In most cases, the 2D material active layers are prepared by chemical vapor deposition (CVD). Here, insulator hexagonal-boron nitride (h-BN) has shown remarkable resistive switching behavior (both volatile[13] and non-volatile[25]) even down to the atomic limit (monolayer).[20] Other 2D materials including semiconducting transition metal dichalcogenides (TMDs)[26] and black-phosphorus [27,28]have been explored. Recent efforts have extended beyond single devices to demonstrate dot-product computation in 2D RRAM arrays, a computation ubiquitous in machine learning, and some have even demonstrated the implementation of linear and logistic regression.[29–32] New efforts[33]

M. Musisi-Nkambwe, S. Afshari, J. Xie, H. Warner, I. Sanchez Esqueda
School of Electrical
Computer and Energy Engineering
Arizona State University
Tempe, AZ 85281, USA
E-mail: isesqueda@asu.edu

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have shown the integration of 2D RRAM (h-BN memristors) with complementary metal oxide semiconductor field-effect transistors (CMOS-FET) in a one-transistor-one-memristor (1T1M) crossbar array configuration, with silicon-based transistors separately located in the front-end-of-line (FEOL). Other research have integrated FET and memristors by stacking 2D materials into the same device.[34] In most studies, however, electrical characterization is limited to DC current–voltage (*I*–*V*) sweep measurements or to measurements of resistance following the application of programming (setting/resetting) voltage pulses. There have been very few experimental studies on the transient response of device switching associated with the dynamic nature of filament formation and dissolution. Moreover, most of those studies only use a single pulse observation[18,21,22,35–37] as a determinant of switching speed and programming latency. For example, in,[18,21] by varying the width and amplitude, the switching time (set latency) (t_{set}) is deduced to be less than the applied pulse width if there is a clear resistance change from the resulting current measurement, rather than direct measurement of the t_{set} metrics. Other cases with direct measurement use a single pulse versus averaging over a series of pulses.[36,37] Also common to those studies are measurements of paired-pulse-facilitation/paired-pulse-depression (PPF/PPD)[4,17,18,22] for gradual set/reset in spiking neural networks or explorations into the level of volatility of the RS regime.[4,13] Some touch on the transition rate (dI/dt) of memristor current[5] as a peek into the transient behavior of the forming filament while others touch on the switching slope (dI/dV) illustrating how much applied voltage is needed to cause a fixed change in current.[22,38]

In this work, we demonstrate an array of few and multi-layer 2D h-BN memristors to study temporal behavior as the device transitions through resistive states. Of importance toward the realization of competitive tera operations per second (TOPS) metrics are more accurate update/programming speeds (low write latency), and access speed (low read latency). Here, extractions of programming speed are taken from the mid-point of the transition edge of the applied voltage pulse to that of the resulting memristor transient current signal for a more accurate set latency measurement and averaged over ten cycles. Energy consumption per state transition is then calculated from the experimental data as a time-integration over the transition period in contrast to typical methods[13,39] which use DC data. Using these methods, we explore the impact of the positive programming pulse amplitude (V_{set}) and edge rates (changing rise/fall times of these programming voltage pulses) as tuning parameters. With increased V_{set} a decrease in set latency is observed trending to under 40 ns for the applied V_{set} range. However, this results in comparatively increasing reset latencies and more variation in the reset phase. The associated switching energies also follow similar trends peaking up to 15× for reset energies compared to the set energies. Given the intent is for neuromorphic training applications this illustrates a focal point in prioritization of these metrics to the reset phase versus the current focus on set phase programming latencies. Significant energy savings can be observed by extrapolating the edge-rates beyond the experimental tool limit to obtain 10 pJ set switching energy for rise/fall times of 10 ns. The set latency similarly can be extrapolated beyond this limit to obtain set latencies under 30 ns. The experimental data also attempts to gain some insight into the RS switching mechanism across temperatures, first to prove the predominant ohmic nature of the filament based on the temperature dependence of LRS resistance. Second, and newly reported, the effect of temperature on switching characteristics.

2. Results and Discussion

2.1. Fabrication of h-BN Memristors

Few- and multi-layer h-BN memristors were prepared using CVD-grown films transferred from copper onto Si/SiO_2 substrates with pre-patterned bottom electrodes (5 nm Cr/35 nm Au). The h-BN film was then patterned into active regions and the electrodes (Ti/Au) were prepared by standard lithography, metal evaporation, and lift-off. Additional details on the fabrication are given in the Experimental Section. **Figure 1** presents different views of our memristor array test structures with the detail of the single device cross-section shown in Figure 1c. The test chip (Figure 1a) contains several arrays, and Figure 1b is a micrograph of a single 1 × 10 array of h-BN memristors. Cross-sectional transmission electron microscopy (TEM) images and Raman spectra identify the microstructure of the h-BN switching layer and are included in our previous work.[29–31] The experimental setup is shown in Supplementary Figure S1 (Supporting Information). Each array of devices shares a bottom electrode while the top electrodes are distinct Ti /Au stacks with memristor active area of 3 μm × 3 μm. The CVD-grown h-BN switching layer results in distinct resistive switching characteristics attributed to the formation of conductive nanofilaments localized to defect-rich grain boundaries.[13,36,40]

A typical device *I*–*V* characteristics are illustrated in **Figure 2** for the multi-layer h-BN ≈10 nm thick) memristor. Similar DC characteristics for the few-layer h-BN memristors were presented earlier.[30] Figure 2a plots the *I*–*V* behavior of Ti/h-BN/Au memristor over a few sample cycles indicating a clear transition between high and low resistance states (i.e., HRS and LRS). Using small read voltage sweeps the current is measured to generate *I*–*V* curves in the LRS (Figure 2b) and HRS (Figure 2c) across various temperatures (10–125 °C). Temperature variation provides a means to explore the characteristics of the filament as well as the electron conduction mechanism. The increase in resistance with increasing temperature in Figure 2b (LRS) is indicative of the metallic nature of the fully formed conducting Titanium (Ti) filament.[36] In Figure 2c (HRS) the decrease in resistance with increased temperature is typically attributed to bulk-limited current conduction mechanism–Trap Assisted Tunneling (TAT).[41] Both HRS and LRS plots are illustrated in Figure 2d showing the inverse relationship to temperature depending on the filament conductance state. This illustrates a difference in the physical nature of the filament supporting a more predominantly metallic filament in the LRS state.[21,29,38] Earlier work [30]presented further statistics for the few-layer version of the same (3 μm × 3 μm) device, the HRS, and LRS distributions as a function of the cycle number as well as the distribution of the set and reset voltages (≈+/−0.5 V). They indicate stable and reliable RS bipolar operations for the same compliant current. Retention is an important metric for non-volatile resistive switching (NVRS) devices, and previous work on similar h-BN memristors has

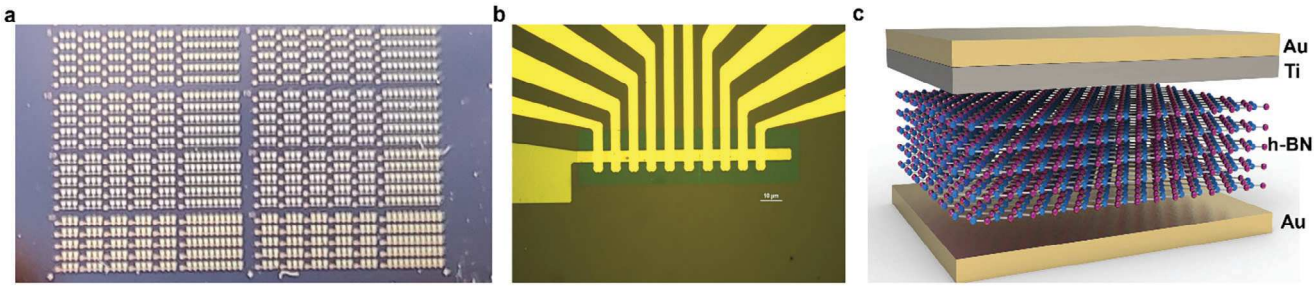

Figure 1. a) Picture of die showing h-BN memristor arrays (1 × 10 and 1 × 3 arrays) b) Micrograph of 2D h-BN memristor arrays (1 × 10) under test with ground connection to the bottom electrode (on the left) and individual device top electrode connections on the top. c) Cross-sectional schematic of the h-BN memristor arrays with Ti/Au top electrode and Au bottom electrodes fabricated onto a Si/SiO_2 wafer.

established strong retention over many devices for LRS and HRS of $> 10^4$ s.[29]

2.2. Transient Response

In recent years there has been a developing understanding of resistive switching in 2D h-BN with growing consensus toward two mechanisms,[36] formation/dissolution of conductive nanofilaments (CNFs) by ion migration from active electrodes or by boron vacancies within the h-BN film. The dominating mechanism is dependent on the material choices (e.g., inert vs active metal) and electrode/h-BN processing (evaporated versus transferred electrode and exfoliated versus CVD-grown h-BN).[36,42] The combinations of these would determine whether the conductive switching is due to a conductive path formed primarily by metallic ion penetration into the h-BN film[21,36] or through the restructuring of boron vacancies.[43] Either way, defects in the CVD-grown h-BN film (grain boundaries, vacancies, etc.) play a significant role. In this work, the use of an active metal (Ti top electrode) likely

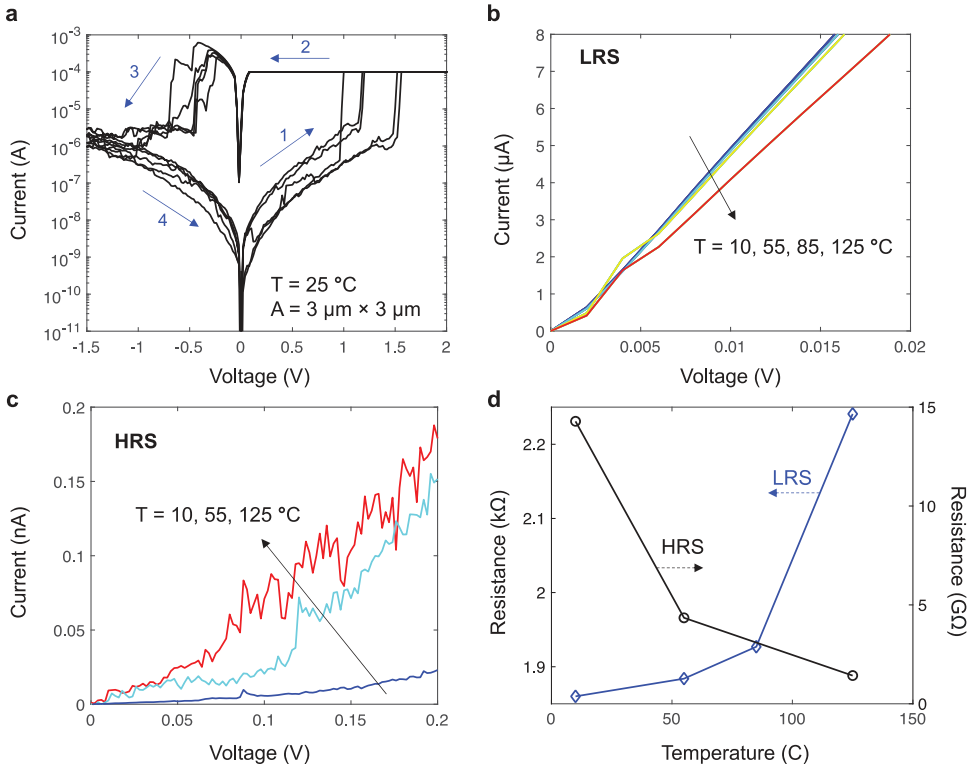

Figure 2. a) Room temperature current-voltage (I–V) characteristics measured on a few-layer h-BN memristor with 3 μm × 3 μm active area (five consecutive cycles are shown). The arrows with number labels indicate the direction of the voltage sweep and corresponding measured currents (positive set phase compliance current at 100 μA and negative reset phase compliance at 1 mA). b) I–V_{read} characteristics in the low-resistance state (LRS) measured at various temperatures show an increase in resistance with temperature. c) The I–V_{read} characteristics in the high-resistance state measured at various temperatures show a decrease in resistance with increasing temperature. d) LRS/ HRS resistance plotted as a function of the measurement temperature.

results in a dominant CNF mechanism by the penetration of the metallic Ti ions into the h-BN stack at regions of preexisting defects within the rigid crystalline lattice.[36,42] This mechanism is similar to the aforementioned CBRAM [9–11]with the exception of the rigid and layered nature of the h-BN dielectric where filament growth opportunities are restricted to percolation regions along native clusters of defects. Metallic ohmic conduction, consistent with the formation of CNF by penetration of Ti, is supported through temperature data in this work.[41] While recent work [41]has explored time-dependent metallic filament formation in h-BN memristors by DC *I–V* sweep-rate dependent extractions of set voltage, here we present a more direct observation based on measurements of their transient response to applied voltage pulses within nanosecond timescales. Specifically, we have measured transient current and voltage characteristics of h-BN memristors in response to short voltage pulses and observed the effect of tuning pulse parameters (amplitude, rise/fall time, etc.) on filament formation (via resistive switching).

Figure 3 illustrates the effect of adjusting the positive programming pulse amplitude (V_{set}) on the resistive switching transient behavior (in both set and reset phases) over ten cycles. The amplitude ranges from ≈1.05 to 1.35 V (an extended version is provided in supporting Figure S4, Supporting Information). Note that in these measurements the negative programming pulse voltage amplitude (V_{reset}) was kept constant at ≈−1.5 V. A timing diagram illustrating the pulse programming characteristics is shown in Figure 3a. When plotting conductance as a function of time through both set and reset phases (Figure 3b) we observe consistent switching between two resistive states (HRS and LRS), even under current self-compliance (no external compliance is imposed). Also, with increasing V_{set} we observe larger current and conductance. We note that to isolate the transient characteristics of the device, we have accounted for charging currents resulting from the testing apparatus (see supplementary section Figure S2, Supporting Information) by subtracting transient signals measured when probes are lifted from the test structure (h-BN memristor).[44] The set latency (t_{set}) is measured/extracted from the midpoint of the positive programming pulse voltage ramp to the midpoint of the resulting conductance transient during the transition from HRS to LRS (inset Figure 3a). The reset latency (t_{reset}) is measured similarly during the LRS→HRS transition. Using the transient signals, we can also directly obtain switching energies by integrating the electrical power ($P = IV$) over time through the transition (HRS→ LRS for "set" energy or E_{set}, and LRS→ HRS for "reset" energy or E_{reset}). To provide a fair comparison across different V_{set} we adjust the analysis to fix the midpoint values of conductance at which we extract latency and energy. In other words, we normalized the extraction to account for the different conductance that results from having different V_{set}. This type of normalization would not be required in cases where current is limited/fixed by external (equipment) or internal compliance (e.g., using series selectors or transistors). Figure 3c plots the average t_{set} (average over all 10 cycles) as a function of V_{set} with and without normalization, and Figure 3d plots the average E_{set} with and without normalization. Including normalization, results in the average E_{set} characteristic (shown in blue) decrease with increasing V_{set}. Correspondingly, a much lower t_{set} is achieved with increasing V_{set} (Figure 3c). Thus, normalization has allowed us to extract the true trend of the memristor programming latency and switching energy as a function of V_{set}. The resulting set latency and switching energy trends are both comparable to current research[13,18,21,35,43] and commercial data.[4,19,45]

Even more interesting and crucial for optimizing latency is the reset phase. With increased V_{set} it is noticed during the transient response that there is increased cycle-to-cycle variation and an impact on the reset time as the conductive filament strength increases offering increasing levels of resistance to dissolution. The extended version of this analysis in supplementary Figure S4 (Supporting Information) shows a trend toward sturdier filaments with increasing V_{set} as evidenced by increased current and increased opposition to dissolution. A quantitative measure of this effect is illustrated in Figure 3e,f where extracted reset latency (t_{reset}) and reset energy (E_{reset}) are shown to increase with V_{set}. An interesting observation is that a wider spread in conductance (over the various cycles) is observed during the reset transients at the lower conductance levels (<25% of the initial conductance), especially for large V_{set}. This is attributed to having an increasing fraction of conductive filaments in the distribution experiencing robustness to reset/dissolution as V_{set} increases. In some cases, the measurements do not extend beyond the timescale where one would see a full reset. In those cases, a larger V_{reset} may be required to break the filaments which is not shown here since this experiment focused only on the trends with varying V_{set}. We note that these parameters (t_{reset} and E_{reset}) can be improved (lowered) if V_{set} amplitudes are reduced relative to the fixed negative pulse amplitude. As is now apparent, the programming speed and switching power of h-BN RRAM is dominated by the higher reset latencies.[21]

Further tweaking and tuning for more competitive latencies and energies can be obtained by investigating the effects of programming pulse rise/fall times. The transient behavior (conductance vs time) plotted in **Figure 4a** illustrates the impact of programming pulse rise/fall time over ten set/reset cycles with fixed positive and negative programming pulse amplitudes (+/− 1.5 V). Here, shorter rise/fall times result in larger dI/dt[5] attributed to faster filament formation. Figure 4a also reveals that longer rise/fall times (e.g., 200 ns) result in conductive filaments not fully resetting within the allotted pulse time (more details in supplementary Figure S5, Suppoting Information). Nonetheless, using the data with a successful reset we can extract t_{set} and E_{set} as a function of the programming pulse rise/fall time. The extractions are plotted respectively in Figure 4b and Figure 4c and show a reduction in set latency and correspondingly a reduction in programming energy as the pulse rise/fall time is reduced from 150ns to 50 ns. Due to test equipment limitations in driving pulse rise/fall times below 50 ns we extrapolate the data to obtain estimates of set latency ($t_{set)}$ and set energy ($E_{set)}$ toward smaller rise/fall times. For example, we show that t_{set} and E_{set} can be lowered to ≈25 ns and 10 pJ, respectively for programming pulses with short rise/fall times.

A comparison plot in Figure 4d illustrates the benchmarking of our device switching energy (E_{set}) versus other academic and commercial devices. In this data set, we have grouped the devices into two separate operating modes: volatile and nonvolatile. In volatile modes, the low compliance current results in weaker filaments ensuring volatility hence lower switching energies required [38,46] (fJ ranges). This would be a similar range expectation

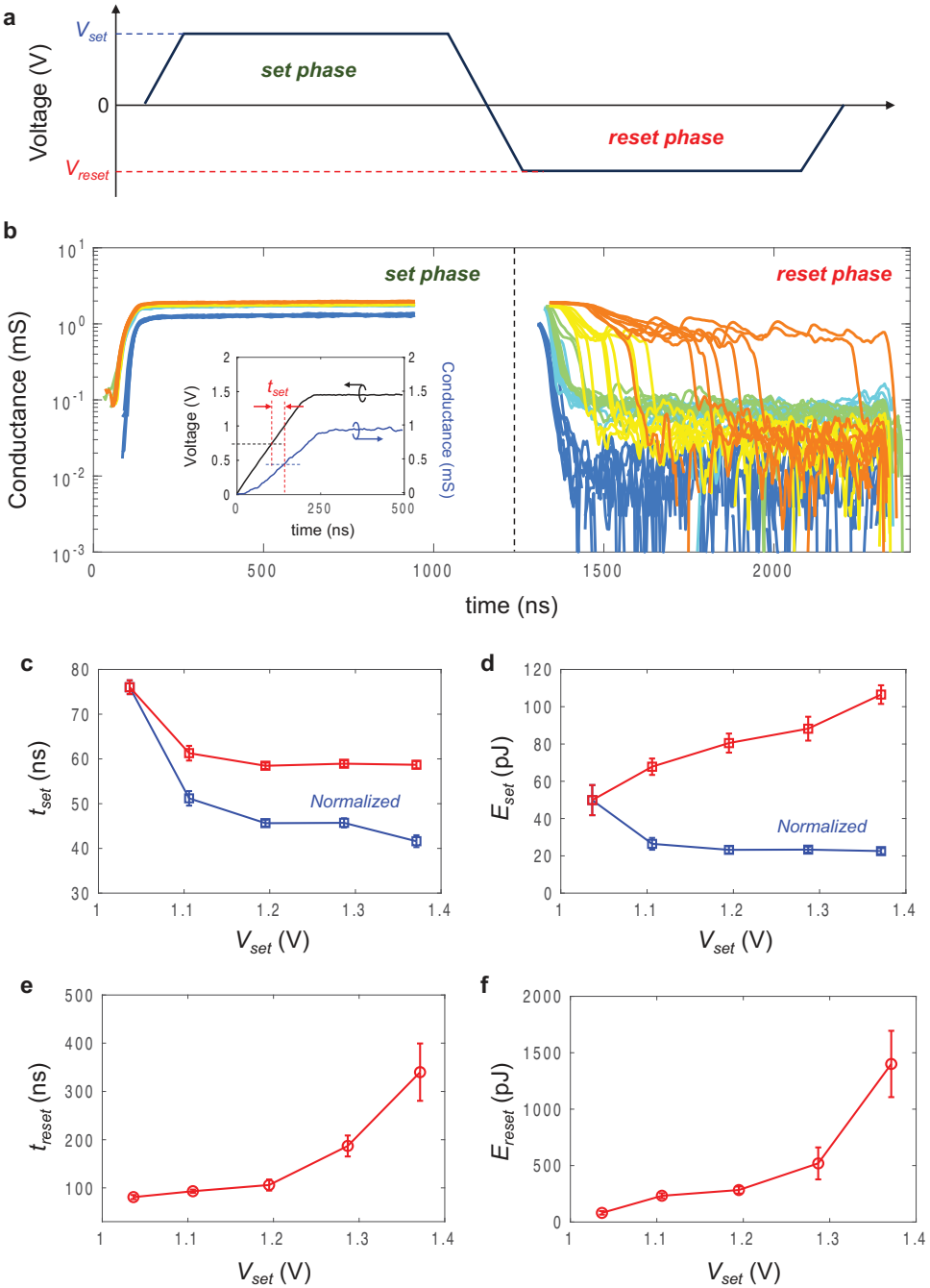

Figure 3. a) Timing diagram illustrating the applied programming pulse set and reset phases. b) Conductance transient response with increasing amplitude of the applied positive voltage pulse (V_{set} ≈1.04, 1.12, 1.20, 1.29, 1.37 V) while the reset phase applied voltage remains at −1.5V. c) Average set latency (t_{set}) (over ten cycles) for increasing V_{set}. Shown in blue are average latencies based on the normalized conductance (see text). d) Average set energy (E_{set}) (and normalized set energy in blue) over 10 cycles for increasing V_{set}. e) Effect of V_{set} on reset latency (t_{reset}) averaged over 10 cycles. f) Effect of V_{set} amplitude on reset energy (E_{reset}) averaged over 10 cycles.

in this work if using low compliance currents to ensure volatility. With nonvolatile devices stronger filaments are formed and need more current and hence result in higher switching energies. The work presented in this paper is not using current compliance and thus ensures nonvolatility. Our results indicate more competitive set switching energies (10–22 pJ) compared to the commercial 6 nJ NAND,[47] 10 pJ MRAM,[48] and the two Metal Oxide-based RRAM (MO-RRAM) with 64 pJ and 24 nJ respectively.[45,49] Similar comparison with set latency data is provided in the supplementary section Figure S7 (Supporting Information) where this work (25–41 ns) presents within the same order as non-volatile h-BN[21] and commercial data for MRAM and MO-RRAM devices

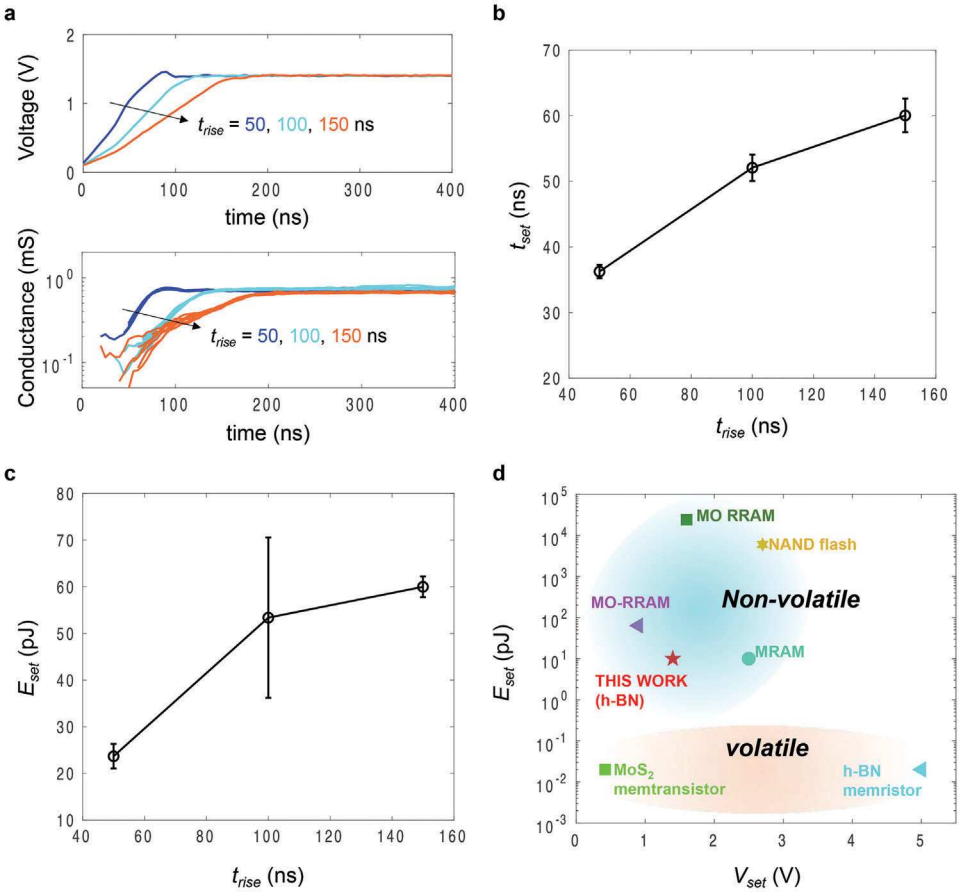

Figure 4. a) Applied positive voltage pulse (top) and resulting conductance (bottom) transient response with increasing voltage pulse rise time (indicated by the colors). b) Average set latency (t_{set}) as rise time(t_{rise}) is increased. c) Average set energy (E_{set}) versus t_{rise}. d) Set energy (E_{set}) comparison with previous works.

(10–20 ns)[47–49] with potential to be further optimized with fewer h-BN layers.[20,36,42,50]

Figure 5a shows 10 cycles of transition from HRS-to-LRS of a single device at two different temperatures, 10 °C (blue) and 125 °C (red). This shows a decreased average LRS state at 125 °C of 1.16 mS from 1.25 mS at 10 °C. This experiment was then repeated for several device samples, as illustrated in Figure 5b and Figure 5c where set latency (t_{set}) and set energy (E_{set}) are captured and averaged over 10 cycles. To account for the LRS state conductance difference between the two temperatures, a fixed current

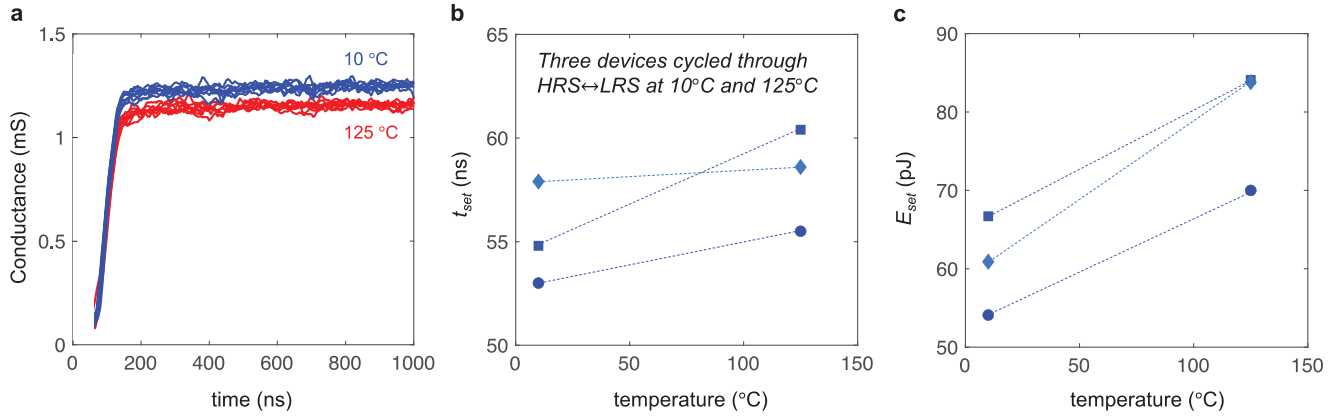

Figure 5. a) Resulting conductance transient response with temperatures at 10 °C(blue) and 125 °C(red). b) Average set latency (t_{set}) response measured across temperatures for various devices. c) Average set energy (E_{set}) response measured temperature for various devices.

threshold (LRS at 125 °C) is used as a normalization measure. The intention of this work is to understand how the switching characteristic varies with temperature. The trend shows that with increasing temperatures there is an increase in both t_{set} of ≈5–10 ns and E_{set} of ≈20 pJ. One theory to the increasing temperature trend is that the effective metallic conductivity of the growing filament decreases with increasing temperature hence more time and energy are required to form a wider filament to meet the same level of conductance achieved at lower temperatures. In other words, the metallic dI/dt rate drops, and hence set latencies increase. Nevertheless, further analysis is needed to fully elucidate the temperature dependence of transient behavior in h-BN memristors.

3. Conclusion

The transient behavior and characteristics of the RRAM as an effective switching device for synaptic update are explored and tuning parameters for optimization of set/reset latency and switching energy metrics. The transient measurements used device self-compliance which ensures devices are well into the non-volatile RS behavior region but means higher currents are required to dissolve the conductive filaments. Switching results illustrate comparative data to commercial and research work even with measurement tool limitations. While the sample size is small, results illustrate h-BN RRAM as a promising 2D device for further exploration. Current studies illustrate device yield and variation challenges and its continued development is spurred by the promise of extremely low current, low switching voltages, and high integration compared to oxide RRAM devices. As of the printing of this work, there is no known commercial device that exhibits all the requirements for the effective synaptic update for neuromorphic computing–large resistive ratios, fast switching times, <10 pJ switching energies, >10 years retention time. Commercial memory is optimized and designed for specific of these metrics but not within a single device. This work studied means to make these metrics more competitive with opportunities to further enhance and optimize by tuning h-BN layer thickness and area of the h-BN memristor device.

4. Experimental Section

Fabrication of h-BN Memristor Arrays: The h-BN memristor arrays were fabricated on a cleaned SiO_2/Si wafer. First, 5 nm Ti and 25 nm Au were deposited on the blank wafer via e-beam evaporation method. Photoresist was spin-coated and patterned by standard lithography process to form the pattern arrays of bottom electrode. Exposed Au and Ti in the photoresist-uncovered regions were removed by Ar sputtering and Ti etch process respectively, then the pattern of bottom electrode in photoresist was transferred onto Au/Ti electrodes after removal of the photoresist. Subsequently, CVD-grown h-BN on copper foil, which was purchased from Six Carbon Technology, Shenzhen, was wet-transferred onto SiO_2/Si wafer with patterned Ti/Au bottom electrodes. Another lithography process was used to pattern the h-BN active region covered by photoresist, and the h-BN at the exposed regions was etched away by oxygen plasma to expose the bottom electrodes underneath. Finally, photoresist was spin-coated again and patterned for 25 nm Ti/25 nm Au top electrodes deposition and liftoff.

Electrical (DC and Transient) Characterization of h-BN Memristors: The DC electrical characterization was conducted on the Cascade semiautomatic probe station using a Keithley 4200 semiconductor characterization system (SCS) using the Source Measure Units (SMUs). The transient measurements were conducted on the Keithley 4200 SCS using the pulse measure units (PMU, model 4225) for programming pulses. The custom test script was written on the Keithley 4200 SCS using the Keithley User Library Tool (KULT) and executed in the Keithley Interactive Testing Environment (KITE). The input parameters to the test script were the pulse width (500 ns), period (1 ms) and rise and fall times (limited to >50 ns) as well as the amplitude positive and negative values ranging from 1.2–2 V. The negative excursions were limited to 1.5 V. Temperature analysis were done by using the Temptronic TP03000 ThermoChuck System (LM02350) whereby temperatures were ramped to 10–125 °C (in 25 °C increments) allowing 15–20 min to soak at each temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

M.M.N., J.X and H.W. performed electrical characterization, J.X. fabricated the h-BN devices. M.M.N., I.S.E. conceived and designed the experiments. MMN, I.S.E. analyzed the experimental results. M.M.N,S.A, J.X.,H.W., I.S.E., wrote the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D RRAM, 2D semiconductors, h-BN, memristors

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