A 5 MHz Capacitor-Isolated Resonant SEPIC DC-DC Converter with a Wide Input Voltage Range

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***Abstract*—High-frequency transformers are typically used in high power density converters requiring isolation or high voltage conversion ratio. However, increased core losses limit the switching frequency to around 1 MHz to maintain low losses and compact form factors. To address this, capacitor-isolated designs are introduced, enabling multi-MHz solutions with low losses, though voltage conversion capabilities pose a concern. This paper presents a 5 MHz capacitor-isolated DC-DC converter based on resonant SEPIC topology, achieving a wide input voltage range with a maximum voltage gain of 8. To minimize losses, the soft-switching operation is implemented across wide input voltage and output power ranges. Additionally, a voltage feedback loop using a hysteresis controller is designed to ensure precise output voltage regulation. The specific parameter design process is proposed in this paper. The hardware is developed with an operation voltage below 100 V and power levels ranging from 41 W to 168 W, making it suitable for various power sources such as batteries or renewable energy sources. Experimental results are provided to demonstrate the feasibility of the design.**

Keywords—Resonant SEPIC topology, capacitor-isolated converter, high-frequency, soft-switching

I. INTRODUCTION (1.5)

In many applications, such as renewable energy systems, electric vehicles, and medical devices, the output voltage of power sources varies significantly due to fluctuating environmental conditions, diverse battery charging inputs, and varying mechanical energy inputs [1]-[3]. To ensure consistent and effective system operation, converters with wide input voltage ranges and narrow output voltages are necessary. Additionally, the ability to step up and down voltages is preferred to accommodate different power sources effectively. Furthermore, considerations such as converter stacking, and the necessity for safe installation and service, and effective isolation are required.

Conventionally, transformers have been used to provide isolation and flexible voltage conversion ratios. Through high-frequency operation, compact designs can be achieved, which is good for system integration purposes. However, as the switching frequency exceeds 1 MHz, the core loss density of ferrite materials in transformers increases dramatically [4], [5]. This makes it difficult to maintain both a compact transformer size and low core losses simultaneously, thereby limiting improvements in converter size and efficiency. To address these limitations, capacitor-isolated designs have been proposed as an alternative solution. These designs use capacitors as the coupling element between input and output ports, leveraging the electric field as the medium for energy transfer. This approach allows for high-frequency operation without the associated core losses, enabling more compact and efficient designs.

However, capacitor-isolated designs offer less flexibility in the converter voltage conversion ratio compared to transformer-isolated designs. [6], [7] have presented capacitive isolation converter designs with a limited voltage gain of 1.25. To overcome this limitation, converter topologies with a broad operating voltage range and high voltage gain need to be considered. The SEPIC converter is a widely recognized topology capable of both step-up and step-down voltage conversion without reversing the output voltage polarity [8]. By using two split capacitors as the isolation barrier, a conventional SEPIC converter can be adapted into a capacitor-isolated converter. However, its hard-switching operation and high voltage stress on power devices result in low efficiency, making

it unsuitable for MHz range operation. To address this, a quasi-resonant SEPIC converter with soft-switching capability is proposed by [9]. However, the design faces challenges due to the need for large input choke inductors that provide a constant current. These inductors typically require magnetic materials to achieve high inductance, which is difficult to realize at high frequencies with minimized losses.

As an alternative, many topologies proposed in the field of RF amplifiers, such as Class E and Class F use finite input inductors, use finite input inductors paired with additional capacitors to provide soft-switching capability, and avoid bulky inductors. Combining Class E and F operations, the Class EF2 topology offers low transistor voltage stress [10]. Nonetheless, this circuit requires many passive components and precise tuning for proper operation. Additionally, these topologies are typically used for low voltage and power applications, such as below 10 V and a few watts, with a narrow voltage operation range. Inspired by quasi-resonant SEPIC and power amplifier topologies, [11] proposed a resonant SEPIC converter that utilizes resonant LC pairs for soft-switching realization for both devices. By employing LC pairs in parallel resonance, higher gain could be achieved. However, [11] demonstrated non-isolated designs only at low voltage and power conditions. No specific analysis of the wide operation voltage range effect on the converter design and soft-switching analysis. Therefore, modifications are required to make it suitable for broader applications. Nevertheless, it became a good candidate for this application.

TABLE I. SPECIFICATIONS OF THE DESIGNED DC-DC CONVERTER

Parameter	Symbol	Values
Input voltage	V_{in}	10-80 V
Output voltage	V_o	60-80 V
Output power	P_o	42-167 W
Operating frequency	f_{sw}	5 MHz
Isolation method		Capacitive

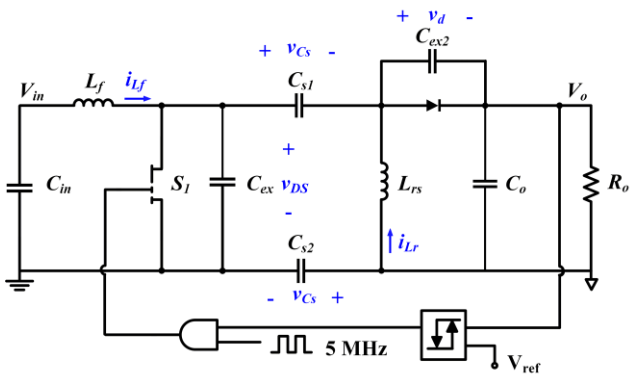


Fig. 1 Schematic of the designed capacitive isolation resonant SEPIC converter.

Overall, this paper presents a resonant SEPIC converter with a wide input voltage range using capacitor isolation, capable of a maximum output power of over 167 W, and operating at 5 MHz Table I lists all the specifications of the designed converter. To minimize losses, achieving Zero Voltage Switching (ZVS) is essential. However, realizing ZVS over a wide input voltage range while minimizing the switching device's reverse conduction losses poses a significant challenge. This paper addresses this challenge by discussing the design guidance for the converter over a wide voltage range. The developed hardware prototype is also presented to demonstrate the concept.

The paper is organized as follows: Section II presents an overview of the capacitive isolated resonant SEPIC converter. The circuit configuration as well as the basic working principle are presented. Section III discusses design considerations for resonant SEPIC over a wide voltage range with ZVS realization. Then, in Section IV, the hardware prototype of the developed 5 MHz and the test results are provided. Finally, Section V concludes the main results.

II. PRINCIPLE OF OPERATION

In this converter, as shown in Fig. 1, a single-switch topology is utilized. The switch S_1 is placed on the input side, and a single diode D is connected to the output terminal. The converter includes an input resonant inductor L_f and a resonant capacitor C_{ex}, which is placed across the main switching device S_1. This capacitor C_{ex} represents both the device output capacitors and additional external capacitors.

To achieve isolation, the impedance-matching capacitor used in previous designs is split into two capacitors, C_{s1} and C_{s2}, which are inserted into the positive and negative rails of the converter. In this modified configuration, C_{s1} and C_{s2} not only serve as the isolation barrier but also function as the medium for energy transfer. For soft-switching of the diode D, additional capacitors C_{ex2}, including the diode junction capacitors, are incorporated. These capacitors resonate with L_{rs} to realize ZVS.

To precisely control the output voltage, a feedback loop is added. The specific design and operation of this feedback loop will be discussed in the following section. It is important to note that the switching frequency of the feedback loop is low, ensuring it does not interfere with the overall operation of the converter. For steady-state analysis, the feedback loop is assumed to be continuously enabled, thus the transient behaviors caused by the switching events of the feedback loop are not considered. When the feedback loop is turned off, the converter ceases to operate, and therefore, the turn-off period of the feedback loop is not discussed here. The operational waveforms of the converter during the feedback-enabled period are illustrated in Fig. 2.

In steady-state operation, a complete switching cycle can be divided into five stages based on the different switch operation

states, starting from the moment S_1 turns on. Before S_1 is turned on, C_{s1} and C_{s2} are fully charged. Diode D is off with its reverse bias voltage in the discharging state. The following description summarizes the circuit operation during each of the five stages with the equivalent circuit for each stage shown in Fig. 3.

1) Stage I [T_0, T_1]:

Due to ZVS realization, the drain-source voltage v_{DS} of S_1 reaches 0 V before T_0. At T_0, S_1 turns on, and v_{DS} remains at 0 V. During this period, inductor L_f is continuously charged by the input voltage source V_{in}, causing the current i_{Lf} to rise. Simultaneously, capacitors C_{s1} and C_{s2} discharge through the device S_1 and charge L_{rs}. Capacitor C_{ex2} also discharges by transferring energy to inductor L_{rs}. As a result, the voltage across L_{rs} increases and reaches the output voltage V_o, which means the voltage across C_{ex2} reaches 0 V at T_1. Then the diode D starts to conduct. The equivalent circuit of this stage is shown in Fig. 3(a).

2) Stage II [T_1, T_2]:

At T_1 the diode D turns on while S_1 remains on. At this moment, the entire input current i_{Lf} flows through S_1. Inductor L_f continues to charge until S_1 turns off at T_2. Due to the conduction of D, the voltage across both capacitors C_{s1} and C_{s2}, denoted as $2v_{Cs}$ is clamped at the output voltage of $-V_o$. With the selection of identical capacitors, the voltage across C_{s1} or C_{s2} is $-0.5V_o$. Consequently, due to this constant voltage, no current flows through C_{s1} and C_{s2}. Inductor L_{rs} is continuously charged through diode D by the output capacitors, as shown in Fig. 3(b).

3) Stage III [T_2, T_3]:

At T_2, S_1 turns off. L_f resoances with C_{ex}. A portion of the inductor current i_{Lf} flows into the device parallel capacitor C_{ex}, causing the voltage across C_{ex}, illustrated as v_{DS} to rise. Meanwhile, C_{s1} and C_{s2} begin charging through the input current i_{Lf}, resulting in the discharge of inductor L_f. In the half-wave mode operation, due to the conduction of the diode, the voltage across inductor L_{rs} remains clamped at $-V_o$. The current from C_{s1} and C_{s2} charges inductor L_{rs} and supplies the output through the diode. The voltage across C_{ex}, and C_{s1} and C_{s2} increases at the same rate, with a difference of V_o. Both L_{rs} and the output capacitors are charged by C_{s1} and C_{s2} until T_3, when the diode D turns off.

4) Stage IV [T_3,T_4]:

At T_3, diode D turns off while S_1 remains off. Inductor L_f is initially discharged by C_{ex}, and C_{s1} *and* C_{s2} until C_{ex} reaches its maximum voltage. Subsequently, C_{ex} discharges along with L_f to charge C_{s1} and C_{s2}. After i_{Lf} reaches 0 A, a negative current provided by C_{ex} continues to discharge L_f while C_{s1} and C_{s2} are charged by C_{ex} until T_4, when C_{ex} is completely discharged and S_1 is ready to conduct in the reverse direction. Inductor L_r is first charged by and C_{ex2}. After reaching its maximum value, it is mainly discharged by C_{ex2}.

5) Stage V [T_4, T_5] :

As the current i_{Lf} continues in the negative direction, S_1 conducts in reverse at T_4. ZVS is realized for S_1 since it remains off during this period. L_f begins charging from V_{in}, while C_{s1} and C_{s2} start charging through S_1 via L_{rs} until reaching their maximum voltage. Subsequently, C_{s1} and C_{s2} discharge through L_f, charging L_{rs}. Meanwhile, C_{ex2} discharges through L_{rs} until v_{cs} drops to 0 V.

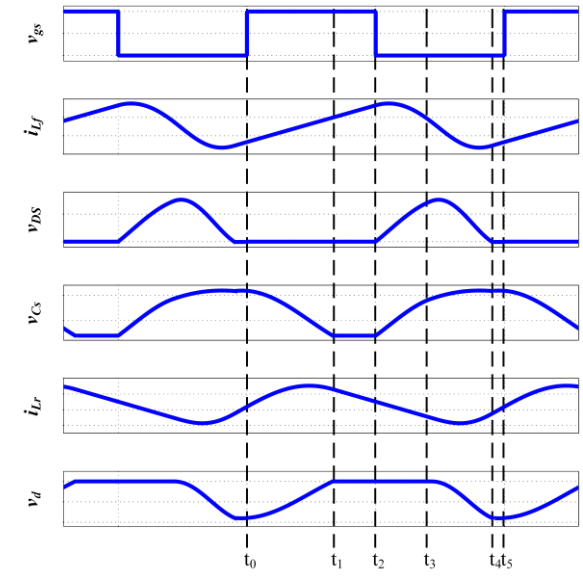


Fig. 2 Waveforms of the resonant SEPIC converter.

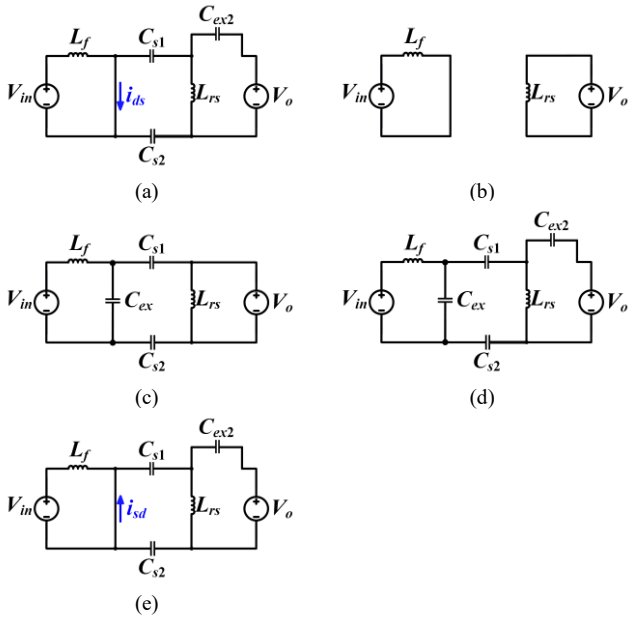


Fig. 3 The equivalent circuits for capacitive isolated resonant SEPIC converter during five stages. (a) [T_0, T_1]. (b) [T_1, T_2]. (c) [T_2, T_3]. (d) [T_3, T_4]. and [T_4, T_5].

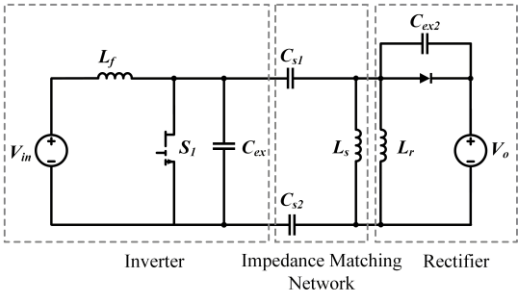


Fig. 4 Three subsystems of a resonant SEPIC topology.

III. Design Considerations

The design procedure for the resonant SEPIC converter can be simplified by dividing the system into three subsystems: the inverter, the impedance matching network, and the rectifier circuits, as illustrated in Fig. 4. Typically, such designs are developed based on fixed voltage and power conditions [12]. However, this converter operates over a wide voltage range, causing significant variation in device parasitic capacitors, which can impact overall converter performance. These challenges will be addressed throughout the design process to ensure optimal functionality and efficiency of the converter across its entire operating range. The design process begins with the rectifier side, followed by the inverter and impedance-matching network. Detailed design procedures for each subsystem will be illustrated in the following sections.

A. Resonant Rectifier Design

The resonant rectifier topology shown in Fig. 5 consists of a capacitor C_{ex2}, which includes both external capacitors and the diode junction capacitor, and a resonant inductor L_r that is utilized to adjust the overall impedance of the rectifier circuit. To mimic the inverter behavior, a sinusoidal current source operating at the switching frequency is used as the input. At the output, a constant voltage source is modeled since the closed-loop control is implemented, as depicted in Fig. 1.

To optimize the rectifier performance, ensuring resistive impedance at the fundamental frequency is essential to prevent circulating currents that cause additional losses. This equivalent resistance can be derived from the fundamental voltage waveform V_{Lr} and the sinusoidal current waveform that can be calculated as follows:

$$Z_r(f_s) = \frac{v_{Lr}(f_{sw})}{i_{in}} \tag{1}$$

As a starting point, C_{ex2} can be initially designed using only the diode junction capacitor. Since L_r and C_{ex2} resonate during the diode turn-off period, the L_r value can then be adjusted accordingly during this resonant period. Fig. 6(a) shows the V_{Lr} waveform and its fundamental frequency component. As a result of the resistive characteristics, the fundamental component of V_{Lr} should be in phase with the input current i_{in}, as shown in Fig. 6(b).

Fig. 7 illustrates the fundamental frequency of V_{Lr} and the phase difference between the fundamental frequency of V_{Lr} and the input sinusoidal current waveforms. However, in this case, L_r can only be adjusted based on a specific capacitance value. Given the wide voltage range of operation in this design, the junction capacitance, which constitutes C_{ex2}, varies significantly. For example, with the junction capacitance ranging from 180 pF to 300 pF, the V_{Lr} waveforms are affected considerably, as shown in Fig. 7(a), causing changes in both the phase and magnitude of the fundamental component. This results in the loss of the rectifier's resistive characteristics.

To address this, adding additional capacitors can help mitigate these effects. For example, adding 1.8 nF capacitors in parallel with the diode helps mask the capacitance variation. Fig. 7(b) shows simulation results with these additional capacitors. Under this condition, the overall phase of V_{Lr} remains relatively stable with a fixed L_r. Although the phase would still change, as mentioned in [12], slightly inductive or capacitive impedance characteristics are acceptable in the circuit operation. However, it is important to note that the total capacitance will affect the reverse voltage and the conduction time of the diode, as shown in Fig. 7(a). Therefore, diode-associated losses need to be considered in the circuit design to help select the final resonant component values.

As mentioned above, the optimal operating point of the rectifier is when it exhibits resistive characteristics from the input. In this design, this point is selected under heavy load conditions, with an output of 60 V and an output power of 167 W, to ensure good efficiency. To address the variation of the junction capacitance, additional capacitors are added, and L_r is tuned under heavy load conditions. After considering losses, Lr is selected to 0.554 μH, and an external capacitor of 1.1 nF is placed in parallel with the diode. This approach helps the converter maintain optimal performance and efficiency across its wide operating voltage range.

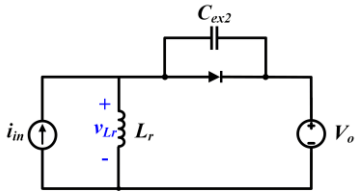
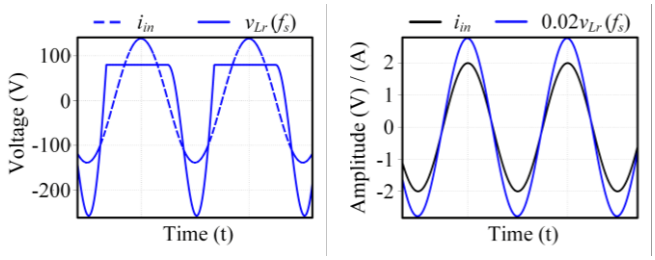
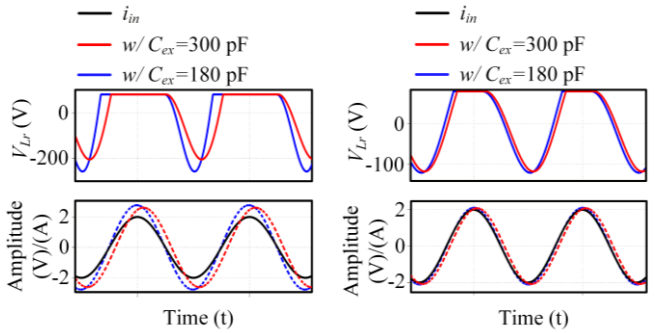


Fig. 5 Model of the resonant rectifier circuit.



(a) (b)

Fig. 6 Simulation waveforms: (a) V_{Lr} and its fundamental component, and (b) comparison between input current i_{in} and the scaled-down fundamental component of V_{Lr}



(a) (b)

Fig. 7 Simulation waveforms of V_{Lr}, a scaled-down fundamental component of V_{Lr} ($0.02V_{Lr}$), and input current i_{in} with (a) resonant rectifier tuned with diode junction capacitors only, and (b) resonant rectifier with an additional 1.8 nF capacitor in parallel with the diode.

B. Impedance Matching Network Design

The impedance matching network, placed between the inverter and rectifier stages, is used to match the rectifier's input impedance with the inverter's output impedance. This impedance alignment ensures efficient power transfer and provides electrical isolation for the applications.

Based on its input voltage and current waveforms at the fundamental frequency, the rectifier circuit can be modeled as an equivalent impedance, denoted as Z_r, under different voltage conditions at the output of the impedance matching network, as depicted in Fig. 8. In this converter the output impedance of the inverter is lower than the input impedance of the rectifier, so an L-shape matching network is employed to adjust the impedance accordingly. In addition, by splitting the capacitor into two identical capacitors, C_{s1} and C_{s2}, capacitor isolation can be achieved. This configuration blocks the DC values through C_{s1} and C_{s2}, enabling the converter to provide both up-and-down voltage conversion capabilities.

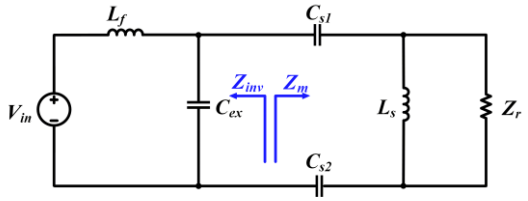


Fig. 8 Equivalent circuit of the converter when the switch is open, with the rectifier circuit modeled as an impedance Z_r.

The goal of the impedance matching network is to ensure that the inverter's output impedance (Z_{inv}) matches the input impedance of the matching network (Z_m) around the switching frequency. When properly matched, Z_{inv} and Z_m align, achieving maximum power transfer near the switching frequency. Although varying voltage conditions affect the parasitic capacitance of the switching devices, the matching network is designed to optimize power transfer under heavy load conditions. During light load conditions, the impedance profile will differ slightly but still maintain similar performance and high efficiency.

C. Inverter Design

The resonant inverter topology employs a small-valued inductor, L_f, to resonate with C_{ex}, which includes the GaN device's output capacitance as well as external capacitors. When the switch is off, the inverter circuit exhibits impedance Z_{inv} from the output terminals. In this design, the L_f, and C_{ex} resonant during the device's turn-off period, defining the overall shape of the drain-source voltage waveform.

For an inverter operating at a 50% duty ratio, a recommended starting point is to tune the input resonant network to twice the switching frequency:

$$f_{r1} = \frac{1}{2\pi\sqrt{L_f C_{ex}}} = 2f_{sw} \tag{2}$$

Similar to the resonant rectifier design, L_f is designed for heavy load conditions to ensure good efficiency under such conditions. To reduce the effect of the GaN device's parasitic capacitance and reduce the voltage stress, additional capacitors are added across the device. Initially, the L_f is designed as 167 nF with external capacitors of 1 nF.

This tuning achieves ZVS and zero dv/dt for the drain-to-source voltage v_{DS}, with the corresponding waveforms under light load and heavy load conditions shown in Fig. 9. However, with the impedance matching network values of 0.5 µH for L_s and 6 nF for C_{s1} and C_{s2}, the v_{DS} resonant waveform reaches 0 V much earlier than the turn-on event, causing long reverse conduction time of S_1. This is significant for GaN devices due to their significant voltage drop during reverse conduction, leading to substantial conduction loss and reduced efficiency. Although ZVS is achieved, the additional reverse conduction losses are undesirable.

To address this, decreasing the resonant frequency f_{r1} can help reduce the reverse conduction time of the GaN device. By adjusting the resonant frequency to a lower value, ZVS is attained just before the turn-on event under heavy load conditions. This is achieved by increasing the inductor values to 200 nH. Fig. 10 illustrates the full converter simulation results with all the updated designed values. At light load, the GaN device still conducts in the third quadrant, but the overall conduction time is reduced compared to Fig. 9(a). Even at a

higher operating voltage condition of 80 V input and 60 V output, ZVS is still attained with minimal reverse conduction time. This adjustment leads to higher efficiency for the converter.

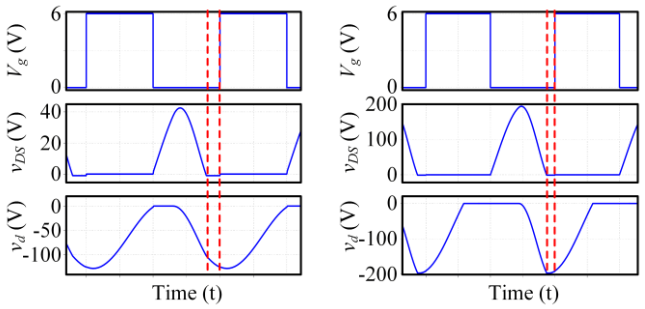


Fig. 9 Simulation results of device voltage waveforms with L_f = 167 nH under (a) light load condition of V_{in} = 10 V, V_o = 60 V, and (b) heavy load condition of V_{in} = 50 V, V_o = 60 V.

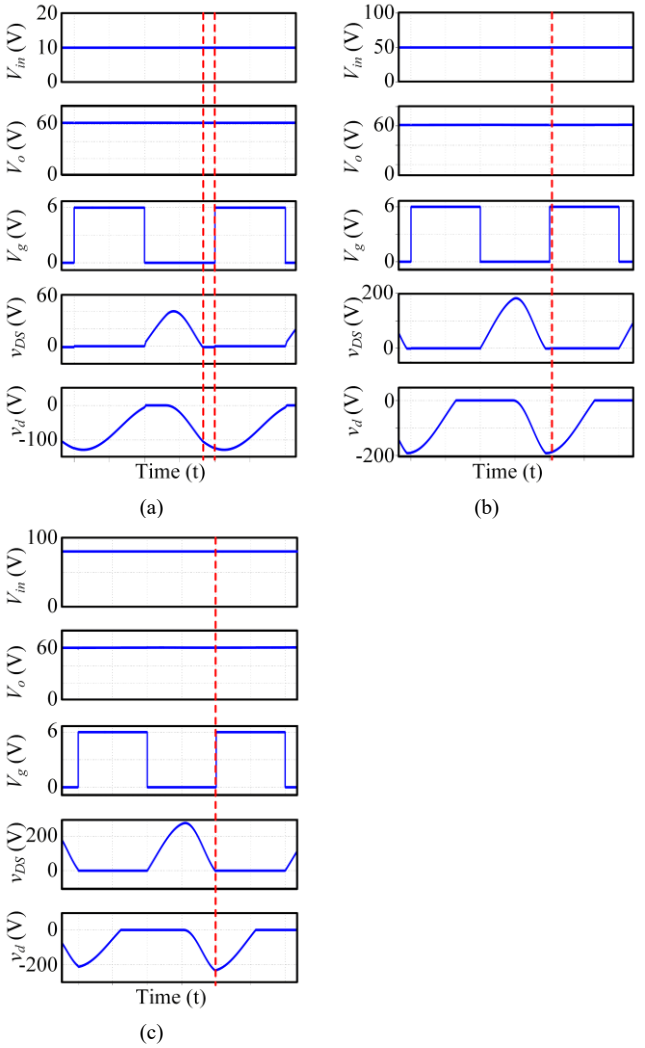


Fig. 10 Simulation results with L_f = 200 nH under (a) light load condition of V_{in} = 10 V, V_o = 60 V, (b) heavy load condition of V_{in} = 50 V, V_o = 60 V, and (c) light load condition of V_{in} = 80 V, V_o = 60 V.

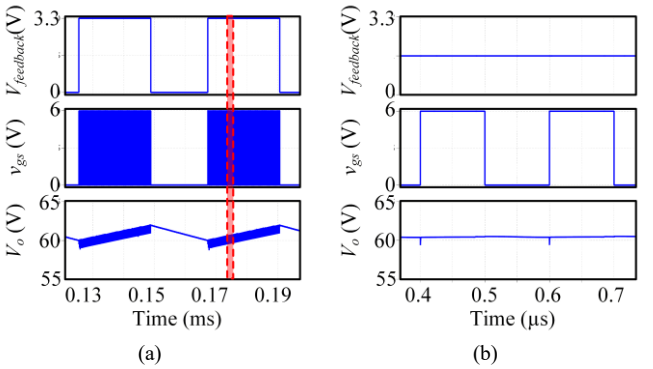


Fig. 11 Simulation results of (a) feedback signal $v_{feedback}$, gate voltage v_g and the output voltage V_o, and (b) a zoomed-in view of the waveforms during feedback signal on-period (as labeled by the red box in (a)).

D. Feedback Loop

As shown in Fig. 1, a hysteresis controller is implemented in the circuit. Due to the small input resonant inductor, the converter has a good dynamic response. When the output voltage (V_o) exceeds the upper boundary, a low signal will be sent to the primary side switch S_1. Then, the converter stops switching and the load is charged by output capacitors (C_o). Once the output voltage reaches the lower boundary, S_1 is enabled and the entire converter operates at 5 MHz. In the design, the upper and lower voltage boundaries are predetermined based on the voltage ripple requirement.

To absorb high-frequency noise and provide stable output voltage, a large output capacitance is recommended. This large capacitance also helps ensure that the feedback signal $V_{feedback}$ switches at a much lower frequency compared to the main switching frequency of 5 MHz. Fig. 11 shows a simulation example under Vin at 50 V and Vo at 60 V. With an output capacitance of 20 uF, the switching frequency of $V_{feedback}$ is around 23.9 kHz, which does not disturb the normal operation of the converter at a high frequency.

IV. Experimental Results

Fig. 12 presents the final developed hardware for the 5 MHz capacitive isolation converter. The design incorporates the main power stages, with specific component values listed in Table II, along with auxiliary components such as the oscillator, auxiliary power supplies, signal isolator, and op-amp. In the circuit design, the inductors L_r and L_s are placed in parallel and modeled as a single equivalent inductance, denoted as L_{rs}, which is utilized in the hardware application. Based on the available components, passive elements such as L_f, C_{ex}, and L_{rs} are fine-tuned for optimal performance. Air inductors are chosen to eliminate core losses, while ceramic capacitors are employed to minimize size and ensure excellent performance during high-frequency resonance. Additionally, a high-voltage ceramic capacitor is utilized for insulation purposes. For best practices, PCB cutouts are implemented beneath C_{s1} and C_{s2}, and isolated auxiliary components. In this design, the highest

voltage stress in the circuit exceeds 200 V; however, commercially available GaN devices are limited to blocking voltages either below 200 V or 650 V. Consequently, a 650 V GaN device is selected for the circuit, with the part number provided in Table II. To address diode losses and voltage stress considerations, 650 V SiC Schottky diodes are also integrated into the design.

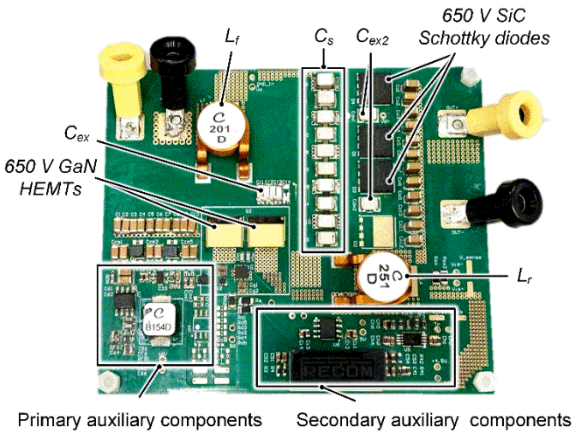


Fig. 12 Hardware prototype of the developed converter.

TABLE II. PARAMETER SELECTIONS FOR THE DC-DC CONVERTER

Parameter	Values
L_f	202 nH
C_{ex} (exclude C_{oss})	0.86 nF
C_{s1}/ C_{s2}	6 nF
L_{rs}	256 nH
C_{ex2} (exclude C_j)	1.1 nF
S_1	2x GS66516T
D	3x C6D10065Q

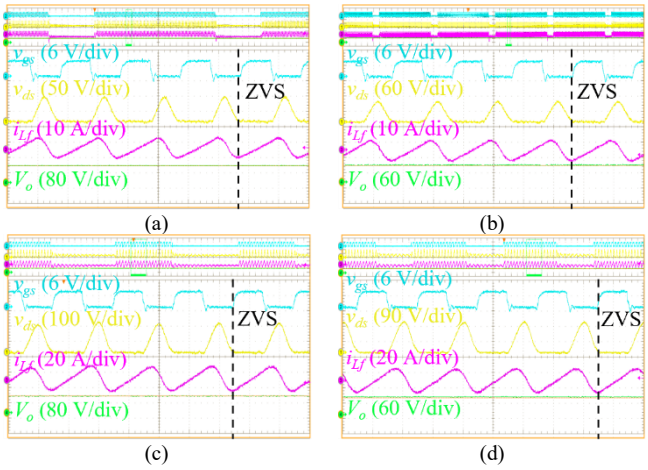


Fig. 13 ZVS verification for (a) V_{in}= 10 V, V_o= 80 V, P_o= 42 W (b) V_{in}= 10 V, V_o= 60 V, P_o= 42 W, (c) V_{in}= 50 V, V_o= 80 V, P_o= 167 W, and (d) V_{in}= 50 V, V_o= 60 V, P_o=167 W.

A. ZVS Verification

Fig. 13 presents the experimental results for both light load (42 W) and heavy load (167 W) conditions, with output voltages of 80 V and 60 V, respectively. The designed parameters allow ZVS across a wide range of voltage and load conditions, ensuring high efficiency for the converter. The test results indicate that at lower input voltages, the drain-source voltage reaches 0 V earlier compared to higher input voltage conditions. Conversely, at high input voltages, ZVS is achieved just before the next turn-on event, effectively minimizing the reverse conduction time of the GaN devices. These experimental findings align with the previously derived simulation results, validating the design procedure. Notably, the inclusion of additional capacitors in parallel with both the GaN devices and Schottky diodes helps maintain relatively consistent switching waveforms, which is advantageous for preserving optimal converter performance. It is important to mention that, at this stage, only the step-down functionality of the converter has been validated in the hardware tests.

B. Efficiency Measurement

To evaluate the efficiency of the designed converter, a power analyzer was employed. Efficiency assessments were conducted for input voltages ranging from 10 V to 50 V and output power levels from 42 W to 167 W. The results are depicted in Fig. 14.

For an output voltage of 80 V, the efficiency increases from 75% at light load to 86.7% at heavy load. Similarly, for an output voltage of 60 V, the efficiency rises from 79.85% at light load to 87.7% at heavy load. Overall, the trend indicates that the 60 V output voltage condition consistently exhibits higher efficiency than the 80 V condition across all load ranges. The maximum efficiency is observed at the heavy load condition with an input voltage of 40 V.

Through the loss breakdown analysis, it was found that at lower input voltages, AC winding losses and device conduction losses dominate the total loss. However, at higher input voltages, C_{oss} losses play a significant role. This finding is particularly relevant for high-frequency GaN applications [13]. Overall, the converter demonstrates its capability for high voltage and high-power applications with high efficiency.

C. Feedback Loop Verification

The output voltage band for the hysteresis controller was set to 10 V for easier observation and functionality verification. According to the results shown in Fig. 15, with a 10 V voltage band ranging from 52 V to 62 V, the feedback loop operates at a frequency of 45 Hz, which is significantly lower than the main switching frequency of 5 MHz. This ensures that the feedback loop does not interfere with the overall performance of the converter. Overall, the functionality of the designed hysteresis controller has been verified.

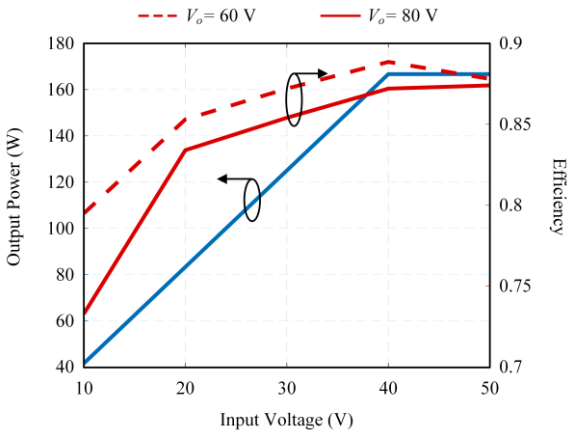


Fig. 14 Measured efficiency and power profile.

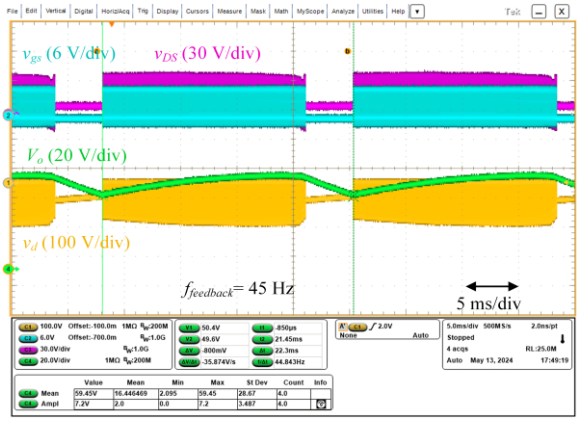


Fig. 15 Experimental results of the designed single-phase converter with closed-loop control at 10 V input and 60 V output condition.

V. Conclusion

This paper presents the design of a 5 MHz isolated resonant SEPIC converter optimized for operation at voltages below 100 V, specifically targeting an input voltage range of 10-80 V and an output voltage range of 60-80 V. The converter utilizes a modified resonant SEPIC topology to achieve high efficiency and stable performance across a wide range of input and output conditions, while also providing isolation. A key aspect of the design is addressing the significant impact of device parasitic capacitance due to the wide operating voltage range. This issue is mitigated by incorporating additional capacitors in parallel with each switching device. To ensure optimal performance under heavy load conditions, all resonant components are selected based on these scenarios. By splitting the capacitors in the impedance-matching network between the positive and negative rails, the converter achieves a capacitive isolation design, reducing its overall size.

The developed hardware effectively demonstrates its voltage step-down capability ZVS across various voltage and load conditions. Efficiency measurements indicate peak efficiencies of 86.7% for an 80 V output and 87.7% for a 60 V output, with the highest efficiency observed at heavy load conditions with an input voltage of 40 V. To ensure output voltage regulation, a hysteresis controller was developed, maintaining a low-frequency feedback loop that does not interfere with the converter's high-frequency operation. In conclusion, the designed 5 MHz capacitive isolation converter achieves high efficiency and stable operation, validating the design approach and component selections.

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