Design and Development of a Compact GaN based Three-level Flying Capacitor Inverter

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***Abstract*— In this paper, a high power three-level inverter based on 650 V commercial gallium nitride (GaN) HEMT (High-Electron-Mobility Transistor) devices is developed and demonstrated. The developed 25 kVA GaN based flying capacitor inverter building block is scalable to high power levels with parallel operation. Firstly, various multilevel inverter topologies are evaluated and compared, including neutral point clamped inverter, active neutral point clamped inverter, T-type inverter, and flying capacitor inverter. The flying capacitor inverter topology is selected considering its efficiency, power density, and cooling system design. The parasitic loop inductances are minimized with magnetic flux cancellation in the power stage design. The estimated power density of the designed flying capacitor 3-level inverter is ~15 kW/L with the realization of a compact circuit layout of the gate driver board and power stage. The power density can even be further improved by optimizing the cooling system. The developed GaN based 3-level inverter can be potentially applied in grid-tied converters, PV systems, energy storage, data centers, motor drives, etc.**

Keywords*— *Inverter, GaN, Switching Loss, Efficiency, High Frequency

I. INTRODUCTION

Wide bandgap semiconductors, such as gallium nitride (GaN) devices and silicon carbide (SiC) offer remarkable improvements in fundamental figures of merit, such as higher voltage ratings, lower on-resistance, and faster switching capabilities [1]–[4]. These advancements increase switching frequencies by an order of magnitude or more, possibly employing smaller passive components within converter circuits. Despite these advancements in semiconductor technology, traditional converter topologies have largely remained unchanged. Conventional designs have not fully exploited the potential benefits offered by wide bandgap devices.

In recent years, multilevel inverters (MLI) have gained great attention in medium voltage and high power applications owing to their various advantages such as lower common mode voltage, lower voltage stress on power switches, lower dv/dt ratio to supply lower harmonic contents in output voltage and current [5]. Comparing two-level inverter topologies at the same power rating, multilevel inverters also have the advantage that the harmonic components of line-to-line voltages fed to load are reduced owing to their switching frequencies. Four commonly used MLI topologies include Neutral Point Clamped inverter (NPC), Active Neutral Point Clamped inverter (ANPC), T-type inverter, and Flying Capacitor inverter (FLC) [6],[7].

Recent research has demonstrated that FLC converters offer substantial efficiency and power density improvements in medium-voltage, kilowatt-scale inverter applications [8]–[10]. These converters benefit from low-voltage stress on transistors and the ability to operate at high switching frequencies. This paper will demonstrate a 25 kVA multilevel inverter building block with scalability. Evaluation, comparison, and the reason for choosing flying capacitor inverter among different multilevel inverter topologies will be shown.

This paper focuses on the development of the high-frequency, compact, scalable three-level flying capacitor inverter utilizing GaN technology. We will examine how the integration of GaN devices [11] into FLC topologies can fully exploit the benefits of wide bandgap semiconductors. Key design considerations, implementation challenges, and performance enhancements will be discussed, to achieve superior power density and efficiency in modern power conversion systems. Our approach includes a detailed analysis of the inverter's design, including the selection and integration of GaN devices, optimization of the flying capacitor network, and the overall impact on system performance. Experimental results are presented to validate the theoretical predictions and demonstrate the practical advantages of the GaN based three-level flying capacitor inverter. The outcome of this research has the potential to advance the state-of-the-art in high-frequency conversion and contribute to the development of more efficient and compact power electronic systems for a variety of modern applications

II. TOPOLOGY EVALUATION

A. Inverter Topologies Comparison

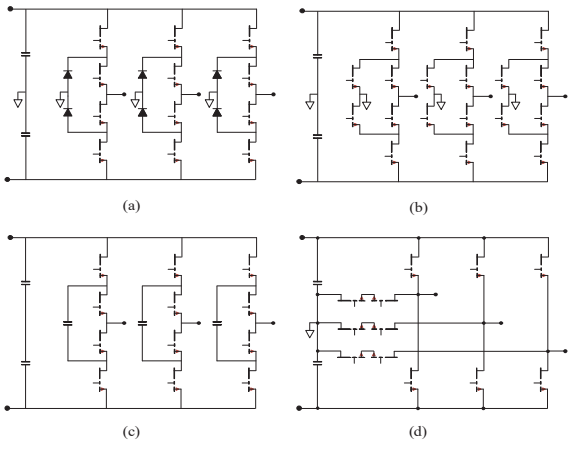
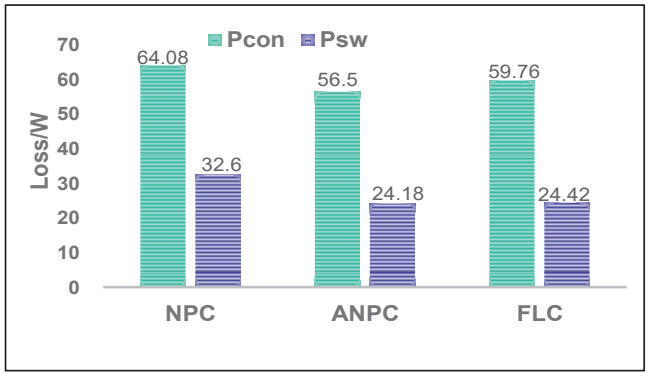


Fig. 1. MLI topologies: (a) NPC. (b) ANPC. (c) FLC. (d) T-type.

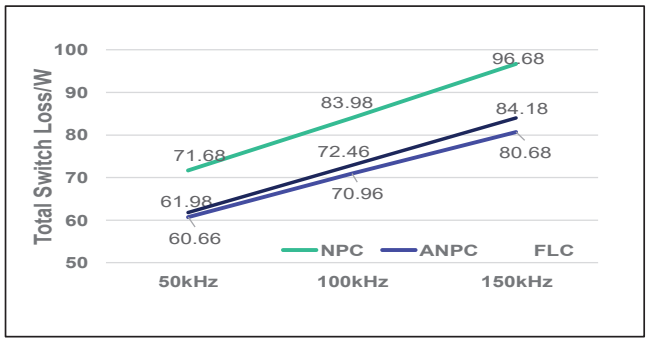
TABLE I. DEVICE QUANTITY OF DIFFERENT TOPOLOGIES

Type of MLI \ Number of Device	Switch	Diode	Isolation gate driver
NPC	12	6	10
ANPC	18	0	11
FLC	12	0	10
T-Type	12	0	7

By comparing the four listed topologies in Fig.1, considering the number of devices, FLC, ANPC and T-Type inverter have no power diodes which cause more power loss. T-Type inverter contains six switches that need to withstand 800 V DC voltage, so the selected 650 V GaN switch is not suitable in this topology. Comparing ANPC and FLC as seen in Fig. 2, under the same testing condition, these two topologies have similar power loss including conduction loss and switching loss based on the simulation and GS66516(the selected device) thermal model in PLECS. Noted that, for ANPC inverter switching pattern, the switch groups are working under different frequencies. Regarding thermal performance, the switches in FLC inverter with the same switching frequency have close temperature distribution which makes FLC inverter more stable than ANPC and cooling system more effective.



(a)



(b)

Figure. 1. GaN device loss comparison based on PLECS. Testing condition: Vdc=800V, fsw=150kHz, Pout=25kV (a): Conduction loss and switching loss compared of three different topologies. (b): Total switch loss changes with effective switching frequency (effective switching frequency: frequency of the output voltage before filter).

B. Simulation Results and Inverter Topologies Selection

Among all the topologies, T-Type inverter has switches handling DC bus voltage, which is beyond maximum device rated voltage, so the other three topologies are consider and compared here. From Fig. 2, majority of inverter switch losses

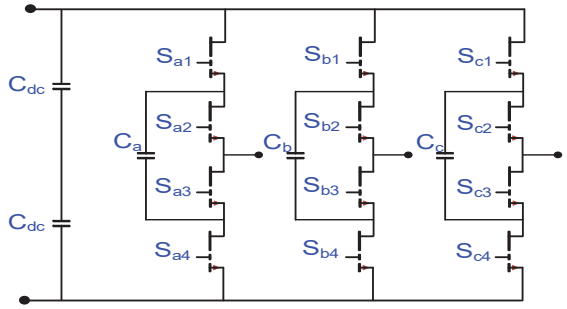


Figure. 3. FLC inverter topology.

are conduction loss. For NPC, its clamping diode voltage drop, and high switch conduction losses result in the lowest efficiency. Comparing ANPC with FLC, the clamped low-frequency switches in ANPC have lower losses than other switches in the same bridge but bring about uneven heat distribution. In FLC, effective output voltage frequency equals 2×fsw (in a 3-level FLC inverter), and all switches have similar power losses and similar heat distribution. In other words, to achieve the same effective switching frequency, the designed FLC switching frequency is 1/2 of ANPC switching frequency which reduces the switching loss, further reduces the size of passive components for filter design, and increases efficiency. Also because FLC has even loss distribution among all the devices, cooling method will be more effective compared with ANPC while the two topologies under the same effective switching frequency have close switch loss.

III. DESIGN OF FLC 3-PHASE 3-LEVEL INVERTER

In three voltage level FLC inverter, the flying capacitor (C_a, C_b, C_c)voltage is one-half of the DC voltage using phase-shifted PWM strategy to conduct switches. Flying capacitor voltage is controlled to be charged and discharged to keep balance through choosing the right combination of switch pattern: level "O" (O1, O2) as seen in Table II. Detailly, in phase A as seen in Fig. 3, switches S_{a1}-S_{a4} and S_{a2}-S_{a3} are two complementary pairs, each complementary pairs have 180° (Phase shift angle=360/(N-1), N=3: N represents inverter output voltage level) phase shift. In switch pattern Table II, 1 represents the switch is on, and 0 represents the off state. Complimentary switch pairs cannot be turned on simultaneously. As Fig. 5 shows, in the single phase PCB layout of the inverter, magnetic flux cancellation is used. In the half bridge of the complimentary switch pairs: S_{a1}-S_{a4}, S_{a2}-S_{a3}, by placing complementary devices on bottom layer symmetrically and placing a decoupling capacitor in the middle of the device positions on top layer, current direction flowing through each layer can be oppositely overlapped, resulting in two layers current magnetic flux cancellation and reducing parasitic inductances. Q3D simulation is done to quantitatively represent the low loop parasitic induction in each phase.

A. *Switching Pattern Explanation*

Table II. FLC SWITCHING PATTERN

Output Voltage	Switch State		Switch Sequence	
			S1	S2
Vdc/2	P		1	1
0	O	O1	1	0
		O2	0	1
-Vdc/2	N		0	0

Table II shows the switching combinations for output phase voltage V_o that is relative to the neutral point of N. A single-phase three-level FLC converter with inductive load is given in Fig. 4(a). The converter voltage modulation strategy is demonstrated in Fig. 4(b). Instantaneous voltage command V_{COM} is scanned by two opposite phase triangular wave carrier signals with 60Hz to define converter switching instants. Carrier waveform s1 is responsible for switching a complementary switch pair S1 and $\overline{S1}$ operation: when sawtooth carrier waveform s1 is above V_{COM}, S1 turns off and $\overline{S1}$ turns on, when V_{COM} is above carrier waveform s1, S1 turns on and $\overline{S1}$ turns off. Similarly, another pair S2 and $\overline{S2}$ movement depends on a comparison of V_{COM} and carrier waveform s2.

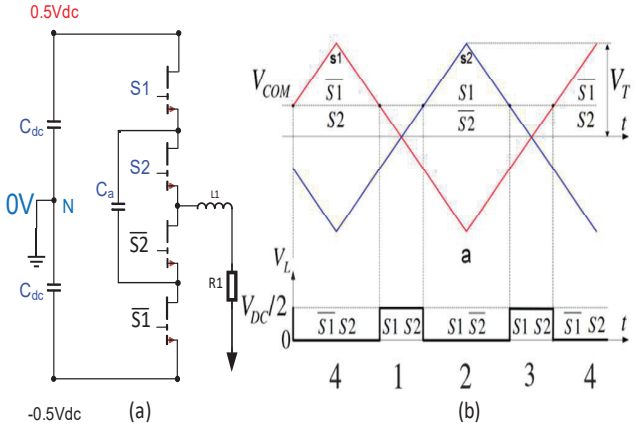


Figure. 4. Voltage modulation process (a): Single phase three-level FLC converter with RL-load. (b): Voltage modulation process and output voltage waveform with switching states.

For switching a complementary switch pair S1-$\overline{S1}$; S2-$\overline{S2}$, Fig. 4. (b) shows converter output voltage corresponding to different states: output voltage V_o=V_{DC}/2 when S1 and S2 are both conducted; output voltage V_o=-V_{DC}/2 when $\overline{S1}$ and $\overline{S2}$ are both conducted. As readily seen from Fig. 4(b), a switching period is comprised of four intervals. Assuming ideal switches, in intervals 1 and 3, FLC generates V_o=V_{DC}/2, noting that the capacitor is disconnected and keeps its initial voltage unchanged at these two intervals. Both intervals have the same duration:

$$\Delta T_1 = \Delta T_3 = \frac{D}{2} T_{PWM} \tag{1}$$

where $D = V_{COM}/V_T$. Intervals 2 and 4 are shown in Fig. 4(b), during intervals 2 and 4, FLC output voltage V_o=0 V and the flying capacitor is charging and discharging correspondingly to maintain the half of DC bus (0 V) level. Both interval:

$$\Delta T_2 = \Delta T_4 = \frac{(1-D)}{2} T_{PWM} \tag{2}$$

and

$$\Delta T_1 + \Delta T_2 + \Delta T_3 + \Delta T_4 = T_{PWM} \tag{3}$$

The right combination of these intervals and operation pattern guarantees that flying capacitor voltage remains constant at 0V when operation and three level output voltage (switch node voltage) is generated.

B. *Component Selection*

TABLE III. 3-PHASE 3-LEVEL INVERTER DESIGN SPECIFICATION

Design Specifications	Parameter
DC bus voltage	800 V
Effective PWM frequency	100 kHz
Fundamental frequency	60 Hz
Load	9.2 Ohm
Power rating	25 kW
Power density	25 kW/L
Cooling method	Air Cooling

The values of the flying capacitors are designed based on the allowed voltage ripple (switch node voltage level N=3). For the FLC converters, the worst-case peak-to-peak voltage ripple on capacitors needs to be below Vdc/ (N −1) by design. Based on Fig 4. (b) the worst case in charge of the flying capacitors (ΔQ_c) can then occur at the longest charging and discharging time of the capacitor when switching state interval 2 or interval 4 reaches 0.5·T_{PWM}=1/[fs(N − 1)], thus,

$$\Delta Q_c = i_{load} \Delta t = i_{load} \frac{1}{f_{sw}(N-1)} \tag{4}$$

Where N=3, the peak voltage ripple on a given capacitor ($V_{ripple,pk}$) is defined as a fraction (α_{cv}) of switch node voltage V_{sw}, the peak-to-peak flying capacitor voltage ripple (ΔV_c) on the capacitor can then be expressed as

$$\Delta V_c = 2 \cdot \alpha_{cv} \frac{V_{dc}}{N-1} \tag{5}$$

Combining (4) and (5), the capacitance required at each node for a given load current, as a function of capacitor voltage ripple is found to be:

$$C = \frac{\Delta Q_c}{\Delta V_c} = \frac{i_{load}}{2 \cdot \alpha_{cv} \cdot V_{dc} \cdot f_{sw}} \tag{6}$$

where f_{sw}=50 kHz. If we select the max voltage ripple, α_{cv} = 7.5 % of V_{dc}, then the minimal $8.9\,\mu F$ flying capacitor is required. A ceramic capacitor (B58035U5106M001) is selected for the flying capacitor, which has the feature of high ripple current capability, high capacitance density, increasing capacitance with DC bias up to operating at high voltage, no limitation of dv/dt, and low equivalent serial inductance (ESL) and resistance (ESR).

TABLE IV. HARDWARE PROTOTYPE COMPONENT LIST

Component	Part Number	Parameter
Flying Capacitor	TDk-B58035U5106M001	10 μF
GaN Switch	GaN System-GS66516T	650 V,25 mΩ
Switch gate driver	Diodes- ZXGD3005E6	10 A, 25V
Power stage GD	Skyworks-SI8271AB-IS	

Isolated power supply	Diodes-NTE1209MC	
Decoupling capacitor	KEMET-C1210C103KDRAC7800	10000 pF

C.Power stage Design for Lower Parasitic Inductance

In high-frequency applications, one of the most important aspects of board PCB layout is to accurately find high slew rate current (high di/dt) loops, while keeping an eye out for parasitic or stray inductances caused by the layout. This type of inductor can produce excessive noise and ringing, resulting in overshot and ground bounces. Here in the design, a magnetic flux current cancellation method is used in the power stage of the PCB to reduce power loop inductance, as seen in Fig. 5. By placing the two series-connected switches S_1 and S_2 in a half-bridge at the

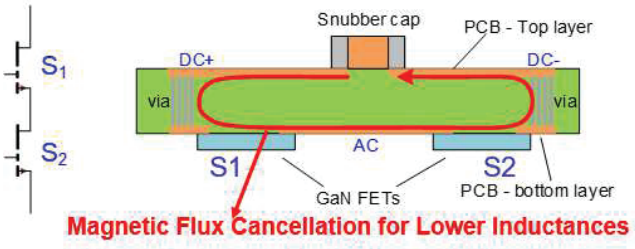


Fig. 5. Magnetic flux cancellation design for single-phase power loop.

PCB bottom layer, the flying capacitors at the middle of the switches on top and using vias to conduct DC+ and DC- nets with the switches drain and source, high-frequency current flows in opposite directions on two adjacent PCB layers, the magnetic flux generated by two current flows will cancel each other. This magnetic flux-canceling effect can lower the parasitic inductance. Notably, to further evaluate this method to see how much parasitic inductance it can reduce in one single-phase power loop of FLC inverter, a Q3D analysis is conducted with results being shown in Fig. 6. In Fig. 6, two half bridge switch pairs S1-$\overline{S1}$; S2-$\overline{S2}$ (seen in Fig. 4(a)) are circled with the red line, the loop inductance of these two pairs decreased, calculated as 6.8 nH and 7.3 nH.

In the hardware prototype design, as Fig. 7 shows, the three-phase three-level FLC inverter hardware prototype has three major parts: control stage (gate driver boards), power stage, and heatsink with fans. The estimated power density of the designed flying capacitor 3-level inverter can reach 15 kW/L, with its

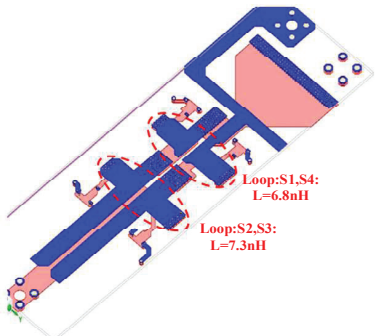


Fig. 6. Ansys Q3D parasitic inductances extraction of single phase (bottom layer view).

dimensions of 127 mm width×140 mm length×92 mm height. Looking into the prototype of the control stage, for each phase, the output signal and biased voltage generated by four gate drivers with four isolated power supplies are vertically connected to the power stage to control four switches by the non-isolated gate driver by the side of GaN device. In each phase of the power stage, two 10 μF ceramic capacitors in series and 0.01 μF decoupling capacitors are across the DC link. The same 500 V,10 μF capacitor used as

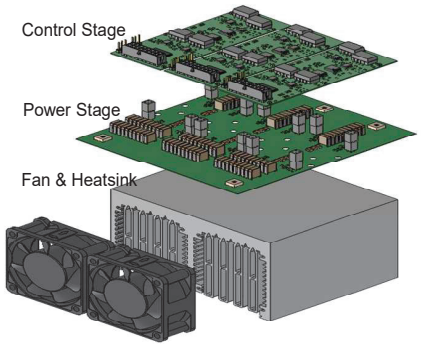


Fig. 7. 25kW Inverter hardware 3D prototype.

flying capacitor is connected parallel with switch S_{a2} and switch S_{a3} in Fig. 3 which is placed in the center of four switches to realize current flux cancellation and further reduce loop parasitic inductance. The air-cooled method is used in the thermal design. Two fans are supplied with 12 V volts from gate driver boards.

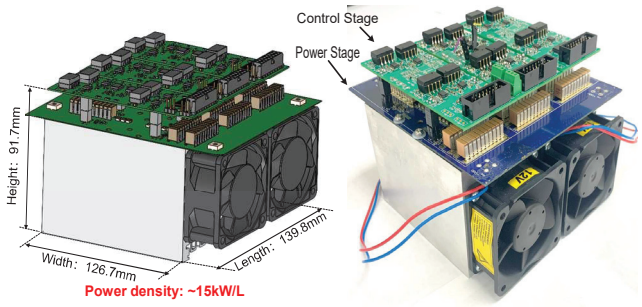


Fig. 8. SOLIDWORKS inverter prototype and hardware prototype.

IV. Experimental Analysis

To validate the basic function of the inverter hardware prototype, the 800 V DC bus voltage test is done, Fig. 9. shows no load testing result. The output voltage of each has three clear voltage levels: 0 V, 400 V, and 800 V (level P). Furthermore, a 3.3 kW power capability testing is done with 800 V DC bus voltage and 68 Ω resistor load for each phase. With resistive load, as seen in Fig. 10(a), a seven-level load current can be seen with Y-load connection. The zoomed-in waveform in Fig. 10(b) shows stable switch node voltage without obvious overshot at turning on and off transient.

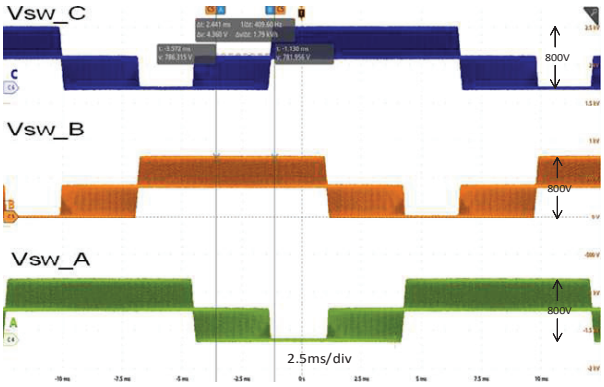
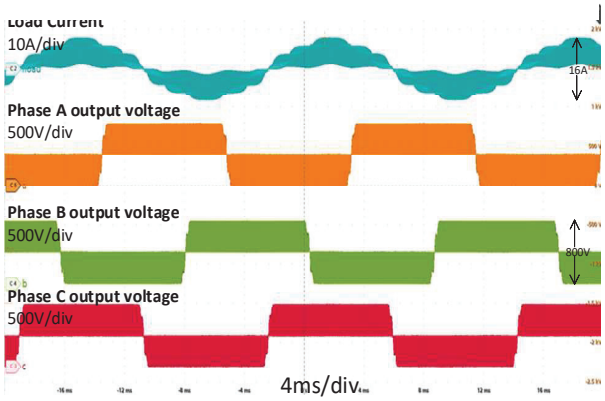
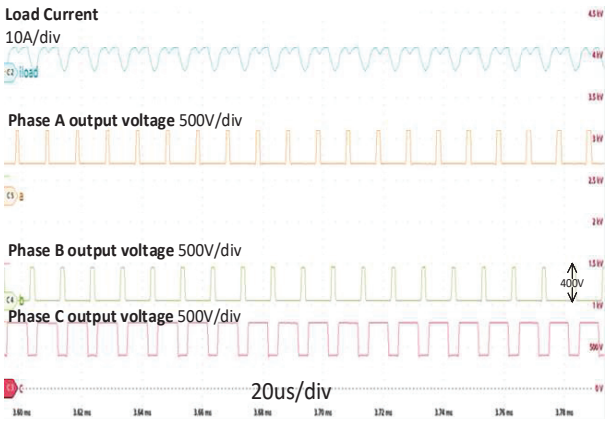


Fig. 9. Switch node voltage of inverter with no load.
Testing condition: DC voltage=800 V, carrier frequency: f_c=50 kHz, modulation frequency: f_{sin}=60 Hz, deadtime: t_d=0.8us.



(a)



(b)

Fig. 10. Three phase switch node voltage waveforms with resistive load: (a): zoomed out with 4 ms/div (b): zoomed in with 20 us/div
Test conditions: Vdc=800 V, power rating=3400 W
Load R=68 Ohm, I_{load_rms}=4.09 A, fc=100 kHz.

V. Conclusion and Future Work

This paper demonstrates a 25 kVA multilevel inverter building block with scalability in detail. Efficiency evaluation, loss comparison, and heat distribution analysis help to determine choosing flying capacitor inverter among different multilevel inverter topologies. The operation method (PWM control strategy) and specific parts in FLC inverter circuit design (PCB layout) are also explained. To achieve the design goal, and operate at high switch speed at 150 kHz, components selection is conducted and shown including flying capacitor and GaN switch. The gate driver circuit design is presented to reduce the gate loop inductances and turn-on and turn-off losses. The power stage with reduced parasitic inductance is demonstrated and verified in Q3D. Experimental results of the hardware prototype working under 800 V DC no load condition and 3.3 kW resistive load condition are presented. In the future, to approach up to 25 kVA power rating, a higher power rating load test will be conducted, efficiency will be calculated, and inverter performance will be improved.

References

[1] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert and B. J. Blalock, "Methodology for Wide Band-Gap Device Dynamic Characterization," in IEEE Transactions on Power Electronics, vol. 32, no. 12, pp. 9307-9318.

[2] M. Jahnes, L. Zhou, Y. Fahmy and M. Preindl, "A Peak 1.2MHz, >99.5% Efficiency, and >10kW/L Power Density Soft-Switched Inverter for EV Fast Charging Applications," in IEEE Transactions on Transportation Electrification, doi: 10.1109/TTE.2023.3330997.

[3] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," in IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724-738.

[4] J. A. Anderson, L. Schrittwieser, M. Leibl and J. W. Kolar, "Multi-level topology evaluation for ultra-efficient three-phase inverters," 2017 IEEE International Telecommunications Energy Conference (INTELEC), Broadbeach, QLD, Australia, 2017, pp. 456-463.

[5] Rodriguez J, Lai S, Peng FZ. Multilevel inverters: a survey of topologies, control and applications. IEEE Trans Power Electron 2002;49:724–38.

[6] Z. Ye, Y. Lei, Z. Liao and R. C. N. Pilawa-Podgurski, "Investigation of Capacitor Voltage Balancing in Practical Implementations of Flying Capacitor Multilevel Converters," in IEEE Transactions on Power Electronics, vol. 37, no. 3, pp. 2921-2935, March 2022.

[7] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference, Toledo, Spain, 1992, pp. 397-403 vol.1, doi: 10.1109/PESC.1992.254717.

[8] N. Pallo, T. Foulkes, T. Modeer, S. Coday and R. Pilawa-Podgurski, "Power-dense multilevel inverter module using interleaved GaN-based phases for electric aircraft propulsion," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 2018, pp. 1656-1661, doi: 10.1109/APEC.2018.8341239.

[9] S. Bernet, "Recent Developments of High Power Converters for Industry and Traction Applications," IEEE Transactions on Power Electronics, 2000, vol. 15, no. 6, pp. 1102- 1117.

[10] I. Yoscovich, T. Glovinsky, G. Sella, and Y. Galin, "Multi-Level Inverter with Flying Capacitor Topology," US Patent 9,318,974, 2016

[11] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2155-2163, May 2014, doi: 10.1109/TPEL.2013.2268900.