High Temperature Characterization and Degradation Test of a Cascode Gallium Nitride Field Effect Transistor

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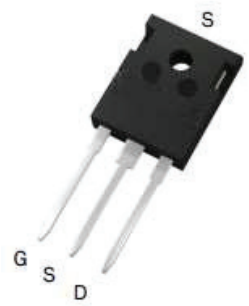
***Abstract*— Gallium Nitride (GaN) is a wide bandgap semiconductor material known for its exceptional performance in high-temperature and high-voltage environments. This makes GaN a preferred material for field-effect transistors (FETs) used in demanding applications. While GaN FETs are theoretically capable of operating at temperatures exceeding 200°C, practical applications often limit their maximum junction temperature to around 150°C, primarily due to packaging limitations, such as those associated with the standard TO-247 package. This paper presents an experimental analysis of the high-temperature performance of GaN FETs, focusing on how elevated temperatures influence various operational parameters. Key areas of investigation include the impact on output characteristics, on-resistance (R_{dson}), threshold voltage (V_{th}), transfer characteristics, and gate leakage currents. Furthermore, the study examines potential degradation effects that may result from prolonged operation at elevated temperatures. The insights gained from this study are crucial for advancing the deployment of GaN FETs in applications that demand robust performance under extreme conditions, including automotive, aerospace, and industrial power systems. Ultimately, the findings will contribute to the development of more reliable and efficient power electronics, pushing the boundaries of GaN technology.**

Keywords— Gallium Nitride, wide bandgap, static characteristics, high temperature, TO-247 package

I. Introduction

Wide bandgap (WBG) power devices, such as GaN FETs, are increasingly being adopted in applications like motor drives, renewable energy systems, energy storage, low temperature application and more, thanks to their superior performance compared to traditional silicon (Si) counterparts [1-3]. Over time, the performance of GaN devices has seen significant advancements [4]. Due to its high electron mobility, GaN operates optimally at high frequencies, making it a reliable alternative to SiC devices. Additionally, the wide bandgap of GaN enables higher voltage applications than Si devices. GaN's high thermal conductivity also supports effective thermal management, allowing the devices to operate at elevated temperatures [5]. These characteristics make GaN FETs particularly suited for applications requiring high efficiency and compact form factors, such as fast-charging power adapters, data centers [6], and electric vehicle [7-8]. The ability to handle higher power densities with lower losses further enhances the appeal of GaN technology in next-generation power systems. As industries continue to demand more efficient and reliable power solutions, the role of GaN devices is expected to expand, driving further innovations in power electronics design and application. A conventional TO-247 package and the device structure is shown in Fig. 1.



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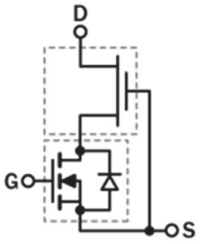

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Fig. 1: (a) Conventional TO-247 package, (b) Device structure

As GaN FET fabrication and application technologies advance, these devices are emerging as leading candidates for next-generation power semiconductor applications [9-10]. High-temperature operation is one of the most promising areas for GaN devices, prompting extensive research to address reliability concerns associated with GaN FETs. This focus on reliability is crucial, as the ability of GaN devices to maintain performance under extreme conditions will determine their viability in critical applications such as electric vehicles, aerospace systems, and industrial power conversion. The ongoing development of packaging solutions and thermal management strategies will further enhance the durability and efficiency of GaN FETs, solidifying their role in the future of power electronics.

In this paper, the characterization of a GaN FET arranged in a cascode configuration with a silicon MOSFET and a GaN HEMT for high temperature is investigated. The GaN FET was subjected to high temperatures by externally heating the device, given that its self-heating can easily elevate junction temperatures to 250°C. The device's typical characteristics

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were tested and compared across temperatures up to 250°C. This research provides a foundation for designing and developing a GaN FET power module capable of reliable operation at 250°C. The preliminary study involved testing GaN FET samples at 250°C to observe characteristic trends and identify potential degradation at high temperatures. Additionally, the standard TO-247 package was tested to establish an industry benchmark.

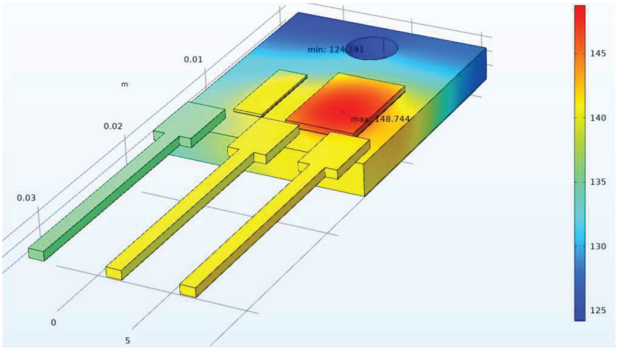
II. Analysis of Thermal Aged GaN FET

Despite their superior operational characteristics, the long-term reliability of cascode GaN devices has raised significant concerns. Extensive research has been conducted to assess their long-term reliability, with power cycling tests (PCT) [11-13] being commonly employed to simulate real-world operating conditions. The failure mechanisms of cascode GaN devices can generally be categorized into two types: chip-level and package-level degradation. Chip-level degradation primarily occurs in the gate region of the GaN HEMT, where internal and nearby defects formed during long-term stress testing can affect the device's electrical characteristics [11]. Package-level degradation, on the other hand, is often linked to issues in the solder layer and bond wires, which can impact the thermal and electrical performance of the device. However, there is limited research that comprehensively analyzes the relationship between chip-level and package-level degradation in cascode GaN devices under prolonged power cycling or thermal stress.

In cascode GaN devices, two primary heat sources are present: the GaN HEMT and the Si MOSFET. These devices are deliberately overlapped in the stacked-die package to minimize package-related parasitics. However, this design complicates heat dissipation compared to conventional configurations where each die is placed directly on the base plate. Additionally, the involvement of both devices within the same package can make it challenging to accurately identify the source of performance issues. The increased thermal stress from the overlapping structure can lead to higher junction temperatures as shown in Fig. 2, which may accelerate device degradation and reduce overall reliability. Parameters in Table I are used to develop the FEA model. From the figure it can be observed that the stacked cascode arrangement has a higher junction temperature (>=4.5°C) than conventional arrangement. Impact of junction temperature difference between vertical and side cascode arrangement is shown in Fig. 3 for different heat transfer coefficient (forced air cooling). From the figure it is observed that there is approximate junction temperature difference of 2.3 °C between the structures, with maximum difference of 4.3 °C. Furthermore, the thermal interactions between the GaN HEMT and Si MOSFET must be carefully managed to ensure efficient operation. Therefore, a comprehensive understanding of the thermal behavior and long-term reliability of these devices is crucial for optimizing their performance in real-world applications.

Table I: Material Parameters used in the FEA model

Material	Thermal Conductivity W/(m·K)	Density (kg/m³)	Heat Capacity (J/(kg·K))
GaN	230	6095	431
Silicon	130	2329	700
Copper	398	385	8600
AlN	310	3320	780
Silver	420	8600	235
GaN: 50 W Silicon: 15W Heat Transfer Coefficient: 2500 W/ (m².K)			



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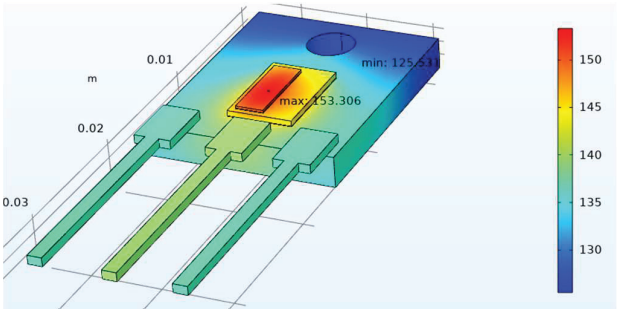

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Fig. 2: Steady State Junction Temperature of Cascode GaN FET: (a) Side Structure, (b) Vertical Structure

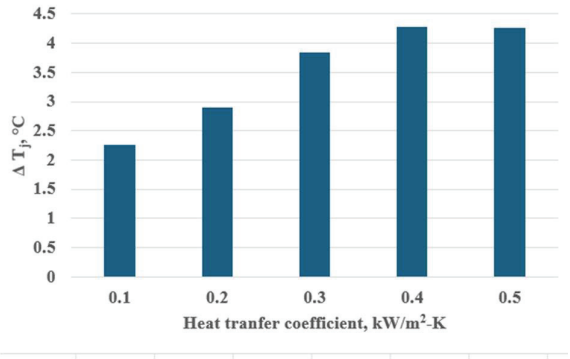


Fig. 3: Steady State Junction Temperature difference between vertical and side Cascode GaN FET for different heat transfer coefficient (forced air cooling)

Current research predominantly focuses on applying high electric fields, elevated temperatures, and high drain biases directly to devices. These stress factors can lead to issues such

as current collapse [14-15], degradation of drain current, threshold voltage shifts, and increased gate leakage current. To simulate real-life operating conditions, GaN devices are subjected to power cycling or thermal aging. During repeated power cycles, the junction temperature rises, contributing to the degradation of GaN FETs. This thermal aging manifests in changes to parameters such as on-state resistance, drain-to-source leakage current, gate-to-source leakage current, and threshold voltage.

As the device undergoes continuous thermal cycling, the material properties of GaN begin to degrade, impacting the device's long-term reliability and performance. Prolonged exposure to high junction temperatures accelerates these degradation mechanisms, potentially leading to early device failure. Table II illustrates the typical changes in GaN FETs, highlighting how critical these factors are in determining the operational lifetime and efficiency of power electronics systems utilizing GaN technology.

Table II: GaN FET Characteristics after PCT

	Before testing	After testing (27.5 k cycles)
Gate Leakage Current	10^{-11} A	10^{-3} A
Drain Leakage Current	10^{-4} A	10^{-3} A
Gate Threshold Voltage	2 V	0.1 V
On State Resistance	0.044 Ω	0.054 Ω

III. High Temprature Characteristics of GaN FET

A 650 V GaN FET, was used to define the high-temperature behavior of GaN devices. The device's maximum junction temperature was set at 250°C using a hotplate, as illustrated in Fig. 4. The static characteristics of the GaN device were analyzed using a curve tracer, with the device connected to the curve tracer while mounted on the hotplate. The test setup is depicted in Fig. 5. The experiments conducted on the device included measurements of leakage current, on-resistance, output characteristics, transfer characteristics, threshold voltage, and gate-to-source leakage current. To ensure accurate heating of the device, a thermal camera was employed to capture thermal images of the GaN device while the hotplate was in use. The GaN device was heated to 150°C, 225°C, and 250°C using the hotplate, with the corresponding thermal images presented in Fig. 6. These images confirm that the desired temperatures for the GaN FET were successfully achieved using the hotplate.

Fig. 4: GaN FET attachment with hotplate

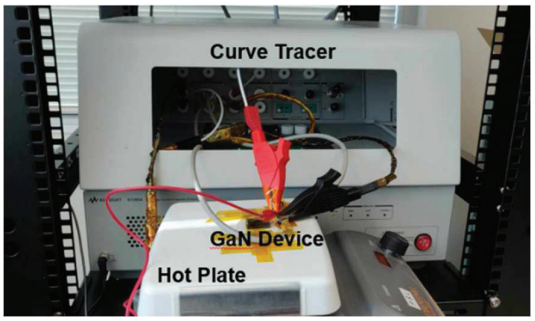
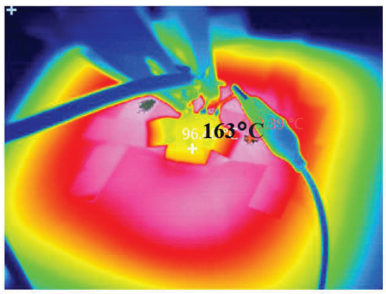


Fig. 5: Experimental setup of GaN FET characterization at 250°C



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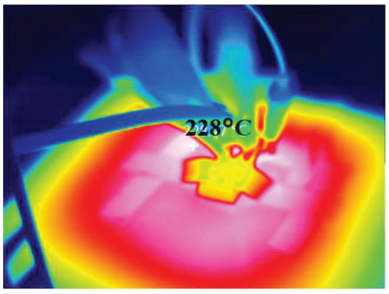

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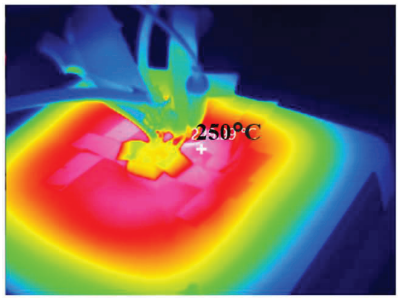

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Fig. 6: Thermal imaging of GaN FET a) 150°C, b) 225°C, c) 250°C

The on-resistance characteristics of the GaN FET are displayed in Fig. 7, revealing a positive temperature coefficient from the experimental results. This behavior suggests that the device's on-resistance increases with temperature, which could influence its efficiency in power conversion applications. As the on-resistance rises, it leads to higher conduction losses, reducing the overall efficiency of the system. This is particularly critical in high-power applications, where even small increases in resistance can result in significant energy losses. Furthermore, the increase

in on-resistance at elevated temperatures may also impact the thermal management of the device, necessitating more robust cooling solutions or design adjustments to maintain optimal performance. Understanding this temperature-dependent behavior is crucial for engineers when designing power electronics that need to operate reliably under varying thermal conditions.

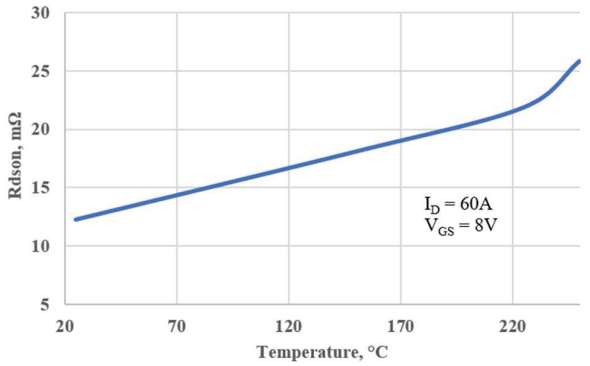
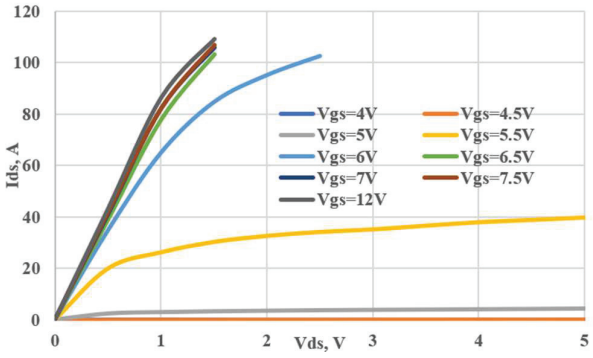


Fig. 7: R_{dson} of GaN FET at different temperatures

Fig. 8 presents the output characteristics of the device across a temperature range of 25°C to 250°C, with Vgs set between 5.5 V and 12 V. The test results closely matched the pattern provided in the datasheet, demonstrating the consistency of the device's performance with its specified parameters. This consistency is crucial for ensuring predictable behavior in practical applications, where adherence to datasheet specifications is vital for system reliability. Transfer characteristics of the module are shown in Fig. 9, indicating that the drain-source current (Ids) decreases with increasing temperature. This trend highlights the thermal sensitivity of the device, which could impact its performance in high-temperature environments. As Ids decrease, the device may experience reduced current handling capability, which could affect the overall power delivery and efficiency in circuits where the GaN FET is deployed. Understanding these temperature-induced variations is essential for optimizing the device's operation in varying thermal environments, ensuring that it performs reliably across a broad range of temperatures. These insights are particularly valuable for applications in industries where devices are exposed to extreme temperature fluctuations, such as automotive or aerospace sectors.



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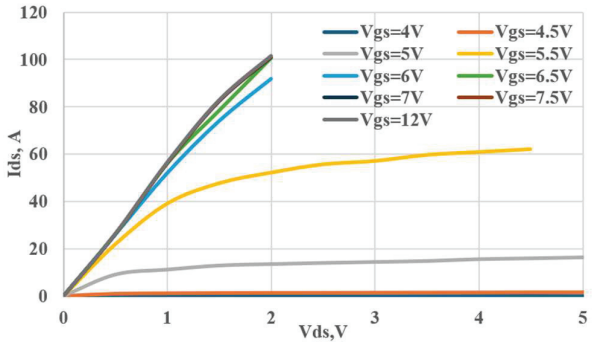

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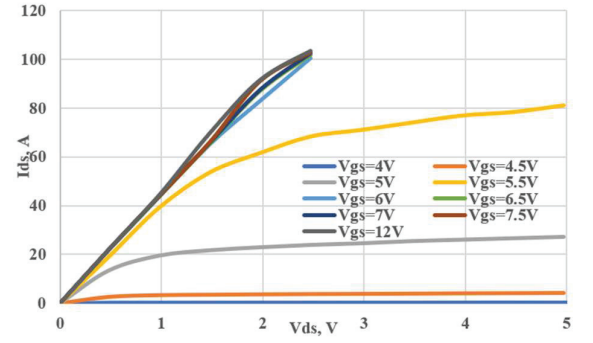

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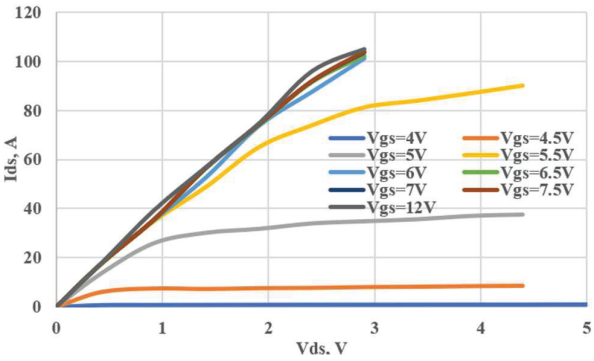

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Fig. 8: Output Characteristics of GaN FET a) 25°C, b) 150°C, c) 225°C, d)250°C

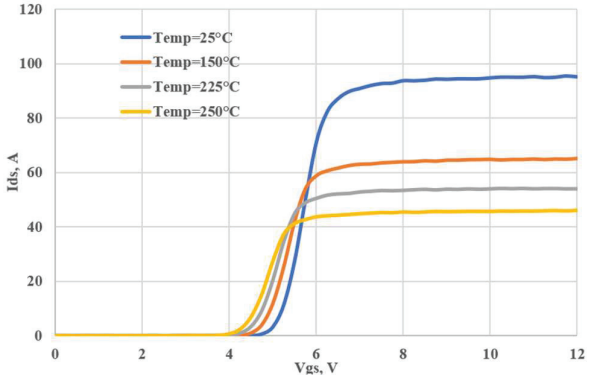

Fig. 9: Transfer Characteristics of GaN FET up to 250 °C

Finally, the threshold voltage of the GaN module, as shown in Fig. 10, decreases at higher temperatures. This decrease is attributed to the reduction in the bandgap of the device, which facilitates easier carrier (electron and hole)

transition from source to channel. Knowing the temperature-dependent shifts in threshold voltage is essential for the precise design and control of GaN-based circuits, especially in high-power and high-frequency applications.

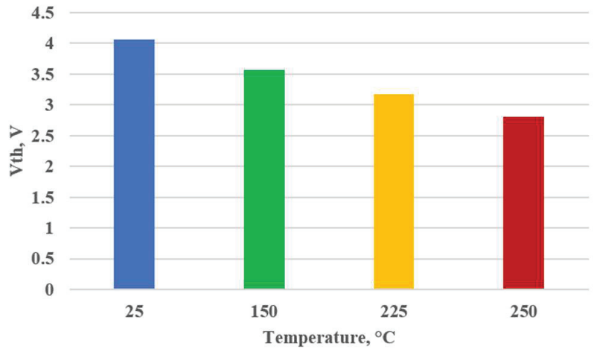

Fig. 10: Threshold Voltage Characteristics of GaN FET up to 250 °C

IV. Performanec Degradation in High Temperature Operation

Post high-temperature operation, the device exhibited noticeable degradation. After high temperature testing, the R_{dson} of the device increased by 10%, under accumulation of thermal stress as shown in Fig. 11. This degradation of R_{dson} adds to the increase in conduction loss of the device. The increase in R_{dson} accelerates the rise of junction temperature of the device, which brings thermal runway earlier.

In a cascode GaN FET, the R_{dson} value did not change that much (10% increase). This suggests that the change in on-state resistance is not attributed to degradation of the channel resistance. Instead, it is likely that the increase in on-resistance is primarily due to degradation related to the device packaging [11]. Factors such as bond wire degradation, solder fatigue, or thermal interface material breakdown could be contributing to the observed increase.

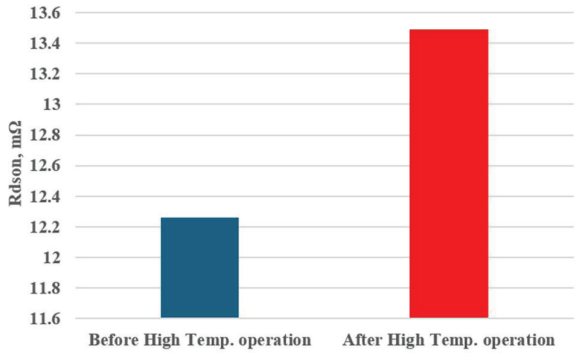

Fig. 11: R_{dson} comparison after high temperature operation

This degradation is further corroborated by the data presented in Fig. 12, where the gate-to-source leakage current (I_{GSS}) increased to 9 µA at a gate voltage of 30 V, indicating significant wear at the gate oxide interface of the GaN FET. The increase in I_{GSS} suggests potential breakdown mechanisms at the microscopic level, such as defects or traps forming at the interface, which could compromise long-term device stability and performance.

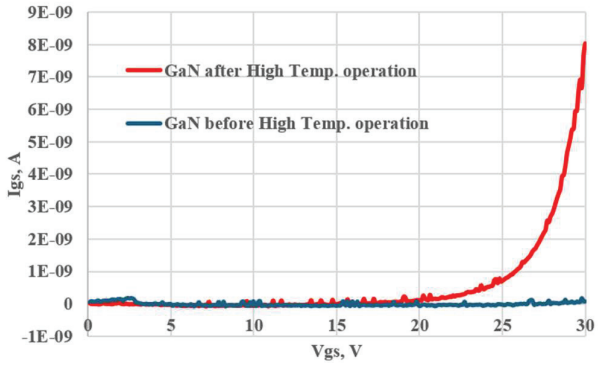

Fig. 12: I_{GS} comparison after high temperature operation

V. Conclusion

GaN FETs are investigated for the development of reliable power modules capable of operating at high temperatures. This paper presents the characterization of a cascode GaN FET for high-temperature applications, with testing conducted at temperatures up to 250°C. The study highlights the device's performance characteristics under these conditions and examines potential causes of degradation. Notably, degradation was observed in the form of an increased R_{dson} value following high-temperature operation, which is attributed to device packaging interface. The results present the importance of understanding the thermal limits of GaN FETs in demanding environments, particularly for applications in industries such as automotive, aerospace, and renewable energy, where devices are often exposed to extreme temperatures. Additionally, the findings suggest that optimizing gate oxide materials and interface design could be crucial in enhancing the longevity and reliability of GaN-based power modules.

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