# Compact GaN-Based 25kW, 480V Three-Level Active Front End Rectifier

Mohammad Hassan Adeli, Erkan Deniz, Necmi Altin, Saban Ozdemir, and Adel Nasiri
Department of Electrical Engineering, University of South Carolina, Columbia, SC, USA
edeniz@mailbox.sc.edu; madeli@email.sc.edu; altin@sc.edu; sozdemir@mailbox.sc.edu; nasiri@mailbox.sc.edu

2024 IEEE Sixth International Conference on DC Microgrids (ICDCM) | 979-8-3503-6363-0/24/$31.00 ©2024 IEEE | DOI: 10.1109/ICDCM60322.2024.10665131

***Abstract*—Interface units are needed to connect DC microgrids to the AC grid. This paper presents a compact and high-efficiency 25kW 480V Gallium Nitride (GaN) based bidirectional Three-Level Active-Neutral-Point-Clamped (3L-ANPC) converter for DC microgrids. The entire system, including the FPGA, DC-link capacitors, switching devices in the topology, and AC grid inductive filters, is integrated onto a single board. The 3L-ANPC topology provides balanced distribution of power losses and voltage stress among the switches. A 200kHz switching frequency is used for the GaN devices to reduce the size of passive elements. A PCB-based DC busbar is designed to minimize inductance, ensure a compact size, and reduce parasitic capacitances. Additionally, PCB-based inductors are designed to minimize size and tolerance on inductance value and reduce magnetic flux pollution in the converter. System control is performed using an Intel ultra-high-speed FPGA. Simulation and experimental results validate the electrical and thermal performance of the proposed design.**

**Keywords—DC Microgrids, active front end; compact design; high efficiency; GaN FETs; 3L-ANPC; PCB-based planar inductor.**

## I. Introduction

In recent years, there has been growing interest in industrial applications towards low-voltage DC microgrids (DCMG), owing to the increase in loads fed by DC voltage in power systems and the desire to increase power conversion efficiency by reducing the number of power conversion stages. Interfaces to the AC grid are crucial to provide bidirectional power flow [1]. An Active Front-End (AFE) rectifier is one of the most preferred interfaces for DCMG applications with their superior features such as adjustable dc-bus voltage, low harmonic distortion of source current, bidirectional power flow, and nearly unity power factor [2]. It is obvious that if the power electronic converters, which are the basic building blocks of these industrial applications, have a high efficiency and compact structure, the efficiency of the entire system will increase significantly, and their dimensions will be reduced [3], [4]. Therefore, there is a growing interest in improving the efficiency, reliability, and flexibility of power converters and reducing their cost and size.

Over the last decade, there has been a migration of power converter device technologies from Si-based IGBTs to Wide-Band Gap (WBG) devices such as silicon carbide (SiC) and gallium nitride (GaN) devices to increase efficiency and power density. Today, 3.3kV SiC MOSFETs are commercially

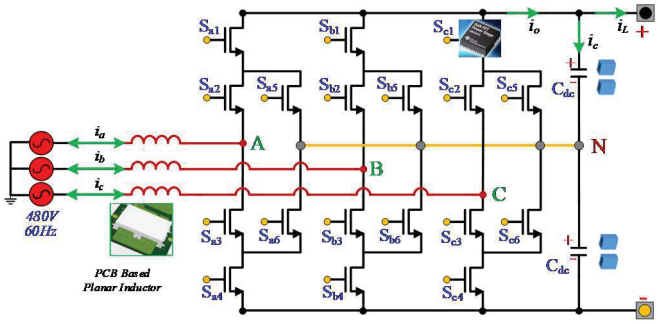



Fig. 1. Circuit of GaN-based 3L-ANPC active front end rectifier.

available, and higher voltage devices are on the horizon [5]. On the other hand, the availability of GaN devices has been at low voltages but much higher frequency. Currently, commercially available GaN devices reach up to 1200V, making them ideal for grid-connected applications. Recently, GaN devices have been preferred in 380V~480VAC applications to create more efficient and compact systems because of their superior breakdown capability, higher electron density, and speed. GaN devices promise lower conduction and switching loss, higher switching frequency, higher operating temperature, and higher reliability [6]. Also, as GaN has no body diode, there is no reverse recovery charge and thus reverse recovery loss. GaN MOSFETs can offer about four times faster dv/dt during turn-on and two times faster dv/dt during turn-off. This significantly reduces switching loss to enable higher switching frequencies. This higher frequency operation allows GaN-based converters to be significantly more compact, as they require smaller passive components and cooling systems.

In recent years, multi-level topologies have gained significant attention for high-power and high-voltage applications [7], [8]. These topologies allow the use of lower voltage, higher current-rated switching devices while achieving high voltage operation. By increasing the number of waveform steps and reducing voltage stress across the switches, they improve the output voltage waveform quality of a voltage source inverter. A low dv/dt results from reduced voltage stress, which in turn minimizes Electromagnetic Interference (EMI) issues. However, as the number of levels increases, increase number of switches increases control complexity [7], [8]. For this reason, 3-level topologies with less switches are widely preferred over other multi-level converters in 380-480V grid-connected applications and motor drivers. Among three-level

topologies, Three-Level Active-Neutral-Point-Clamped (3L-ANPC) converter is widely preferred due to its ability to ensure smoother operation of control systems and efficient power conversion. 3L-ANPC has two current paths for the output "zero" level, allowing for a balanced distribution of semiconductor power losses among the switches. Moreover, it maintains an acceptable level of electromagnetic compatibility (EMC). Besides, a comprehensive review of published works and developed products reveals the absence of state-of-the-art high-power and high-voltage GaN-based converter for connection directly to the 480V grid.

Space Vector PWM (SVPWM) signals at 200kHz are generated by using an Intel ultra-high-speed FPGA. The performance of the proposed system is validated with MATLAB/Simulink simulations and experimental studies.

In this work, a compact GaN-based 25kW, 480V 3L-ANPC active rectifier is designed and implemented. To achieve a compact size, a PCB-based DC busbar and PCB-based inductors are designed to minimize parasitic capacitances and inductor tolerance. This approach also enables automatic manufacturing of the system. The overall converter is a single, compact board system with the size of 13×12×4 inches, making it a compact solution. 650V, 26mΩ GaN FETs with a minimal switching loss are used to build 3L-ANPC rectifier connected to a 480V AC grid as shown in Fig.1. Space Vector Pulse Width Modulation (SVPWM) signals are generated at a frequency of 200 kHz by leveraging the capabilities of an Intel ultra-high-speed Field-Programmable Gate Array (FPGA). The performance of the proposed system is comprehensively validated through a combination of MATLAB/Simulink simulations and experimental studies.

## II. Design of GaN-Based 3-Level AFE Rectifier

In this study, a 25kW 3L-ANPC bidirectional converter, as shown in Fig. 1, is designed to operate at a 200kHz switching frequency to minimize the size of all passive components. The 3L-ANPC converter was introduced to address the uneven loss distribution in the 3L-NPC converter and to enhance the maximum output power. As illustrated in Fig. 1, the 3L-ANPC topology comprises six switches per phase. GaN switches are used to operate at high switching frequencies, significantly reducing both conduction and switching power losses in the proposed converter. The $S_{x5}$ and $S_{x6}$ switches alleviate the voltage stress on the middle switches, $S_{x2}$ and $S_{x3}$, which bear the highest stress in managing the DC bus voltage. Employing ANPC and increasing the number of waveform steps reduces the voltage across the switches, leading to lower dv/dt and mitigating EMI issues. In a multi-level converter, various switching techniques can be utilized to achieve goals such as reducing losses, mitigating EMI, and ensuring an even distribution of losses among the switches. In a 3L-NPC structure, employing a single zero switching state (O) directly impacts the distribution of losses among the switches. Active clamp switches enhance the converter's flexibility by managing PWM strategies and providing zero-voltage level in two distinct ways, regardless of the load current direction. In this work, a single zero state PWM technique is implemented to create a short commutation loop, significantly reducing the impact of large stray inductance associated with longer commutation loops and minimizing overall losses compared to other strategies [9]. The subsequent section provides a detailed discussion of this technique.

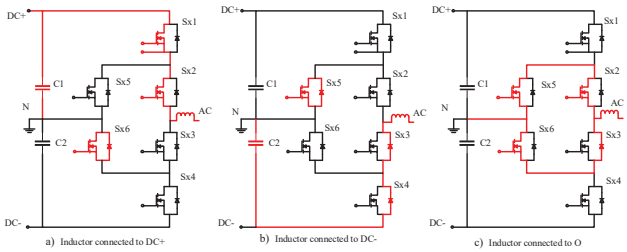



Fig. 2. Commutation loop when $i > 0$ for a) connecting to $+V_{DC}$, b) connecting to $-V_{DC}$, c) connecting to neutral.

### A. Modulation and Switching Pattern

SVPWM for three-level converters is among the most advanced and promising modulation techniques for three-phase systems. SVPWM uniquely determines the switching sequence of the switches, optimizing performance in several ways. Compared to traditional PWM, SVPWM generates fewer harmonics, causes lower switching losses, utilizes the DC supply voltage more efficiently, and is highly compatible with digital controllers. One of the key advantages of SVPWM over sinusoidal PWM is its superior voltage utilization. SVPWM has a modulation range that is 15% higher, achieving a voltage utilization factor of $2/\sqrt{3}$ [10]. This results in improved efficiency and performance, making it a preferred choice for high-performance applications. The three-level SVPWM technique is derived from the two-level SVPWM method, but it introduces significantly more complexity. This complexity arises from the increased number of converter switches and the challenge of maintaining neutral point voltage self-balancing. The additional switches provide more flexibility and control, but they also require more sophisticated algorithms to manage the switching states effectively. In this work, a SVPWM technique with a single zero state to create a short commutation path loop is employed. Using this method, two commutation groups are utilized: one with switches $S_{x1}$, $S_{x3}$, and $S_{x5}$, and the other with $S_{x2}$, $S_{x4}$, and $S_{x3}$. These two groups alternate between line frequency and switching frequency. This technique achieves a more balanced distribution of stress and loss when applying SVPWM modulation [11] by having the inner switches assist the clamping switches. Utilizing the SVPWM technique within this strategy achieves the lowest possible switching loss for the ANPC [9]. In this scenario, which provides a mixed 3-level output, only a single zero state is available instead of the two neutral states, O+ and O-, which typically commute from P and N, respectively. As illustrated in Fig. 2, the neutral current flows through two neutral paths, significantly reducing conduction losses. Table 1 outlines the switching states for Positive (P), Negative (N), and O, with $x$ representing the index of each leg. These states are obtained by comparing the sinusoidal reference voltage with two carrier waveforms.

TABLE I. SINGLE ZERO STATE PWM TECHNIQUE

| Output Voltage | State | Cell 1 | | Cell 2 | | Cell 3 | |
|---|---|---|---|---|---|---|---|
| | | $S_{x1}$ | $S_{x5}$ | $S_{x2}$ | $S_{x3}$ | $S_{x4}$ | $S_{x6}$ |
| $+V_{DC}/2$ | P | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | O | 0 | 1 | 1 | 1 | 0 | 1 |
| $-V_{DC}/2$ | N | 0 | 1 | 0 | 1 | 1 | 0 |

During the P switching sequence, $S_{x6}$ is activated to evenly distribute the DC voltage when switches $S_{x3}$ and $S_{x4}$ are turned off. Similarly, $S_{x5}$ is activated during the N switching sequence. Switches $S_{x1}$ and $S_{x5}$, along with $S_{x4}$ and Sx6, function complementarily. For the neutral state, both the upper and lower paths for the neutral current are utilized simultaneously, resulting in a single neutral state, unlike other PWM strategies. By using both neutral current paths to conduct current, the conduction loss of the neutral current is reduced significantly due to the lower on-state resistance.

### *B. Parasitic Inductance Calculation and Design*

At high switching speeds, it's crucial to minimize the total parasitic inductances in the converter commutation loops to prevent voltage overshoots that can lead to the failure of switching devices. Parasitic inductances can occur in converter current loops due to various components, including DC-link capacitors, positive and negative DC bus terminals, neutral bus terminal, and switches. These inductances can be attributed to the sum of five main sources: the equivalent series inductance of DC-link capacitors ($L_{ESL}$), the inductance of positive and negative busbar ($L_{bus}$), the inductance of neutral busbar ($L_n$), mutual inductances ($L_m$), and the self-inductance of power switches ($L_s$).

The positive and negative DC bus terminals are the primary contributors to inductance and play a crucial role in minimizing parasitic inductances. In a two-layer DC busbar, parasitic inductance can be broken down into two components: self-inductance and mutual inductance. The total parasitic inductance can be calculated with (1) [12].

$$L_{\text{tot}} = \frac{\mu_0\,\mu_r\,l}{\pi}\left(\frac{1}{4}+\frac{4h}{h+w}-\frac{2h}{\sqrt{4\,(d+h)^2+kw^2}}\right) \tag{1}$$

where $l$, $w$, and $h$ represent the length, width, and thickness of each plate, respectively, and $d$ denotes the thickness of the insulator separating the two plates. By increasing the mutual inductance between two adjacent busbar layers we can effectively reduce the parasitic inductance [13].

### *C. Circuit Board Design Consideration*

In this study, a six-layer PCB layout is designed to distribute the current efficiently, with two layers dedicated to the positive DC bus, two for the negative DC bus, and one for the neutral bus. The layers are separated by insulators with thicknesses of 0.14mm and 0.35mm, resulting in extremely low parasitic inductance values due to the DC busbars. The instantaneous power at the DC side of the circuit, as depicted in Fig. 1, can be accurately calculated using (2) under ideal conditions.

$$P_{\text{dc}}(t) = \left(\frac{V_{\text{ac}}\,I_{\text{ac}}}{2}\cos\varphi - \frac{V_{\text{ac}}\,I_{\text{ac}}}{2}\cos(2\omega t+\varphi)\right) + \frac{L\omega\,I_{\text{ac}}^2}{2}\sin(2\omega t+2\varphi). \tag{2}$$

This power calculation considers the double-line frequency ripple components arising from both the AC side and the filter inductor. To mitigate these ripple effects, DC-link capacitors are necessary to eliminate the double-line frequency component. For the proposed system, the total DC-link capacitor value, which is required to achieve a 5% DC voltage ripple, is calculated as 160uF [14]. In the DC-link, two capacitor groups with a total capacitance of 320µF were created by combining 16 film capacitors with a capacitance of 40µF each, rated for 450VDC and featuring an extremely low ESR of 5.3mΩ and ESL of 11nH. LMG3522R030 650V, 55A, 26mΩ GaN FET devices are used for the 3L-ANPC circuit.

Since the proposed system is operating at 200kHz, and with three-level features, only an L-type filter is used between the grid and GaN-based 3L-ANPC converter as seen in Fig. 1. The value of each filter inductance is calculated as 90µH for 18% current ripple by using (3). To reduce size and tolerance on inductance value, PCB-based inductors are designed by using Ferroxcube planar E cores (E64/10/50) with 3F36 material. The total number of turns for the PCB-based planar inductance is calculated as 19. In this case, 5mm wide PCB traces were created as shown in Fig. 3 to carry the 30.1A (rms) phase current. As a result, the total number of 19 windings is distributed on five small PCBs placed between two E64/10/50 cores as shown in Fig.3. The size of each PCB-based planar inductance is 3.8×2 ×2.5 inches.

$$L_f = \frac{V_{\text{dc}}}{8 \times f_s \times I_{\text{ph}} \times \Delta I_{\text{ph}}} \tag{3}$$

In order to obtain the efficiency of AFE, the core losses occurring in PCB-based inductors must be calculated. The core loss for an E64/10/50 E with an effective volume of 35500 $mm^3$ was calculated as 0.7W using the data sheet of the 3F36 material. The total core losses are calculated as 4.2W considering three-phase PCB-based planar L filters.

## III. SIMULATION AND POWER LOSS CALCULATION

To analyze the performance, adjust parameters, and develop a control scheme, the 25kW, 480V 3L-ANPC is simulated by using the Voltage Oriented Control (VOC) method in MATLAB/Simulink. The simulation model is shown in Fig. 4. The VOC is a widely used method in grid-connected applications to control both active and reactive power. The main idea of VOC is to align the vector of grid voltage with

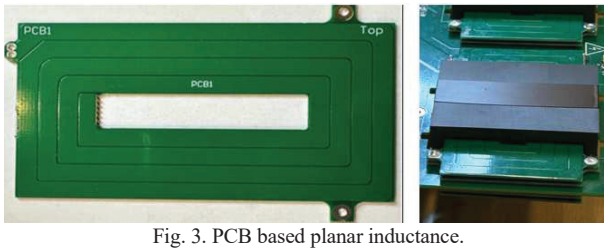


Fig. 3. PCB based planar inductance.

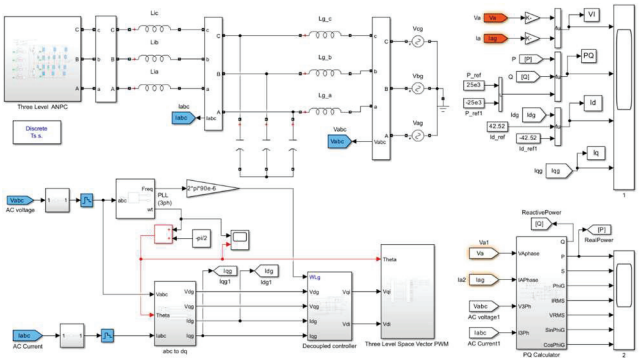


Fig.4. MATLAB simulation circuit of 3L-ANPC based AFE.

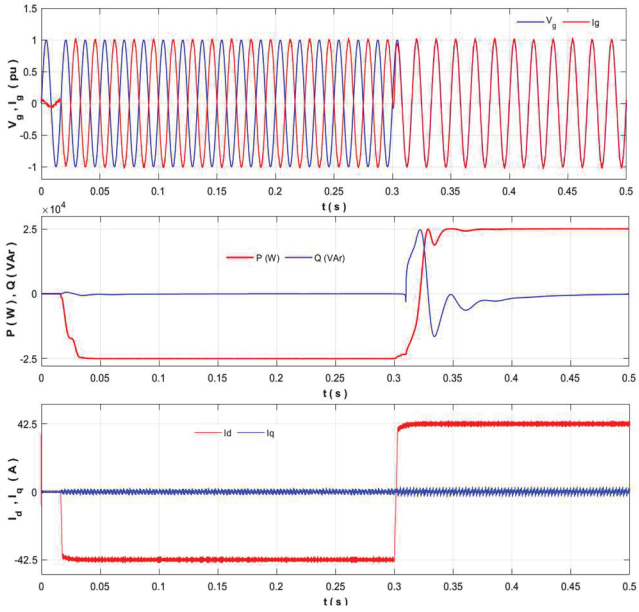



Fig.5 a) Grid voltages & currents, b) active & reactive power, c) active & reactive current.

the direct axis of the rotating (*dq*) reference frame. Due to this decoupling, active and reactive power can be managed independently in both Inverter and Rectifier Mode. Space Vector PWM signals for 3L ANPC are achieved from the output of the VOC method.

To test the performance of the converter in both directions, the reference active power of the AFE is changed from +25kW to -25kW after the first period in the model given in Fig. 4. The change of phase voltage and current at the common connection point, the change of active and reactive power of the AFE, and the change of the *dq*-components of the current are given in Fig. 5. As seen in the figure, after the first period, AFE works as an inverter and injects 25kW of active power into the 480V grid. In this case, there is a 180° phase difference between the grid voltage and current. After 0.3s, AFE starts working as a rectifier and draws 25kW of active power from the grid. In this case, there is no phase difference between the grid voltage and current. In the steady state, the reactive power exchange is zero for two operation modes. The VOC has successfully ensured active and reactive power exchange with AC grid by controlling

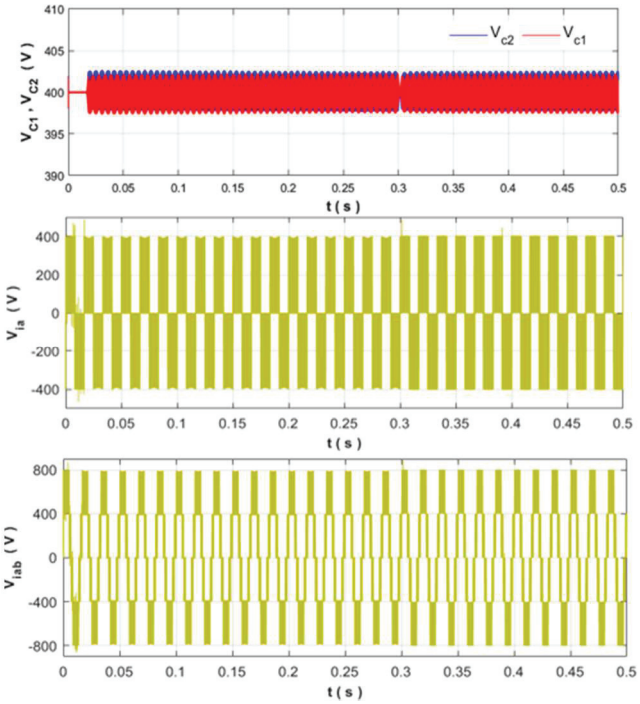



Fig.6 a) DC capacitors voltages b) inverter phase-neutral voltage, c) inverter phase-phase voltage.

the active and reactive current components of the current ($i_d$, $i_q$). The variation of the output phase voltage, phase-to-phase voltage, and dc-link capacitors voltages of the AFE is given in Fig. 6. As seen in the figures, the voltage of each DC-link capacitor is also equal to half of the DC voltage, and it is balanced for two operation modes.

To achieve the efficiency of the AFE, it is necessary to calculate the converter losses. For this purpose, firstly drain-

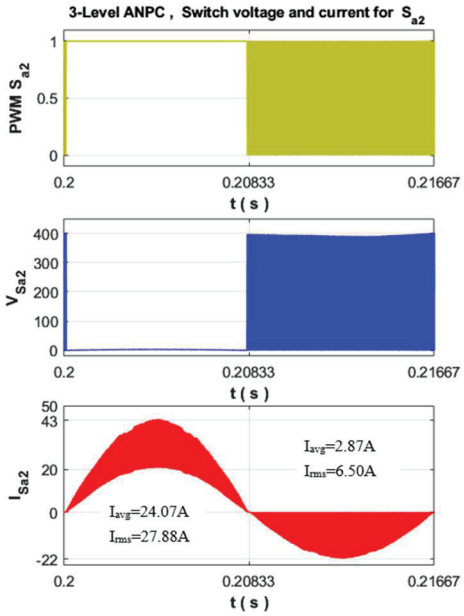



Fig.7 a) PWM signal b) drain-source voltage, c) drain current for $S_{a2}$

source voltages and drain currents are measured for all GaN devices in the simulation. For example, the drain-source voltage and drain current for the $S_{a2}$ switch are given in Fig. 7. Then, the conduction and switching losses for the LMG3522R030 GaN devices are calculated by substituting the measured signals and datasheet information for GaN in Equations (4)-(6).

$$P_{\text{con}} = I_{\text{rms}}^2 \times R_{\text{DS}_{\text{on}}}(T_{j100°\text{C}}) \tag{4}$$

$$P_{\text{on}} = \frac{1}{2} I_{\text{DS}} \times V_{\text{DS}} \times \frac{V_{\text{DS}}}{V_{\text{DS}_{\text{Test}}}} \times \frac{I_{\text{D}}}{I_{\text{D}_{\text{Test}}}} \times t_{\text{on}} \times f_{\text{s}} \tag{5}$$

$$P_{\text{off}} = \frac{1}{2} I_{\text{DS}} \times V_{\text{DS}} \times \frac{V_{\text{DS}}}{V_{\text{DS}_{\text{Test}}}} \times \frac{I_{\text{D}}}{I_{\text{D}_{\text{Test}}}} \times t_{\text{off}} \times f_{\text{s}} \tag{6}$$

where $t_{on}$ is the turn-on rise time and $t_{off}$ is the turn-off fall time. For the test conditions where these times are obtained, the drain-source voltage is $V_{DSTest}$ and the drain current is $I_{DTest}$. These values are taken from GaN's data sheet. Considering both GaN switch losses and filter core losses, the total power loss for the 3L ANBC-based AFE is obtained as approximately 1.33%, as seen in Table 2. This shows that AFE has an efficiency of 98.67%.

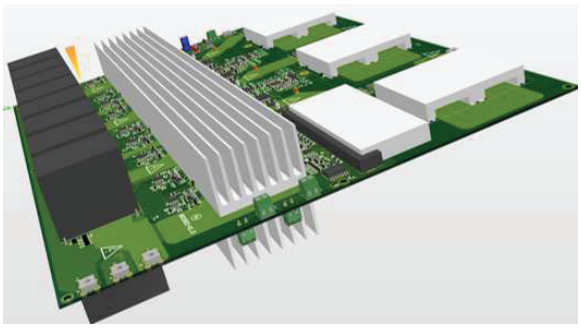
TABLE II. POWER LOSSES FOR THREE LEVEL AFE

| | 0 < t < T/2 | | | T/2 < t < T | | | |
|---|---|---|---|---|---|---|---|
| | $P_{Con}$ | $P_{on}$ | $P_{off}$ | $P_{Con}$ | $P_{on}$ | $P_{off}$ | $P_{avg}$ |
| $S_{a1}$ | 28.70 | 5.03 | 39.6 | 0 | 0 | 0 | 73.33/2= 36.67 W |
| $S_{a2}$ | 30.31 | 0 | 0 | 1.65 | 0.09 | 0.72 | 32.77/2= 16.39 W |
| $S_{a3}$ | 1.65 | 0.09 | 0.72 | 30.40 | 0 | 0 | 32.86/2= 16.43 W |
| $S_{a4}$ | 0 | 0 | 0 | 28.68 | 5.03 | 39.6 | 73.31/2= 36.66 W |
| $S_{a5}$ | 1.64 | 0.09 | 0.72 | 1.64 | 0 | 0 | 4.1/2= 2.05 W |
| $S_{a6}$ | 1.64 | 0 | 0 | 1.64 | 0.09 | 0.72 | 4.1/2= 2.05 W |
| Total Losess for 3-Leg of ANPC | | | | | | | **330.66 W** |
| Total Core Losess for 3-phase Lfilters | | | | | | | **4.20 W** |
| $25kW * (x/100) = 334.86W$ | | | | | | | $x = \%1.33$ |

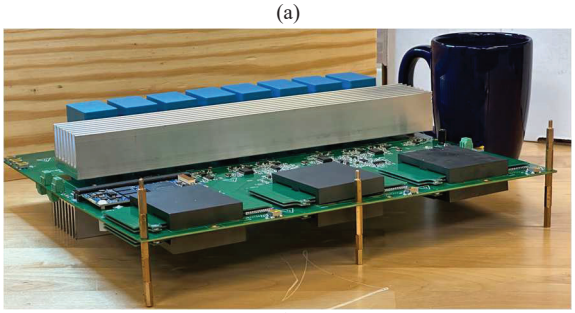
## IV. EXPERIMENTAL RESULTS

After the simulation stage, the board layout of a 480V grid-connected, bidirectional, GaN-based 25kW AFE is created in Altium as shown in Fig. 8(a) by using the detailed schematics for all circuits. A custom-designed 25kVA, 200kHz 3L-ANPC board employing all GaN devices, gate drives, DC capacitors, measurement circuits, output L-filter and FPGA controller is shown in Fig. 8. The size of the system is 13×12×4 inches.

This controller is responsible for generating gate signals, reading grid-side voltage and current measurements, and receiving the fault, overcurrent, and temperature signals sent by LMG3522R030 GaNs. Device programming is achieved using VHDL codes generated by the Simulink HDL coder. For accurate measurements, two Analog-to-Digital Converters (ADCs) of AD7328 are employed to monitor the three-phase voltages and currents at the DC side, the converter, and the grid side of the system. Each ADC provides a throughput rate of 1MSPS across eight channels. With five channels of each ADC dedicated to reading high-speed measurements from the sensor boards, this throughput rate ensures efficient data handling. Communication between the ADCs and the FPGA is facilitated by a high-speed SPI interface protocol, ensuring rapid and reliable data transfer. The system operation is synchronized with the 60Hz grid phase through Phase-Locked Loop (PLL) control.



(a)



(b)

Fig. 8. (a) Board Layout of the proposed system (Altium) (b) A real view of the GaN-based 25kW AFE.

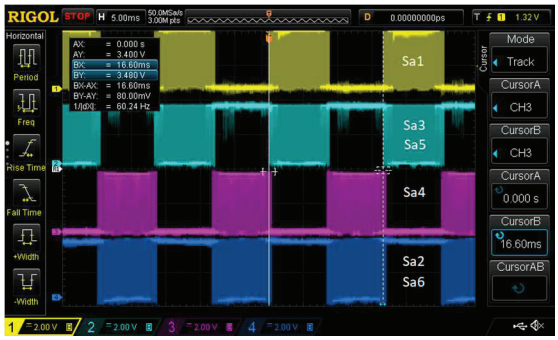



Fig. 9. The 200kHz SVPWM signals for one phase leg.

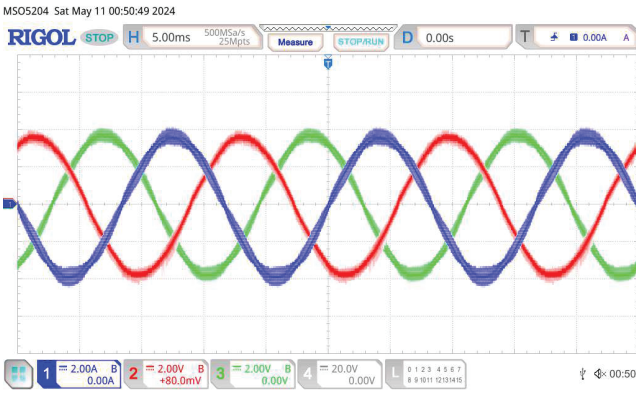



Fig. 10. Real time results three-phase current waveform for $f_{sw}$=200kHz with $V_{DC}$=100V.

Additionally, decoupled current control is used to generate the precise PWM gate signals needed for efficient modulation. This comprehensive setup ensures that the proposed modulation scheme is both robust and effective under real-world conditions. The Gate-Source voltage signals are evaluated on the board as shown in Fig. 9 illustrating the switching in half of the cycle in the switching frequency and half of the cycle in the grid frequency. In this experiment, the current is controlled at a 2A reference, as shown in Fig.10. Fig. 11 displays the measurements of the phase-neutral voltage (channel-B, pink) and the phase-A current waveform (channel-A, yellow). The grid voltage and current are synchronized, and the phase-neutral voltage exhibits three levels. Additionally, Fig. 12 shows the line-to-line voltage between phases-A and B (channel-B, pink). The converter phase-neutral and the line-to-line voltage depicted in Fig. 10 and Fig. 11 are consistent with the simulation results of Fig. 6.

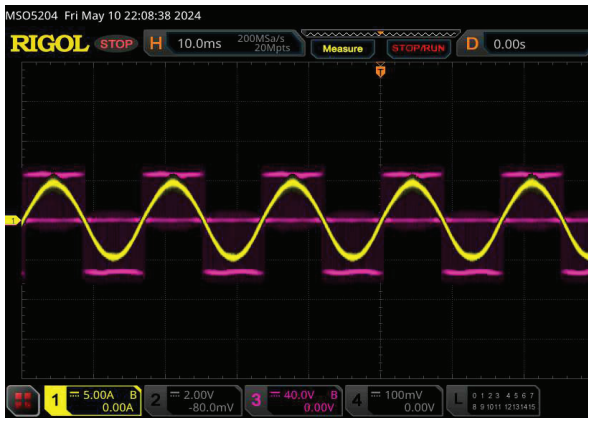



Fig. 11. The 200kHz SVPWM signals for one phase leg.

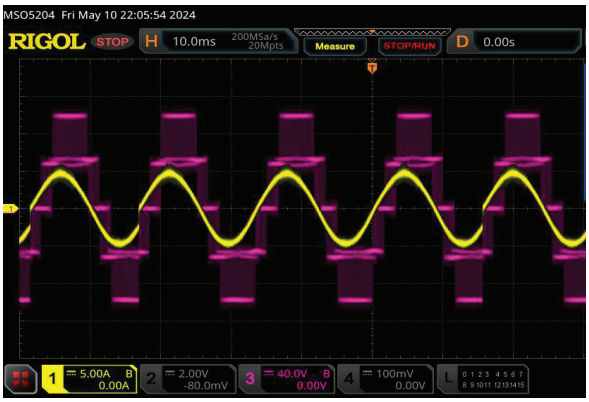



Fig. 11. The 200kHz SVPWM signals for one phase leg.

## V. Conclusions

In this study, a compact and highly efficient bidirectional GaN-based 25kW AFE converter has been designed and implemented which can be used for many industrial applications in 480V grid. Besides, PCB-based dc-link, and PCB-based L filters were preferred to achieve a highly efficient and compact system design. The efficiency of the entire system is calculated approximately 98.67%. With high switching frequency, and preferred design method, high power density and efficiency are obtained. In addition, the proposed single-board design enables automatic manufacturing and decreases the cost.

## Acknowledgment

Dr. Erkan Deniz (edeniz@firat.edu.tr) thanks financial support from the Scientific and Technological Research Council of Turkey (TUBİTAK) BIDEB-2219 Postdoctoral Research Program.

## References

[1] V. Ž. Lazarević, M. Abplanalp, F. Canales, M. Schweizer, A. Antoniazzi and L. Ghezzi, "Functional Features of Isolated AC/DC Converter Interface in Future Low-Voltage DC Microgrids," 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-8

[2] N. Altin, S. Ozdemir, "Three-phase three-level grid interactive inverter with fuzzy logic based maximum power point tracking controller", Energy Conversion and Management vol. 69, pp. 17–26, 2013.

[3] O. Aydogmus, E. Deniz, and K. Kayisli, "PMSM Drive Fed by Sliding Mode Controlled PFC Boost Converter," Arab J Sci Eng, vol. 39, pp. 4765–4773, April 2014.

[4] P. Bhuvela, H. Taghavi and A. Nasiri, "Design Methodology for a Medium Voltage Single Stage LLC Resonant Solar PV Inverter," 2023 12th International Conference on Renewable Energy Research and Applications (ICRERA), vol.1, pp. 556–562, Oshawa Canada, Sep. 2023.

[5] K. Kumari, S. Mapa, R. Maheshwari, "Loss Analysis of NPC and T-Type Three-Level Converter for Si, SiC, and GaN based Devices," 2020 IEEE 9th Power India International Conference (PIICON)

[6] M. Najjar, e.t all, "Design Procedure and Efficiency Analysis of a 99.3% Efficient 10 kW Three-Phase Three-Level Hybrid GaN/Si Active Neutral Point Clamped Converter," IEEE Transactions on Power Electronics, vol. 37(6), pp. 6698–6710, June 2022.

[7] Deniz E., Altun H., Beş Seviyeli Izole DA Kaynaklı Kaskat Inverterin SDGM Teknigi Ile Kontrolü, SAÜ. Journal of Science, 2007, 11(1)1, 1-9.

[8] M. Najjar, H. R. Nielsen and L. B. Rasmussen, "A High-Power Density Three-Phase Three-Level Hybrid IGBT/SiC Interleaved Active Neutral Point Clamped Voltage Source Converter," 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe),vol.1, pp.1-6, Aalborg, Denmark, 2023.

[9] G. Zhang, Y. Yang, F. Iannuzzo, K. Li, F. Blaabjerg and H. Xu, "Loss distri-bution analysis of three-level active neutral-point-clamped (3L-ANPC) converter with different PWM strategies," 2016 IEEE 2nd Annual Southern Power Elec-tronics Conference (SPEC), Auckland, New Zealand, 2016.

[10] S. K. Mondal, B. K. Bose, and V. Oleschuk, "Space vector pulse width modula-tion of three-level inverter extending operation into overmodulation region," IEEE Trans. Power Electron., vol. 18, no. 2, pp. 604–611, Mar. 2003.

[11] Y. Jiao, F. Lee, "New Modulation Scheme for Three-Level Active Neutral-Point-Clamped Converter with Loss and Stress Reduction", IEEE Transactions on Industrial Electronics, vol. 62, no. 9, September 2015.

[12] Y. Wang, A. Poorfakhraei, M. Narimani and A. Emadi, "A 70kW 3-Level Active Neutral Point Clamped Traction Inverter PCB Design for Stray Inductance and Thermal Performance Optimization," IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society, Toronto, ON, Canada, 2021, pp. 1-6,

[13] H. Gui et al., "Design of Low Inductance Busbar for 500 kVA Three-Level ANPC Converter," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 7130-7137.

[14] H. Zhang, X. Li, B. Ge and R. S. Balog, "Capacitance, dc Voltage Utilizaton, and Current Stress: Comparison of Double-Line Frequency Ripple Power Decoupling for Single-Phase Systems," in *IEEE Industrial Electronics Magazine*, vol. 11, no. 3, pp. 37-49, Sept. 2017.