IEEE Open Journal of
Power Electronics

Received 13 September 2024; accepted 8 October 2024. Date of publication 15 October 2024;
date of current version 6 November 2024. The review of this article was arranged by Associate Editor Lei Gu.

Digital Object Identifier 10.1109/OJPEL.2024.3481056

Thermal Modeling and Degradation Profiling of E-Mode GaN HEMTs for Aging Characterization

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This work was supported in part by the National Science Foundation under Grant 2239966, and in part by the OUSD(R&E) T&AM/MINSEC Program through the Cornerstone OTA Contract under Grant CS-19-0202.

ABSTRACT Managing the thermal behavior of GaN devices under test (DUT) poses significant challenges during accelerated thermal cycling (ATC) tests, particularly due to the compact packaging of small GaN devices (e.g., QFN package) and the sharp rise in the device's R_{DSon} at high junction temperatures. This paper presents a framework for analyzing and modeling the thermal response performance of the ATC test setup and evaluating the impact of non-linear dissipated power on the GaN DUTs. It outlines the limitations of conventional thermal sensors in accurately estimating the DUT's junction temperature through case temperature measurements under ATC conditions. The analysis and modeling of the experimental junction temperature response function shows about 4 s time constant in the measurements using a thermistor placed near the DUT, highlighting the GaN DUT's susceptibility to thermal runaway under ATC conditions ($T_{j-max} > 125$ °C), where the thermal time constant significantly exceeds the DUT's thermal transient time. Consequently, an on-state resistance (R_{DSon})-based T_j estimation method is employed to monitor the T_j and control the thermal cycling window boundaries effectively. Experimental investigations of several e-mode GaN HEMTs under different ATC windows are conducted to validate the ATC testing framework. Moreover, the temperature coefficient of on-state resistance (α) is characterized and quantified - considering fully packaged individual GaN DUTs' mechanical and electrical degradation mechanisms.

INDEX TERMS E-mode GaN HEMTs, reliability assessment, accelerated thermal cycling, junction temperature estimation, thermal modeling, and R_{DSon} thermal coefficient.

I. INTRODUCTION

Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) have recently emerged as a potential key switching power device – enabling high-efficiency (≥99%) kilowatts-range power converters even with high switching frequencies (>1 MHz) [1]. However, since GaN power FETs have been in commercial use relatively recently, there is no sufficient data to assess their practical reliability and the encompassing power converters. Unlike silicon-based power-switching devices, whose reliability methodologies matured over decades of application and enhancement, GaN power FETs' lifetime, failure mechanisms, and other reliability metrics require further investigation. Accelerated stress tests, a traditional method for evaluating the reliability of power semiconductor devices, follow established protocols [2], [3], [4], [5].

According to the physics of failure approach, the semiconductor component's lifetime will be shorter at higher junction temperatures (T_j) [6]. Hence, accelerated thermal cycling (ATC) is one of the most commonly used methods for rapid reliability assessments of power semiconductor switching devices [7], [8]. The ATC involves subjecting the device to temperature cycles above and below room temperature for thousands of hours or cycles to identify different degradation mechanisms. The variation in junction temperature during ATC is facilitated by either active or passive heating methods. In active heating, AC or DC current is injected through the DUT's drain-source channel to induce self-heating by the conduction and/or switching losses where the junction temperature can be adjusted. In passive heating, the DUT's junction temperature is adjusted by soaking the

device in a thermal chamber where the ambient temperature is controlled. The DUT can be characterized by swinging the ambient temperature inside the thermal chamber within the thermal cycling window. Both approaches contribute to several mechanical and electrical degradation mechanisms from the DUT's packaging perspectives to the semiconductor material and technology's point of view. Throughout such tests, the junction temperature is an imperative parameter to monitor properly to avoid DUT's failure due to thermal runaway. Given the relatively lower thermal conductivity of GaN and Si devices compared to silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) and the small packaging (i.e., QFN) for e-mode GaN HEMTs available in the market, thermal management is a challenging process during ATC for small packages [9]. While the thermal heat pad for the GaN devices (i.e., source pad) with QFN package is relatively small compared to Si MOSFETs within the same voltage and current ratings, it is challenging to manage the thermal dissipation from the GaN FET's junction channel to ambient. Additionally, the increase in the on-state resistance (R_{DSon}) by T_j variation from 25 °C to 150 °C can be roughly double for GaN FETs compared to SiC FETs [10] – this adds more complexity to dissipate the heat from the junction to the ambient environment for GaN device under ATC. Commercially available infrared cameras, thermocouples, thermistors, and other commercial temperature sensors have delays in the order of milliseconds or more. Hence, these sensors are not preferable for monitoring GaN HEMTs junction temperature under a wide-range ATC tests. Most available research and knowledge about the Foster thermal modeling technique used for the analysis of thermal performance of power semiconductor DUT usually assume steady state junction temperature [11], [12], [13]. This assumption is not true in several applications dealing with fast changing mission profiles, and also in case of devices like GaN FETs whose on-state resistance varies quickly with rise in temperature. Furthermore, such an assumption is particularly not applicable for ATC tests as the DUTs' junction temperature changes throughout each thermal cycle window (running across a few seconds). Hence, this paper presents a non-linear dissipated power profile-based thermal analysis and empirical modeling method to accurately extract the time constants associated with the measurement of junction-to-ambient temperature of the DUT – validating the importance of utilizing proper temperature measurements for GaN HEMT devices under wide-windows ATC test.

For monitoring GaN HEMTs' aging/degradation, several common indicators (R_{DSon}, transconductance, the drain current (I_D), gate leakage current, and gate-source threshold voltage) were reported in [14], [15]. However, due to the accuracy and difficulties associated with the measurements of each health indicator, R_{DSon} is being widely employed as a suitable parameter for monitoring GaN devices' aging/degradation [15], [16], [17]. While the V_{DSon} measurement circuits may add complexity to the real-world applications, and impose overshoot, and oscillation to the voltage/current waveforms of the DUT, this paper introduces an alternative aging inductor which is the heating time for the DUT to swing the junction-to-ambient temperature within a predefined temperature-limits shrinks with the devices' aging time. Thus, by monitoring the DUT's heating time with respect to the DUT's junction/case-ambient temperature window, the remaining useful lifetime of the degradation level can be modeled and extracted.

The temperature coefficient of the on-state resistance is essentially the R_{DSon} characteristic slope, indicating how the on-resistance increases with temperature. For the GaN HEMTs, the R_{DSon} is approximately consist of the metallic contacts' resistance of the drain and source terminals and the conduction channel between the drain and source (i.e., the two-dimensional electron gas, 2DEG). This research provided insights on the temperature coefficient of the R_{DSon} for GaN HEMTs under accelerated thermal cycling as another parameter to validate the increase in the on-resistance with devices aging. When compared Si power MOSFETs and SiC MOSFETs with respect to on-state resistance temperature coefficient, SiC MOSFETs feature significantly lower, and less temperature-sensitive on-state resistance. This lesser temperature coefficient can be partially attributed to the decrease in the channel resistance of 4H-SiC MOSFETs with increasing temperature due to an increase in MOS channel mobility caused by the de-trapping of charges in the gate oxide [18]. This decrease in the channel resistance counteracts the increase of the drift region resistance, resulting in a lower positive temperature coefficient in the total on-state resistance [19]. However, the reduction in the temperature coefficient for GaN HEMTs with the devices aging considered in this research can be partially attributed to the increase in the conduction channel resistance, drain-source contacts degradation, and reduction in the electrons' density in the 2DEG channel as the devices age.

This paper presents a detailed analysis and modeling of the thermal response function for an experimental laboratory GaN ATC testing setup designed and developed to investigate and address the abovementioned concerns. Under different ATC profiles, several GaN HEMTs (rated: 650 V, 7.5 A, and 180 mΩ R_{DSon}) with integrated gate drivers are investigated experimentally to assess their health conditioning and degradation patterns. To avoid the thermal runaway scenario experienced in the early stage of this research, as highlighted in the thermal analysis in next sections, R_{DSon}-based T_j estimation method is utilized to perform online/in-situ monitor T_j and control the thermal cycling window boundaries over a long-term automated ATC testing of GaN DUTs. Additionally, the Keysight power device curve tracer (B1506A) is used to characterize the DUTs offline every 1000 cycles and validate the online R_{DSon} measurements from the automated testing setup. Based on that, this research highlights thermal performance and challenges associated with e-mode GaN HEMTs under ATC as follows:

i) The proposed thermal analysis and empirical modeling method considering 'non-linear' dissipated power profiles provide more precise estimation of the thermal

behavior of the DUTs, and also be applied to various power devices under thermal cycling conditions. Mathematical analysis of the proposed modeling approach and the corresponding explanation of the thermal response are also provided in this paper.

ii) The research highlights an alternative aging indicator for semiconductor switching devices, emphasizing the junction channel's heating time during the thermal cycling test or the time taken for the R_{DSon} to change from one value to another higher value during the heating time of the ATC is reduced with aging.

iii) R_{DSon} temperature coefficient (α) analysis validates that the α values of GaN DUTs' decrease with aging – caused by mechanical and electrical degradation mechanisms of the fully packaged GaN DUTs.

II. THERMAL ANALYSIS AND MODELING

In this research, e-mode GaN HEMTs are evaluated and characterized under long-term ATC testing. The junction channel is actively heated up to a specified maximum temperature (T_j limit) by passing DC current through the drain-source channel. It is then turned off to allow the DUT to cool to a predefined minimum temperature level (e.g., room temperature), which marks the end of the thermal cycle. Notably, no heatsink is attached to the DUT in the ATC setup to facilitate proper self-heating and monitor and analyze the DUT's temperature measurements. Different thermal cycling test profiles are considered in this research, which are tabulated in Section III.

Individual e-mode GaN HEMT devices, rated for 650 V DC blocking voltage, 7.5 A continuous current, and on-state resistance of 180 mΩ at 25 °C ambient temperature with an integrated gate driver are considered in this research [20]. Fig. 1(a) shows the GaN board layers developed to have a single GaN device with a thermistor attached near the device, decoupling capacitors, and other conditioning circuits for the integrated gate driver of the GaN DUTs. The GaN board's layout includes minimized gate, drain, source, and measurement terminals for direct insertion into device curve tracers for characterization or into the ATC power supply and measurement circuits, as depicted in Fig. 4(c), where the current/voltage measurements and power supply and load connection points take place. The GaN PCB board includes an array of 20 (4×5) vias beneath the device's source pad (at the bottom, as shown in the bottom layer in Fig. 1(a)), which aids in heat dissipation through natural convection, as no heatsink is attached to the DUTs. The ATC is intended to heat the GaN devices' junction channel actively to a particular T_j max and subsequently cool down to a specified T_j according to predefined boundaries of the thermal cycle. The DUTs are self-heated by passing DC current through the drain-source channels and monitoring the junction temperature to reach the predefined limit. Then, the DUTs are turned off to allow them to cool down naturally until the junction temperature reaches the predefined T_j low. A thermal sensor (i.e., thermistor) is attached near

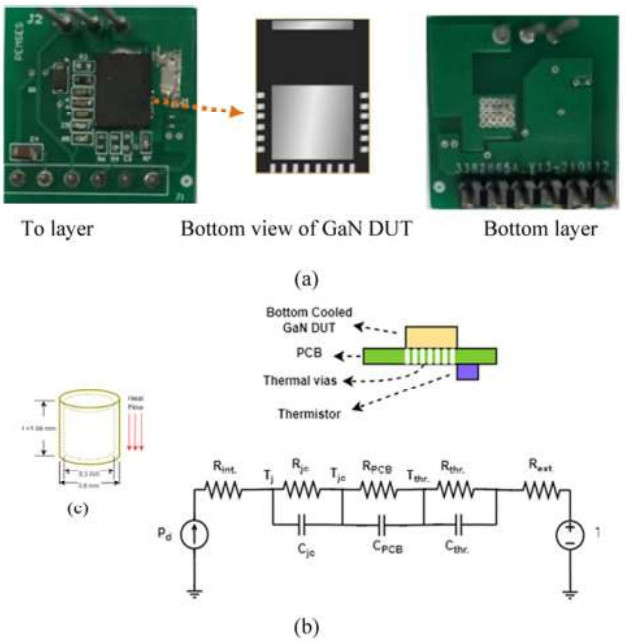


FIGURE 1. GaN DUT board. (a) Top and bottom layers of the GaN boards and the bottom view of the GaN DUT in QFN package (rated 650 V, 7.5 A DC). (b) Thermal via dimensions. (c) Equivalent thermal circuit of the GaN board includes the components involved in the DUT's T_{ja} measurements.

the GaN devices and serves to estimate the junction temperature of the DUT during the ATC. The equivalent thermal circuit for the components (mainly, GaN device, PCB, and thermal sensor) involved in the T_j monitoring is presented in Fig. 1(b) – which is derived based on the Foster thermal modeling approach [11], [12], [13]. As shown in Fig. 1(b), the $R_{th}C_{th}$ network denotes the thermal resistance and capacitance of the individual components (GaN DUT, PCB, and thermistor as individual devices) involved in the junction temperature measurements. As the GaN DUT is subjected to a power pulse during the heating time of the thermal cycle, a thermal steady-state or equilibrium is not reached as the device's on-state resistance increases. Thus, the *RC* network represents the time constant contributed by the multiple devices involved in the experimental thermal response function measurement. On the other hand, the thermal response function has a dependency on devices/ or power electronics circuit's properties. Hence, the linear region of temperature change inside the devices is represented by $R_{int.}$ and R_{ext}. This model is derived based on experimental thermal response function measurement during accelerated thermal cycling of GaN HEMT DUTs, where no heatsink was used.

The equivalent thermal model represents the dissipated power (p_d) generated by self-heating, driven by the product of ($I_D^2 \times R_{DSon}$). Given the R_{DSon} is changing with T_j according to the datasheet [20] and pre-testing characterization performed in the lab to extract the R_{DSon} relationship with T_j, the power dissipation function follows the pattern of the change in R_{DSon} with T_j under a constant heating current (I_D). As per the thermal circuit representation in Fig. 1(b), the ambient temperature is modeled as a constant voltage source (i.e.,

25 °C). The thermal impedances are represented by multiple networks of thermal resistors and capacitors corresponding to the components (GaN device, PCB, and thermistor) involved in the T_{ja} measurements. The heat flow is downwards from the GaN device's junction through the PCB vias into the ambient environment, aided by natural convection. A thermistor is placed near the PCB's vias for DUT's temperature measurement and estimation of T_j. Since the FR4 epoxy has a relatively low thermal conductivity of ~0.3 W/mK [21], the vias provided a channel to get the heat to the ambient atmosphere and increase the thermal conductivity between the top and bottom layers of the PCB. The Cauer network is mainly used to assess the thermal modeling of different layers of a component or module, while Foster modeling is typically used to study the thermal system comprising multiple components. Hence, considering that this research includes testing the GaN devices that are fully packaged (without access to internal layers), the Foster thermal network is used for the analysis without factoring in the internal layers of the devices.

Based on the temperature response of the system, a Foster thermal model can be constructed by connecting multiple *RC* circuits in series and organized into subsets with decoupled time constants [13]. Subsequently, a complete mathematical model of the Foster network can be derived by summing the exponential terms in a closed form of the simple analytical expression. The Foster thermal model is typically preferred for describing a system's thermal behavior with multiple components on the PCB. Foster's model describes thermal behavior as a "individual device" where thermal resistances and capacitances of the system are combined as a net thermal impedance (Z_{th}). For a given power converter, the thermal response function can be expressed as in (1) [11], [12], [13].

$$T_{th}(t) = p_d(t) Z_{th} \tag{1}$$

Where T_{th} is the thermal response function, $p_d(t)$ is the dissipated power as a function of time, and Z_{th} is the system thermal impedance (i.e., $Z_{th} = R_{th}\ C_{th}$). The Foster thermal impedance consists of combinations of parallel *RC* network, as depicted in Fig. 1(b). Therefore, the thermal impedance can be presented in the s-domain as in (2).

$$Z_{th}(s) = \sum_{i=1}^{\infty} \frac{R_i}{R_i C_i s + 1} \tag{2}$$

Where R_i and C_i represent the thermal resistance and capacitance, respectively, of individual devices involved in the measurement of the response function. For a constant dissipated power, by substituting (2) in (1), the thermal response function can be written as in (3).

$$T_{th}(s) = \frac{P_d}{s} \sum_{i=1}^{\infty} \frac{R_i}{R_i C_i s + 1} \tag{3}$$

where the term (P_d/s) is the s-domain representation of dissipated power as a step function (i.e., P_d is constant). By taking the inverse Laplace transformation for the (3), the thermal response function can be expressed in time domain as in (4) for a step response dissipated power [11].

$$T_{th}(t) = P_d \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}}\right) \tag{4}$$

Here, P_d is assumed as a constant value, R_i is the individual devices' thermal resistance, τ_i is the thermal time constant determined by the multiplication of the R_i and thermal capacitance (C_i) of the different elements of the system, and n is the number of devices involved in the thermal response function (T_{th}) measurement.

The dissipated power can be expressed as in (5).

$$p_d = |V_{DSon} I_D| + |I_G^2 R_{G,int}| \tag{5}$$

Where the product term (V_{DSon}. I_D) represents the switching and conduction losses, V_{DSon} is the on-state voltage drop across the DUT, whereas the dissipated heat of the internal gate driver resistor is represented by $I_G^2 R_{G,int}$ (which is ignored in this analysis as the internal gate resistance is about 2 Ω and the average gate-source current is about 40 μA when the device is fully turned on [19] and [22]; leading to a dissipated power of $<<1$ μW). Since DC drain-to-source (I_D) current is used to heat the DUT during the heating time of the ATC, the switching losses do not significantly contribute to the device's self-heating. So, the dissipated power is approximated as a conduction power loss as in (6), where p_d is a function of heating time.

$$p_d \approx |I_D^2 R_{DSon}| \tag{6}$$

In the thermal cycling test under consideration (and in many practical cases), the dissipated power profile is not constant. The DUT is exposed to self-heating through a DC current (I_D), causing the R_{DSon} value to change dynamically. This dynamically changes the dissipated power during the thermal cycling process in a non-linear fashion. Accordingly, this paper presents an empirical modeling technique that considers non-linear dissipated power profile. As per the system model shown in Fig. 1(b), the thermal impedance can be expressed for the junction-to-ambient (Z_{ja}) condition. The time constants associated with the main components used in the junction temperature measurement (i.e., GaN DUT, PCB, and thermistor) and presented in the equivalent thermal impedance network are τ_i (where $\tau_i = R_i C_i$). Accordingly, the junction-to-ambient temperature (T_{ja}) response function can be written as in (7).

$$T_{ja}(s) = p_d(s) Z_{ja}(s)$$

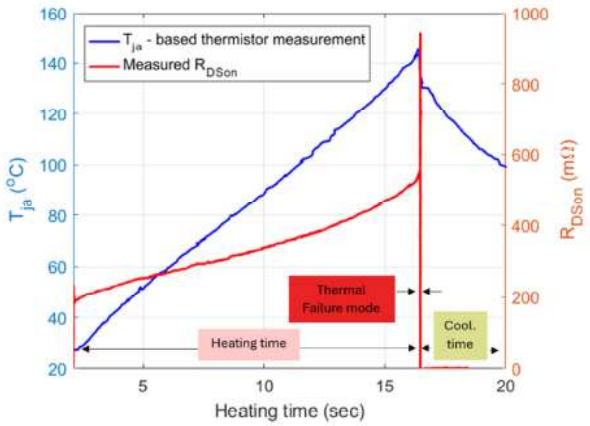
Or

$$T_j(s) = p_d(s) Z_{ja}(s) + T_a(s)$$

where

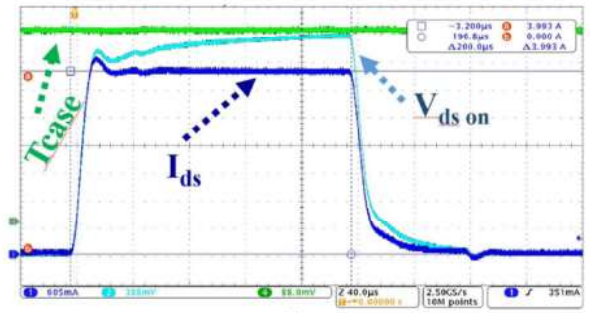
$$Z_{ja}(s) = \sum_{i=1}^{\infty} \frac{R_i}{R_i C_i s + 1} \tag{7}$$

Here, T_j is the junction temperature, T_a is the ambient temperature (i.e., ~25 °C), p_d is the dissipated power function in the DUT's junction, and t is the heating time of the ATC.



(a)

(b)



(c)

FIGURE 2. **(a) Measured T_j using a thermistor at the bottom of the experimental GaN board, calculated R_{DSon} -based on I_D and on-state voltage measurement, and an exponential curve fitted measurement of T_{ja} with respect to the thermal cycle heating time. (b) GaN FET experienced thermal runaway under a thermal cycling test with a thermistor for DUT's case temperature monitoring. (c) T_c measurement using thermistor verses R_{DSon} measurement for estimating T_j under a short pulse of drain-source current.**

From preliminary thermal cycling tests of multiple GaN DUTs, the devices experienced thermal runaway, as shown in Fig. 2. It was a result of the 'not fast-enough' junction temperature measurement system used in the control of the ATC boundaries (where a thermistor was used to monitor the GaN DUT case temperature for estimating the junction temperature of the DUT). The thermistor measurements were calibrated and verified by soaking the GaN board with the thermistor in the thermal chamber and testing it at different temperature levels. It can be noticed in Fig. 2(a) that during the thermal cycling window of 25 °C to 180 °C, the thermistor measurement temperature was not fast enough to capture the rapid rise in T_j caused by a rapid increase in R_{DSon} as the device junction temperature approaches the thermal cycle window limit. Consequently, the GaN DUT experienced thermal runaway, as shown in Fig. 2(b). During the heating up time of the thermal cycles, the junction temperature of the GaN DUT keeps rising as the conduction loss (I^2R_{DSon}) keeps increasing in the junction (due to R_{DSon} increase), resulting in higher heat dissipation throughout (since there is no heatsink or any cooling mechanism used during the heating time of the thermal cycles); where the heating current here is DC current. Therefore, thermal equilibrium operating point is not reached during the heating time of the thermal cycles even though it is in several seconds. The estimation of the junction temperature using the R_{DSon} value allows for an almost immediate capture of the real-time temperature information (just a few milliseconds). However, the use of a thermistor with slow response would create additional delays (in the order of seconds, as discussed in next) for the temperature measurements [23], that can create reduced accuracies or errors, and may even lead to thermal runaway. Hence, thermistors or thermocouples would not be sufficient for such transient tests.

Subsequently, an investigation on R_{DSon} measurement is explored in which a current pulse is injected through the drain-source channel of the GaN DUT, and the device's case temperature, V_{DSon}, and I_D are recorded, as shown in Fig. 2(c). It can be noticed that passing a current of about 600 mA for about 200 μs causes the R_{DSon} (which is equal to V_{DSon}/I_D) to increase as depicted in V_{DSon}, while the case temperature is not able to capture this change in the junction temperature. Therefore, for ATC tests of GaN DUTs, R_{DSon}-based T_j estimation method is adopted further in this research to allow the implementation of accelerated wide thermal cycling windows ($T_{j\text{-max}} > 125$ °C) and ensure a fast T_j estimation approach to avoid thermal runaway scenarios.

To analyze the thermal performance of the components involved in the ATC of the GaN board and the causes of the DUT's thermal runaway, the hereafter section presents a generalized thermal modeling approach for evaluating the thermal time constant values involved in ATC testing – where p_d is varying with heating time (linearly or non-linearly). Based on (7), the Z_{ja} can be expanded according to the individual thermal impedance of each component in the GaN board as in (8).

$$Z_{ja}(s) = \frac{R_1}{\tau_1 s + 1} + \frac{R_2}{\tau_2 s + 1} + \frac{R_3}{\tau_3 s + 1} + \ldots \\ \ldots + \frac{R_i}{\tau_i s + 1} \tag{8}$$

where R_i and τ_i are the thermal resistance and thermal time constant of individual components involved in the junction temperature measurements. For a given p_d and a measured temperature according to (7), the system's Z_{ja} can be calculated.

From the temperature response function (T_{thr}) deduced using the thermistor measurements during the experimental

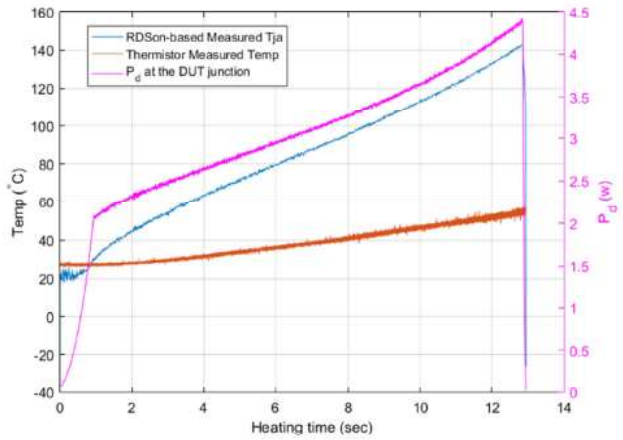


FIGURE 3. Measured dissipated power and temperatures of the DUT.

accelerated thermal cycling (depicted in Fig. 3), the data are imported into MATLAB software to perform curve fitting and extract the thermistor 'measured temperature response function as presented in (9). The best fit for the measured data is fitted with a type-I exponential function. The curve fitting tool generates the constants a, b, c, and the R^2 value, which correspond to the goodness of fit of a model.

$$T_{thr}(t) = a * e^{-bt} + c \tag{9}$$

The constants a, b, and c equal 1.23, 0.25, and 12.4, respectively. The statistical R^2 value is 0.956. Based on (8), the thermistor's thermal impedance can be expressed as in (10).

$$Z_{thr}(s) = \frac{T_{thr}(s) - T_a(s)}{p_d(s)} \tag{10}$$

where Z_{thr} is the thermal impedance of the thermistor. It is worth noting that thermistor exhibits non-linear resistance-temperature properties, and most are extremely non-linear [23], which makes it necessary to use a more complex form to derive accurate temperature measurements, as considered in this research. According to (8), the thermistor's thermal impedance is given in (11).

$$Z_{thr}(s) = \left(\frac{R_{thr}}{\tau_{thr}}\right)\left(\frac{1}{s + \frac{1}{\tau_{thr}}}\right) + \frac{R_{ext}}{s} \tag{11}$$

R_{ext} is an additional thermal resistance that contributes to the thermistor's response, as in Fig. 1(b). By substituting (11) in (10) and taking its inverse Laplace transformation, the thermistor's time constant and thermal impedance can be calculated by equating the yield equation to (9), which is presented in (12).

$$\frac{R_{thr}}{\tau_{thr}} e^{-\frac{t}{\tau_{thr}}} + R_{ext} = 1.23 * e^{-0.25t} + 12.4 \tag{12}$$

By comparing both sides of (12), τ_{thr} equals 4 s (which is fairly matching the existing application note on NTC thermistors presented by Vishay in [24], R_{thr} equals 4.92 °C/W, C_{thr} equals 813 mJ/°C, and an external thermal resistance (referred to as R_{ext}. in Fig. 1(b)) is 12.4 °C/W.

To calculate the thermal impedance between the DUT's junction channel and the thermistor, the impedance ($Z_{\text{j-thr}}$), which is depicted in Fig. 1(b), can be extracted by subtracting the experimental thermistor measurement curve from the R_{DSon}-based estimated junction temperature curve ($T_{\text{j-RDSon}}$) according to (13).

$$Z_{j-thr}(s) = \frac{T_{j-R_{DSon}}(s) - T_{thr}(s)}{p_d(s)}$$

where

$$Z_{j-thr}(s) = Z_{PCB}(s) + Z_{jc}(s)$$

and

$$T_{j-thr}(s) = T_{j-R_{DSon}}(s) - T_{thr}(s) \tag{13}$$

and $T_{\text{j-thr}}$ is the thermal response function between the junction channel of the GaN DUT and the thermistor, Z_{PCB} is the PCB thermal impedance, and Z_{jc} is the GaN DUT junction to case thermal impedance as depicted in Fig. 1(b). From the experimental measurements shown in Fig. 3, the junction temperature is measured from I^2R_{DSon} measurements and used with the thermistor-measured thermal response function as in (13) to extract the junction-to-thermistor thermal response function ($T_{\text{j-thr}}$). Then, $T_{\text{j-thr}}$ is fitted using MATLAB curve fitting tools, which generates the constants a, b, c, d, g, and the R^2 value corresponding to a model's goodness of fit. The $T_{\text{j-thr}}$ curve is best fitted with a type-II exponential function with a statistical R^2 value of 0.964 as represented in (14).

$$T_{j-thr}(t) = a * e^{-bt} + c * e^{-dt} + g \tag{14}$$

The constants a, b, c, d, and g equal 5.662, 4, 288.8, 8, and 22.6, respectively. Based on the (8), thermal impedances Z_{jc} and Z_{PCB} can be expressed as in (15).

$$Z_{PCB}(s) = \frac{T_{jc}(s) - T_{thr}(s)}{p_d(s)}$$

and

$$Z_{jc}(s) = \frac{T_j(s) - T_{jc}(s)}{p_d(s)} \tag{15}$$

where T_{thr}, T_{jc}, and T_{j} are denoted in Fig. 1(b). By substituting (15) in (13), taking the inverse Laplace transformation of the yield equation, the PCB and GaN DUT thermal time constants and impedances can be calculated by equating the yield equation to (14) – as expressed in (16).

$$\frac{R_{jc}}{\tau_{jc}} e^{-\frac{t}{\tau_{jc}}} + \frac{R_{PCB}}{\tau_{PCB}} e^{-\frac{t}{\tau_{PCB}}} + R_{int} = 5.662^* e^{-4t} + 288.8^* e^{-8t} + 22.6 \tag{16}$$

R_{int} is an additional thermal resistance contributing to the PCB's thermal impedance, as Fig. 1(b) denotes. By equating both sides of (16), τ_{jc} equals 250 ms, R_{jc} equals 1.4155 °C/W, C_{jc} equals 177 mJ/°C, the thermal time constant of the PCB (τ_{PCB}) is 125 ms, and the corresponding thermal

TABLE 1. A Summary of the Thermal Time Constant and Impedance Values Involved in the Hardware Setup of the GaN DUT Junction Temperature Measurement

Components	*Thermal time constant value*	*Thermal impedance*
GaN HEMT	250 ms	R_{jc} =1.4155 °C/W C_{jc} = 177 mJ/°C
PCB layout, including 20 vias underneath DUT	125 ms	R_{PCB} =36.1 °C/W C_{PCB} = 3.463 mJ/°C R_{int} =22.6 °C/W
Thermistor	4 s	R_{thr} =4.92 °C/W C_{thr} = 813 mJ/°C R_{ext} =12.4 °C/W

resistance and capacitance are 36.1 °C/W and 3.463 mJ/°C, respectively. The internal thermal resistance (referred to as R_{int}. in Fig. 1(b)) is 22.6 °C/W.

Comparing the thermal impedance and time constant values attributed to different parts of the hardware setup, as summarized in Table 1, it is evident that the thermistor's time constant dominates the equivalent thermal impedance circuit. Furthermore, other commercially available thermal sensors, like thermocouples, thermal cameras, etc., also have significantly high time constants for DUT T_{ja} measurements. Thus, the T_j measurement technique for GaN FETs under ATC tests needs to be critically assessed before the hardware design and setup.

III. EXPERIMENTAL RELIABILITY TEST PLATFORM: CONCEPT AND OPERATION

The experimental setup, illustrated in Fig. 4, is designed to facilitate the "plug-and-play" integration of multiple GaN boards onto a single measurement and power supply board, as shown in Fig. 4(a)–(c). Two identical hardware setups/boards are used to implement thermal cycling tests of 5 GaN devices per setup, as one setup is shown in Fig. 4(a). Both boards are set up in the same enclosure and connected to the same DC power supply and electronic load, as shown in the single-line diagram in Fig. 4(a) and (b). The measurement circuit's on-state voltage is attached to the GaN boards, as shown in Fig. 4(a). At the same time, dSPACE MicrolabBox acts as a control unit and instantaneous data acquisition system for online monitoring of the device's degradation process during the ATC tests, as shown in Fig. 4(b). In constant current mode, an electronic load is used to allow predefined DC current values to heat the DUT. Other power supply and measurement boards are utilized for current and V_{DSon} sensing circuits and thermistor signal amplification. The GaN devices are mounted on small boards for easy interchange between the ATC setup shown in Fig. 4(c) and the curve tracer every 1000 thermal cycles for assessment. R_{DSon} is monitored online during the

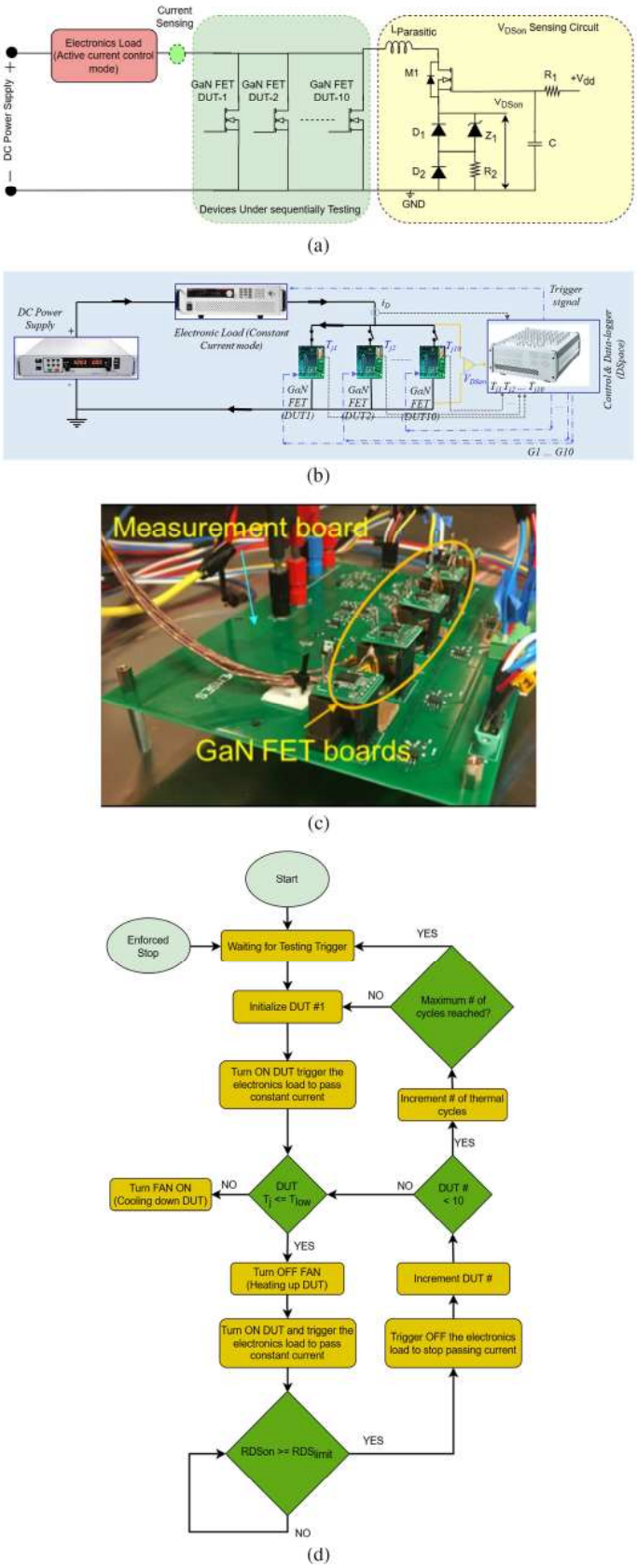


FIGURE 4. Experimental GaN FET degradation setup. (a) Testing circuit schematic. (b) Test block diagram, including the control unit. (c) Zoomed-in picture for a set of GaN FETs under test. (d) Testing flow chart.

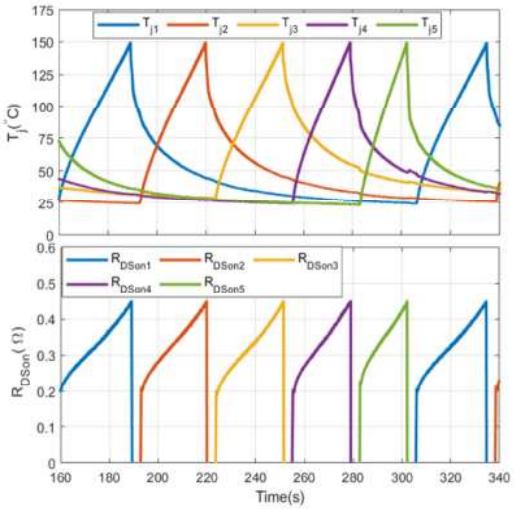


FIGURE 5. Simulation waveforms of sequential thermal cycling of multiple GaN DUTs under different DC current values under the same maximum thermal cycling windows.

ATC tests based on the V_{DSon} measurement circuit shown in Fig. 4(a), [25], [26]. The time taken for voltage-sensing is a few tens of nanoseconds, and the measurement error is within ±10 mV. The R_{DSon} for the DUT is calculated online during each thermal cycle to achieve a fast and accurate estimation of T_j for the GaN FETs to control the ATC window preciously.

The testing flow chart shown in Fig. 4(d) demonstrates the sequential thermal cycling of 10 GaN FET boards following the devices assigned identification number in the control algorithm. The test control is implemented in dSPACE MicroLabBox (1202), which includes measurements, calculations, or control of the following: i) R_{DSon} values continuously, ii) over-voltage/current protections, iii) control of PWM (or on and off states), iv) fans to cool down the device temperature during the off time of the thermal cycles, v) setting the DC current value in the electronic load (used to heat the devices), vi) R_{DSon} threshold and limit values, and vii) the number of the thermal cycles to be executed. Once the first DUT starts heating up and the R_{DSon} limit (or estimated T_j limit) is reached, the DUT is turned off. No heat sink is used in the GaN FET boards to ensure self-heating of the DUT with a DC current and accurately estimate the heat dissipated in the channel caused by the conduction loss. Once the first DUT is turned off after completing the heating time, it starts cooling down naturally. While the first DUT enters the cooling mode, the second DUT is activated to perform thermal cycling per its pre-set R_{DSon} low and limit values as depicted in Fig. 5. Once the maximum junction temperature is reached, that device is turned off. Following this operation pattern, multiple devices are sequentially thermally cycled using the same testing setup. When a DUT fails, the control algorithm triggers an alarm signal on the dSPACE platform and bypasses the device to proceed with the remaining devices.

The testing configuration allows sequential active thermal cycling for multiple GaN devices simultaneously, as depicted

TABLE 2. Thermal Cycling Test Conditions and GaN DUT Specifications [20]

Parameters	*Specifications/descriptions*
Operation	• ATC by DC current. • T_j measurements: Thermocouple and R_{DSon}-based estimation approaches. • $I_{DC,\ heating}$ = 2.5 A (heating current). • $ATC = t_{heating} + t_{cooling}$. • No heatsink is being attached to the DUTs.
Thermal cycling window and corresponding heating DC average current	• R_{DSon} limit = 500 mΩ, corresponding to T_j to 170 °C, $t_{heating}$ = 18 s, and $t_{cooling}$ = 54 s - for fresh device. • R_{DSon} limit = 550 mΩ, corresponding to T_j of 185 °C, $t_{heating}$ = 22 s, and $t_{cooling}$ = 63 s - for fresh device. • R_{DSon} limit = 575 mΩ, corresponding to T_j of 190 °C, $t_{heating}$ = 25 s, and $t_{cooling}$ = 70 s - for fresh device. • R_{DSon} limit = 600 mΩ, corresponding to T_j of 200 °C, $t_{heating}$ = 27 and $t_{cooling}$ = 85 s - for fresh device. • Each group of 2-3 GaN devices under test is ATC from R_{DSon} low level of 180 mΩ corresponding to room temperature of 25 °C (for fresh device) to R_{DSon} limits mentioned above.
e-mode GaN HEMTs under test (rated values)	• $V_{DS\text{-}blocking}$ = 650 V • $I_{D\text{-}continuous}$ = 7.5 A at 25 °C case temperature • R_{DSon} = 180 mΩ at 25 °C T_j • Regulated voltage for the integrated gate driver circuit = 6 V • QFN package

in Fig. 5. Each GaN DUT is heated up to a predefined thermal cycle limit one after the other by injecting DC current (i.e., I_D) and according to the ATC specifications listed in Table 2. Fig. 5 presents thermal cycling waveforms from simulation results, showcasing the use of various DC values of heating currents considered to perform the same thermal cycle window across several GaN devices. The higher the DC current used for generating the heat inside the GaN DUT (i.e., R_{DSon5}), the shorter the heating time for the devices to reach the thermal cycling window boundary. Active thermal cycling allows achieving the desired ΔT_j by adequately selecting the heating current and the heating time of the ATC. This type of calibration is performed at the beginning of the experiment to ensure that the measurements are properly monitored throughout the long-wear-out phenomenon) is compensated by adjusting the thermal cycling window ($T_{j\text{-}low}$ and $T_{j\text{-}limit)}$, which is referred to as term degradation testing. In order to keep the ΔT_j value constant or within a limited range of variation throughout the degradation process, the increase of R_{DSon} (due to the R_{DSon} low and R_{DSon} limit in Tables 2 and 3) every thousand thermal cycle count. The ΔT_j value is a crucial parameter in determining the lifetime of power components [27], [28]. Its increase causes a faster degradation,

TABLE 3. Extracted R_{DSon} Limit for a Fresh Device and Used for GaN HEMTs T_j Estimation.

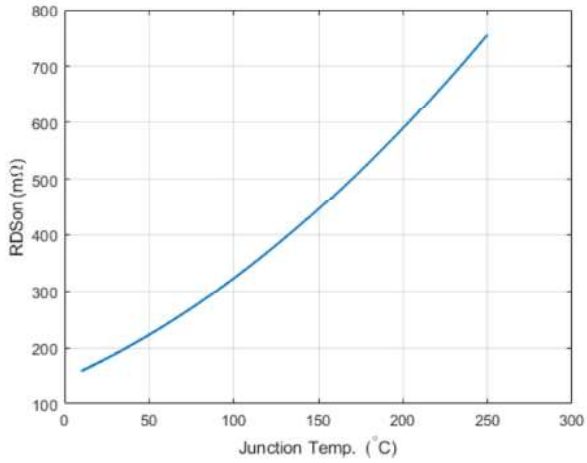
R_{DSon} Limit (mΩ)	Estimated T_j (°C)
180	25
450	150
500	170
550	185
600	200

leading to a relatively smaller number of cycles to failure. It is worth noting that the heating time also affects the lifetime of power components, even if to a lower degree with respect to ΔT_j.

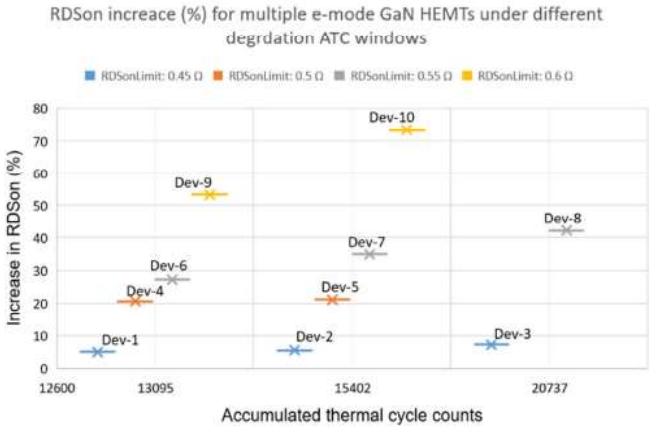
The R_{DSon} relationship with the T_j of GaN HEMTs is extracted by soaking the GaN DUT in a thermal chamber at different temperatures for around 30 minutes before measuring the R_{DSon}. Then, a 1A/120 μs pulse width current pulse is applied to the DUT, and the V_{DSon} is measured to calculate the corresponding R_{DSon}. Thus, the pre-experimental extraction of the R_{DSon} relationship with T_j is illustrated in Fig. 6(a) and summarized in Table 3 for a fresh GaN device (i.e., not degraded). The base R_{DSon} value of every thermal cycle is ∼180 mΩ (as presented in Table 2), the devices' R_{DSon} and represents the room temperature (i.e., 25 °C). Multiple maximum/limitR_{DSon} values are used for various devices under ATC, as shown in Fig. 6(b) – where the R_{DSon} limit defines the maximum temperature of the thermal cycle assigned for each device. For ten individual e-mode GaN HEMTs under tests, the accumulated increase in the R_{DSon} with respect to thermal cycling counts are clearly depicted that the devices with less thermal stress (Dev-1, Dev-2, and Dev-3) experienced much less increase in the R_{DSon} compared to the devices with high thermal stress (Dev-9 and Dev-10). After about every 1000 thermal cycles, the R_{DSon} threshold and limit values are recalibrated (shifted up) according to the permanent increase of the device's R_{DSon} caused by the degradation with the aging time presented in Fig. 6(b).

The R_{DSon} measured at room temperature (25 °C) and the accumulated change in the degradation process of multiple GaN HEMTs with more than 18 k thermal cycles (where the total heating time is about 250 hours, and the cooling time is about 750 hours) are shown in Fig. 7. The most stressed devices have an R_{DSon} limit value of 600 mΩ (or 200 °C T_j), while for the least stressed devices, it is 450 mΩ (or 150 °C T_j). The R_{DSon} values of the devices increase almost linearly against the number of thermal cycles.

It is important to understand the variation of R_{DSon} values at different temperatures before and after aging with ATC thermal cycling profiles. Four similar groups of devices (3 stressed with thermal cycling degradation and one reference for benchmarking) are considered for characterization with different stress levels, as labeled below.



(a)



(b)

FIGURE 6. Change in R_{DSon}. (a) Experimentally extracted the relationship between the R_{DSon} and junction temperature of GaN HEMTs at a V_{GS} of 6 V internally regulated according to the supplier recommendations in the datasheet [19]. (b) Percentage increase in R_{DSon} for multiple devices under ATC testing with thermal cycling counts under different ATC windows (room temperature to R_{DSon} limit/max labeled in the graph).

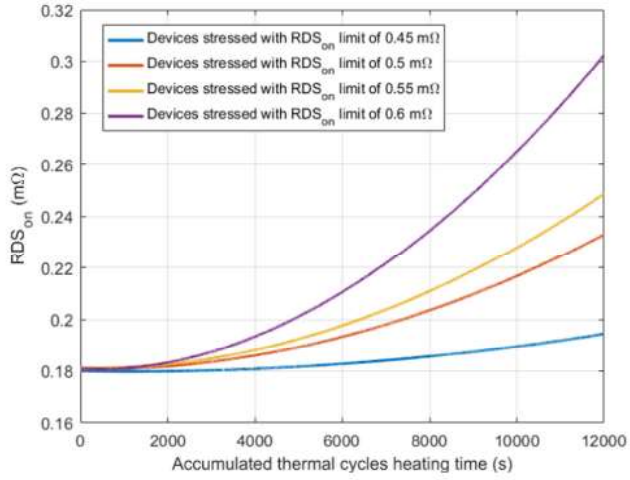


FIGURE 7. Experimentally fitted curve of R_{DSon} versus accumulated heating time of thermal cycles performed per device.

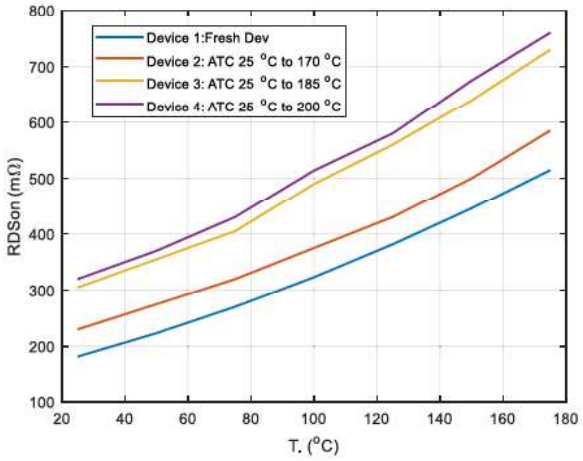


FIGURE 8. R_{DSon} versus junction temperature curves for multiple devices degraded with different thermal cycling windows – captured after about 18k thermal cycles per device.

- Device 1: Fresh device (zero thermal cycles) which has not been placed in thermal cycling testing.
- Device 2: Fairly degraded devices (30% increase in R_{DSon} after about 18k thermal cycles) with thermal cycling window of (25 °C to 170 °C).
- Device 3: Fairly degraded devices (60% increase in R_{DSon} after about 18k thermal cycles) with thermal cycling window of (25 °C to 185 °C).
- Device 4: Fairly degraded devices (75% increase in R_{DSon} after about 18k thermal cycles) with thermal cycling window of (25 °C to 200 °C).

Each group of devices (labeled in Fig. 8 as Device 1, Device 2, Device 3, and Device 4) consists of 2-3 individual GaN devices that undergo the same ATC testing conditions (i.e., heating current and heating and cooling times as shown in Table 2). The R_{DSon} versus junction temperature curves for the devices under test are extracted by soaking the devices in the thermal chamber for about 30 minutes at each junction temperature presented in Fig. 8. Then, a DC current pulse of 1A and 120 μs pulse-width is applied to measure the R_{DSon} per each temperature setting. The measured R_{DSon} curves are presented in Fig. 8. It can be noticed that the fresh device (Device 1) reached an R_{DSon} value of 500 mΩ at a T_j value of 170 °C, whereas the fairly degraded device (Device 2) reached an R_{DSon} value of 500 mΩ at a T_j value of 150 °C. Hence, when it is needed to maintain the junction temperature cycling window fixed during the degradation process (where T_j is estimated based on the R_{DSon} measurements), the R_{DSon} limit needs to be adjusted after every certain number of thermal cycles according to a newly extracted R_{DSon} vs. T_j curve with the aging time.

The results showed matching characteristics for each group of devices under each thermal cycling window performed for those particular devices. The percentage of the R_{DSon} increase per each thermal cycling window can be due to various degradation mechanisms that become more pronounced with continued thermal cycling, such as prolonged thermal cycling

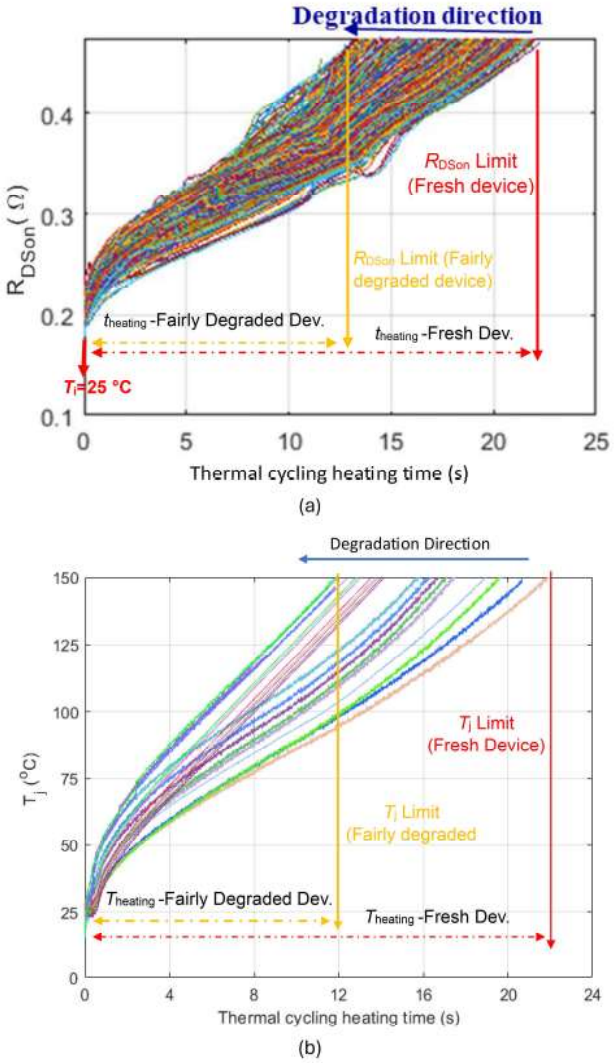


FIGURE 9. GaN devices' thermal cycling characteristics for two devices. (a) Multiple thousands of R_{DSon} curves for a GaN DUT were measured at different accumulated thermal cycle counts under a fixed R_{DSon} limit of 0.475 Ω. (b) Estimated T_j – based RDS_{on} limit operation for thermal cycling of DUT to keep the T_j window in the range of ~25 °C to ~150 °C; the R_{DSon} limit is adjusted according to R_{DSon} change measured at 25 °C with aging after about every thousand thermal cycle counts.

can lead to the formation of new defects, which can scatter carriers and increase resistance; high temperature can cause metal contacts between the die and the device package surface to diffuse, potentially changing the contact resistance; and degradation of passivation or insulation layers which can degrade over time, leading to increased surface leakage currents or trapping of carriers.

A detailed physical analysis of the device before and after thermal cycling may be required to pinpoint the underlying mechanisms. It often involves a combination of the factors mentioned above and can also be influenced by the specifics of the device structure, fabrication process, and the materials used. Furthermore, preliminary X-ray imaging of GaN DUTs is provided next, highlighting the possible degradation mechanisms induced. Fig. 9 shows the R_{DSon} curves during

the heating time for thousands of ATC for two devices with almost the same stress level, where Fig. 9(a) is a device operated under a fixed R_{DSon} limit of 0.475 Ω, while Fig. 9(b) is a device operated with fixed T_{j} limit (via adjusted R_{DSon} limit) to keep the T_{j} window in the range of ∼25 °C to ∼150 °C. The starting point of the R_{DSon} curves presents the R_{DSon} value at room temperature (i.e., the starting point of the thermal cycle), as shown in Fig. 9(a). It can be observed that the R_{DSon} value at room temperature increases with age. Additionally, the results in Fig. 9(a) reveal that the heating time taken for the R_{DSon} to reach a specific limit (i.e., R_{DSon} -limit of 0.5 Ω) decreases with the aging of the device. To represent it in a different way, T_{j} is calculated based on the R_{DSon} measurements, as shown in Fig. 9(b), the heating time for the GaN device from room temperature (about 25 °C) to a T_{j}-limit (here, 150 °C) gets reduced with the aging of the device. Hence, T_{j} transient time from room temperature to a specific temperature threshold under a certain mission profile can also be considered a potential alternative for the device's health monitoring. The change in the T_{j} transient time might be caused not only by the higher R_{DSon} and corresponding higher power losses in the aged device, but also by a higher resistance caused by solder degradation. Furthermore, higher resistance can also be caused by bond wire degradation. The degradation characterization here is fully packaged individual GaN DUT's degradation where the packaging, bond wires, metallic contacts, and other degradation mechanisms are inherited. It is worth noting that the ATC tests affect the aging of the wire bonds, packaging, etc., in addition to the dies, which cause faster degradation of the overall device, as captured in this research.

IV. ANALYSIS OF THE AGING CHARACTERISTICS OF THE DUTS' TEMPERATURE COEFFICIENT OF ON-STATE RESISTANCE

Another study is conducted considering the devices characterized in Fig. 8 with different aging profiles to assess the variation of the DUTs' temperature coefficient of on-state resistance (R_{DSon}). The R_{DSon} temperature coefficient (α) for each device is calculated at the beginning of the ATC (thermal cycle count < 50 cycles) and after the DUTs are fairly degraded (∼18k thermal cycles), as shown in Fig. 10. The temperature coefficient of resistance (R_{DSon}) of each device can be calculated using (17).

$$\alpha = \frac{\left(\frac{R_{DSon-\max} - R_{DSon-25C}}{T_{j-\max} - T_{j-25C}}\right)}{R_{DSon-25C}} \tag{17}$$

where $R_{\mathrm{DSon-max}}$ is the $R_{\mathrm{DSonlimit}}$, $R_{\mathrm{DSon-25C}}$ is the R_{DSon} measured at 25 °C, $T_{\mathrm{j-max}}$ is the junction temperature measured at R_{DSon} − limit, T_{j} − 25C is the room temperature where R_{DSon} − 25C is measured. It can be noticed that the devices have slightly different R_{DSon} thermal coefficients at the beginning because the devices start from R_{DSon} slightly different from the datasheet value measured at room temperature (i.e., 25 °C), and the net 'α' value of the FET is a result

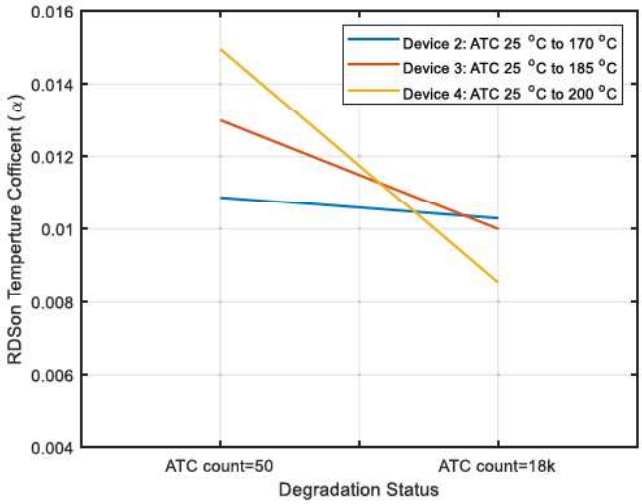


FIGURE 10. R_{DSon} thermal coefficient for multiple devices at two degradation statuses: low thermal cycles and relatively degraded stage with about 18k thermal cycles count.

of different elements in the components. However, according to each device's assigned thermal cycling window limit, the R_{DSon} temperature coefficient tends to decrease with the DUT aging. Furthermore, the higher the peak thermal cycling temperature, the higher the slope of the R_{DSon} temperature coefficient, as seen in Fig. 10. In other words, the temperature coefficient decreases with the aging of the device according to the thermal coefficient equation (i.e., (17)) as '$R_{\mathrm{DSon\ -25C}}$' increases with the aging time of the devices under test- caused by mechanical and electrical degradation mechanisms of the fully packaged GaN DUTs. The larger the thermal cycling window (higher ΔT_{j}), the more slope of α is observed, as shown in Fig. 10.

For a GaN DUT degraded with a thermal cycle window of 25 °C to 185 °C and after several months of continuous thermal cycling tests where the number of cycles reached about 18k, 3D X-ray Microscopy with nanoscale resolution capability (model SKYSCAN 2214) is used to construct the 3D model of the GaN DUT, as shown in Fig. 11(a). The dimension of the smallest past observed from the 3D model of the GaN DUT is 40 × 30 μm^2. For a fresh GaN device where no thermal cycles have been carried out, the micro-CT scanner image, as presented in Fig. 11(b), which is sliced from the 3D model, clearly shows no voids. After 18k thermal cycles, the CT scanner of the GaN DUT shows significant voids and de-lamination development, as shown in Fig. 11(c). While the research considered single e-mode GaN HEMTs for testing as fully packaged individual GaN DUTs, separation of the degradation mechanisms (electrical and mechanical) is complicated, and both are inherited in the measurements with no separation. According to initial failure analysis imaging of the GaN devices considered in the research, the increase in the R_{DSon} is expected to be caused by the die-attach de-lamination and possibly bond-wire cracking, which is not clear in the 3D constructed model, as similar degradation for other devices reported in [29] and [30]. Some voids are observed under the

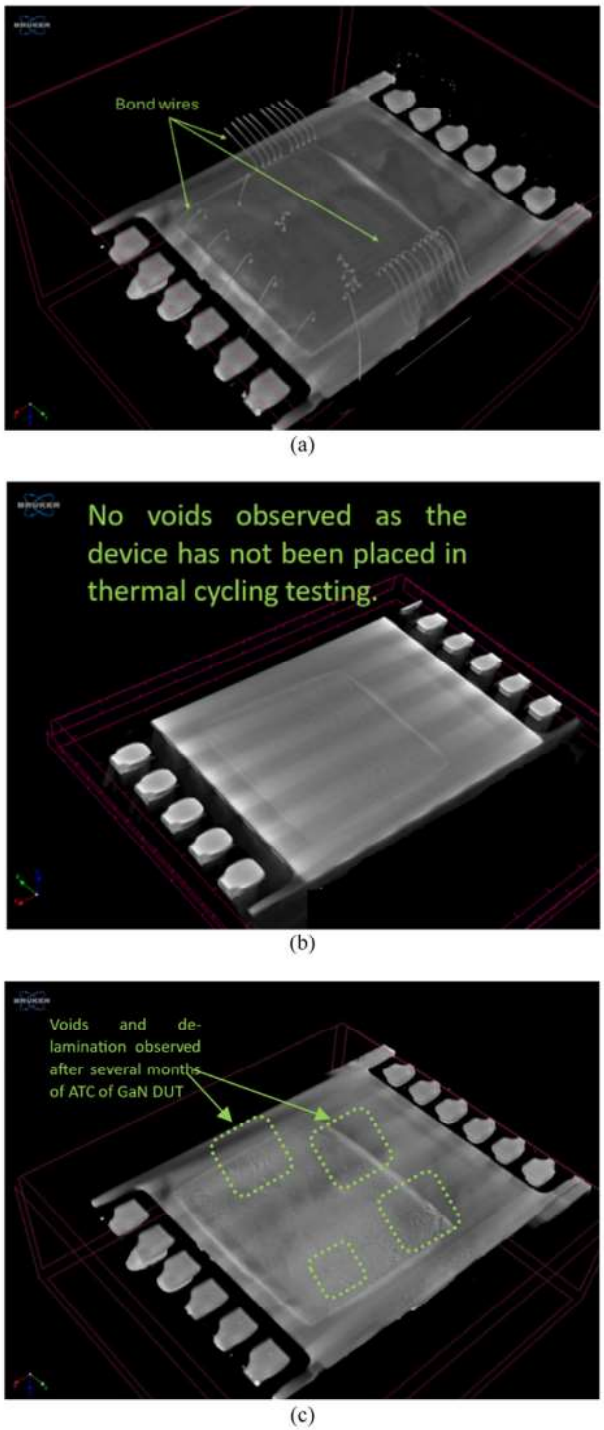


FIGURE 11. 3D X-ray micro CT imaging for a GaN FET. (a) 3-D model showing the internal bond wires within the DUT. (b) A fresh device (zero thermal cycles) has not been placed in thermal cycling testing. (c) Fairly degraded devices (60% increase in RDSon after about 18k thermal cycles) with thermal cycling window of (25 °C to 185 °C).

die area. Consequently, the area of contact for heat conduction has decreased, resulting in a decrease in the thermal dissipation performance of the device with aging. This will contribute to higher T_j for the operation of an aged device, assuming that the power dissipation and the ambient temperature remain fixed, as shown in Fig. 9(b), where the heating time for the GaN device from room temperature (about 25 °C) to a T_j-limit (here, 150 °C) gets reduced with aging.

Thermal cycling stresses the DUT due to mismatched coefficients of thermal expansion (CTEs) among packaging layers, leading to mechanical stresses from different expansion rates caused by self-heating effects (conduction losses). This results in solder joint cracks and wire bond lift-offs, with the degradation observable through changes in on-state resistance and thermal resistance, as noted in references [7] and [31], [32], [33], [34], [35]. An increase in the switching power devices' thermal resistance and R_{DSon} due to void formation in the die-attach solder, as evidenced by X-ray and scanning acoustic imaging, indicates degradation over stress time [36]. The fast power cycling (the time is in the order of tens of seconds) and higher temperature swing ($\Delta T > 100$ K) leads to wire-bond failure, while slow power cycling (the time is in the order of minutes) and lower temperature swing ($\Delta T < 80$ K) leads to solder fatigue related failures [7]. The abovementioned degradation mechanisms are mainly triggered by the temperature cycling, but they are also affected by the average temperature and the heating time.

V. COMPARATIVE ANALYSIS AND DISCUSSIONS

A comparative study of parametric changes in relevant Si-based power devices with almost the same power rating is provided in Table 4. However, some detailed information about the thermal cycling profiles for the results presented in [14] and [37], [38]. Typically, the higher ΔT_j is, the more are the electrical parametric changes and failures reported. Comparing Si MOSFET degradation data presented in [37] to the GaN devices presented in this research, it can be noticed that a significant increase in the R_{DSon} has been observed in Si MOSFET for almost the same ATC profile ($t_{heating}$, $t_{cooling}$ and ΔT_j) and device power ratings under much less thermal cycle counts performed for the Si MOSFET. Similarly, Si IGBT thermal cycling results in a much higher increase in the on-state voltage drop, as presented in [37], compared to the GaN HEMTs considered in this research for almost the same ATC profile and device power ratings. Thermal cycling tests of SiC MOSFETs are presented in [38]. The results show that SiC MOSFETs have longer R_{DSon} stability for a period of time before starting to increase drastically compared to the GaN devices considered in this research, as reported in Fig. 6(b). This difference might be associated with the devices' packaging and the material's thermal properties. Comparing E-mode GaN HEMTs' degradation results presented in [14] to the GaN devices considered in this research under the same ATC profile, almost similar changes in R_{DSon} have been reported. Cascode GaN device (Si MOSFET and GaN HEMT) results show a minor increase in the R_{DSon} after significant thermal cycles count – compared to Si MOSFET, GaN HEMT, SiC MOSFET, and Si IGBT. It is reported that the change in R_{DSon} of Cascode GaN device is insignificant with the V_{gs}. This may be implying that the R_{DSon}

TABLE 4. Comparative Parametric Changes of Si and GaN-Based Devices Under Thermal Cycling Tests

Ref	DUT	Thermal cycling condition	Observation
[37]	• Power Si MOSFET • Rated DC blocking voltage/ DC current are 400V/11A • R_{DSon} = 350 mΩ at ambient temp.	ΔT_j = 130 °C (50-180 °C), $t_{heating}$ = 20s, and $t_{cooling}$ = 40s	Increase in R_{DSon} ~ 66% after 2.7k thermal cycles count
	• Si IGBT • Rated DC blocking voltage/ DC current are 1200V/11A	ΔT_j = 180 °C (40-220 °C), $t_{heating}$ = 20s, and $t_{cooling}$ = 40s	Increase in on-state voltage drop ~ 27% after 1.6k thermal cycles count
[38]	• SiC Power MOSFET in SOT-227b package • Rated DC blocking voltage/ DC current are 1200V/68A	ΔT_j = 90.5 °C (30-120.5 °C), and heating current = 22.5A DC	Increase in R_{DSon} ~ 7% after 20k thermal cycles count, but it is increased by ~ 107% after 50k thermal cycles count
	• R_{DSon} = 34 mΩ at ambient temp. (i.e., 25 °C)	ΔT_j = 70.5 °C (50-126.5 °C), and heating current = 22.5A DC	Barely increase in R_{DSon} after 50k thermal cycles count
[14]	• E-mode GaN HEMT (p-GaN gate) • DC blocking voltage/ DC current are 650V/30A • R_{DSon} = 50 mΩ at ambient temp. • GaN Systems package	ΔT_j = 125 °C (25-150 °C)	Increase in R_{DSon} ~ 10% after 28k thermal cycles count
	• Cascode GaN device (Si MOSFET and GaN HEMT) • DC blocking voltage/ DC current are 650V/36A • R_{DSon} = 60 mΩ at ambient temp. • TO-247-3 package.	ΔT_j = 125 °C (25-150 °C)	Increase in R_{DSon} ~ 8% after 500k thermal cycles count
Proposed Research	• E-mode GaN HEMT with an integrated gate driver • Rated DC blocking voltage/ DC current are 650V/7.5A • R_{DSon} = 180 mΩ at ambient temp. (i.e., 25 °C) • QFN package	ΔT_j = 125 °C (25-150 °C), heating current = 2.5A DC, $t_{heating}$ = 15s, and $t_{cooling}$ = 45s	Increase in R_{DSon} ~ 8% after about 20k thermal cycles count
		ΔT_j =150 °C (25-170 °C), heating current = 2.5A DC, $t_{heating}$ = 18s, and $t_{cooling}$ = 54s	Increase in R_{DSon} ~ 21% after about 15k thermal cycles count
		ΔT_j = 160 °C (25-185 °C), heating current = 2.5A DC, $t_{heating}$ = 22s, and $t_{cooling}$ = 63s	Increase in R_{DSon} ~ 41% after about 22k thermal cycles count
		ΔT_j =165 °C (25-190 °C), heating current = 2.5A DC, $t_{heating}$ = 27s, and $t_{cooling}$ = 85s	Increase in R_{DSon} ~ 72% after about 17k thermal cycles count

change is reasonably affected by package-related degradations in addition to the channel degradation. However, for the GaN HEMTs, the increase in the R_{DSon} is significant as V_{gs} gets reduced. Therefore, channel resistance mainly contributes to the increase in GaN HEMTs' net on-resistance with aging time.

VI. CONCLUSION

A framework for analyzing the characteristics of accelerated thermal cycling (ATC) test setup is presented in this paper, along with an evaluation of the effects of non-linear dissipated power-based degradation profiles in e-mode GaN HEMTs' channels. The proposed thermal modeling method can also be applied to other switching devices operating under accelerated thermal cycling tests – to model the thermal impedance and calculate the thermal time constant of the components involved in the measurement of T_j. The modeling is based on the experimental GaN HEMT DUTs' junction-ambient temperature measurements. The analysis shows that the thermistor-based DUT junction temperature monitoring method suffers from a significant time constant of the thermistor's time constant (i.e., 4 s). Thus, an indirect approach using R_{DSon} measurements is utilized to calculate the DUT's junction temperature. Therefore, a wide range of thermal cycling tests were conducted with almost no failure/ thermal runaway experienced on the DUTs compared to adapting traditional thermal sensors (like thermistors) available in the market. The experimental tests, including the characterization of the DUT using the power device curve tracer, validated the R_{DSon}-based T_j estimation method - in terms of its concept, operating principle, and performance. This method shows a promising approach suitable for the reliability assessment and in-situ health monitoring of GaN devices and the encompassing power converters.

A comparative study of parametric changes in relevant Si-based power devices with almost the same power rating was presented. Compared to Si MOSFET, SiC MOSFET, and Si IGBT, GaN HEMTs experienced less increase in the R_{DSon} with aging under ATC. However, SiC MOSFETs have longer thermal stability where very minor increases in the R_{DSon} were reported for a long period at the beginning of the ATC time.

The experimental results highlight an alternative aging indicator during device degradation, i.e., the T_j rise time from the base temperature to the T_j steadily decreases with the aging of the devices. It is a promising indicator for aging monitoring of semiconductor switching devices (including GaN). Moreover, the experiments also validated that the temperature coefficient of R_{DSon} resistance reduces with aging, and the rate of reduction is significantly related to the thermal stress applied.

The analysis of the temperature-coefficient of the R_{DSon} validated the devices aging, where the reduction in the temperature coefficient for GaN HEMTs can be partially attributed to

the increase in the conduction channel resistance, drain-source contacts degradation, and reduction in the electrons' density in the 2DEG channel as the devices age.

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