Improved Sensing Circuit for On-State Resistance Measurement of High and Low-Side GaN FETs

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***Abstract*— This paper presents an improved on-state resistance (RDS_{on}) measurement scheme for high and low-side GaN FETs, which is critical for reliable and precise assessment of GaN HEMT power devices' lifetime and degradation patterns. The proposed circuit is based on an active voltage clamp using Si MOSFET and Schottky and Zener diodes. The proposed circuit features lower parasitic inductances and capacitances by replacing the Si MOSFET with e-mode GaN FET. This modification contributed to much lower ringing and spikes in the voltage and current waveform of both the measurement FET and the DUT. The absence of an embedded body diode in the GaN device in the measurement circuit allows zero reverse recovery operation, making it more viable in high-frequency power converters. This study also provides a detailed design analysis of a bootstrap GaN-based on-state voltage (VDS_{on}) sensing scheme for high-side FETs, useful in multiple converter configurations for in-situ devices' health monitoring and conditioning. Simulation and experimental results validate the performance and features of the proposed concepts.**

Keywords*— Gallium Nitride (GaN) devices, on-state voltage measurement, dynamic on-state resistance, reliability, and bootstrap-based active clamp voltage.

I. INTRODUCTION

GaN FET-based power converters are advancing rapidly, offering higher power density and efficiency, improved lifespan, and robust reliability. However, due to limited historical data, industry stakeholders remain concerned about GaN device reliability, especially as charge-trapping effects can increase on-state resistance (RDS_{on}) over time [1-2]. Additionally, applications like automotive and aviation have spurred research into the high-temperature reliability of GaN FETs [3], as the GaN HEMTs devices experience reduced current conduction capability caused by the charge trapping phenomena, which increases the device channel resistance, which is essential for power converters design when considering efficiency and cooling system size.

For monitoring GaN HEMTs' aging/degradation, several common indicators (RDS_{on}, transconductance, the drain current (I_D), gate leakage current, and gate-source threshold voltage) were discussed in [4-6]. However, due to the accuracy and difficulties associated with the measurements of each health indicator, RDS_{on} is widely employed as a suitable parameter for monitoring aging/degradation [5-8]. Typically, the RDS_{on} of a GaN FET is determined by the device's I-V curve from the datasheet under a specific operating condition. However, RDS_{on} can be significantly affected by different operating conditions, and assessing it under various conditions is crucial for improving the reliability of GaN FETs.

A fast extraction method for dynamic RDS_{on} of GaN HEMTs was presented in [9-10]. This method used an active voltage clamping circuit to measure VDS_{on} and I_D. According to [11], high VDS_{on} measurement accuracy could be achieved via fast-switching diodes with small parasitic capacitances and a current mirror technique. The disadvantage of this approach is that a differential probe must be used for measurement. In [12-15], another high-speed VDS_{on} measurement circuit for GaN HEMTs was adopted. Although SiC diodes were employed to achieve fast sensing speed and reduce the overshoot in the measured VDS_{on}, the critical drawback of this technique is that the forward current of the sensing diode must be kept very low to prevent its temperature from increasing. As a result, this approach is challenging for practical, long-term reliability assessments.

Most of the presented electrical circuits for GaN HEMT devices' on-state voltage measurement are focused on bottom-placed (low-side) devices where the source of the FET is the same as the power ground. However, for online condition monitoring of power converters where high-side devices are used, it is challenging to adopt the same circuits due to isolation issues as the source of the high-side FET is not grounded. This paper offers a simple and effective method for measuring the RDS_{on} of GaN FETs under hard and soft-switching operating conditions, which can be easily implemented. The proposed circuit provides significant advantages over existing research, as it minimizes voltage spikes in the voltage/current waveforms of both the GaN device under test (DUT) and the FET in the measurement circuit. The proposed circuit employs a bootstrap-based active voltage clamp approach for on-state voltage measurement of both high and low-side FETs.

II. COMPARISON OF GAN FET'S ON-STATE VOLTAGE MEASUREMENT TECHNIQUES

The basic concept in the VDS_{on} measurement circuit is that when the DUT is ON, the measurement circuit is connected in parallel with the DUT; when the DUT is OFF, the measurement circuit gets disconnected from the DUT. In such an operation, the parasitic inductances and capacitances contributed by the circuit measurement's components and the connection between the measurement circuit and the GaN DUT play a significant role in superimposing ringing and spikes in the measurement circuit's components (including the measured VDS_{on}) and the GaN DUT – especially at high

switching frequency operation (or high di/dt involved in GaN DUT operation). Additionally, the speed of the measurement circuit should be fast enough to capture the VDS_{on} adequately. This section explores three VDS_{on} measurement circuits: (a) Current-mirror based VDS_{on} measurement, (b) diode-with-voltage-divider-based VDS_{on} measurement, and (c) FET-based VDS_{on} measurement.

Current-mirror based VDSon measurement circuit, shown in Fig. 1(a), uses a Wilson current mirror which consists of three BJTs, three resistors, five/more low voltage Schottky diodes, and two high voltage Schottky diodes. Wilson current mirror ensures the same current is supplied from the mirror circuit. The current flowing through the diodes (D_b and D_a) is the same. When the DUT (V_s is connected to the source and V_d is connected to the drain of the GaN DUT) is ON, the mirror current flows into DUT's drain and source through diodes D_a and D_b. Hence the voltage across the nodes (A and B) reflects the VDS_{on} of the DUT. When the DUT turns OFF, the diodes (D_a and D_b) block the high voltage; hence the currents from the Wilson mirror flow through the diodes (D_1 -to D_5). The voltage during the transient is clamped to the sum of forward voltage drops of D_1 to D_5. Based on the LTSpice simulation of the circuit using proper commercially available components, The measured VDS_{on} (i.e., V_{AB}) accurately traces the VDS_{on} of the GaN DUT. At the same time, there is a voltage spike during the turn-OFF. The measurement takes about 31.5 ns to track the VDS_{on} within ±10 mV error.

Diode-with-Voltage divider Rds-on measurement circuit, shown in Fig. 1(b), uses two Schottky diodes (D_1 and D_2), two Zener diodes (D_3 and D_4), with two voltage divider resistors (R_1 and R_2) and an *RC* filter. The GaN DUT's drain and source terminals are connected to nodes A and B. The VDS_{on} is measured across the resistor R_2. When the GaN DUT is OFF, the diode D_1 blocks the voltage, and the VDS_{on} (or V_s as labeled in the circuit) is clamped to the voltage divider value (V_{cc}*R_2/(R_1+R_2)). When the DUT turns ON, the diode D_1 conducts, and hence the sensed voltage (V_s) shows DUT's VDS_{on} in addition to the diode D_1 forward voltage. This additional diode voltage can be estimated using the V_s, V_{cc}, and I-V characteristics of the D_1. Proper selection of the components D_1, D_2, R_1, and R_2 ensures faster measurement of the DUT's VDS_{on} within 45ns. From the circuit simulation, the Sensed voltage (V_s) traces the VDS_{on} within an offset of the diode D_1 forward voltage drop. There are voltage spikes at the sensing node during the turning OFF of the DUT. The sensed node tracked the VDS_{on} within an offset of 886 mV and ±10 mV error due to diode voltage drop.

The FET-based VDS_{on} measurement circuit or the conventional VDS_{on} measurement circuit in the next section is shown in Fig. 1(c). The circuit operation is depicted in the next section. From the circuit simulation, the sensed voltage V_s accurately traces the DUT's VDS_{on} within 20.1 ns and ±10 mV measurement error. However, there are voltage spikes at the sensing node during turning ON and turning OFF of the DUT.

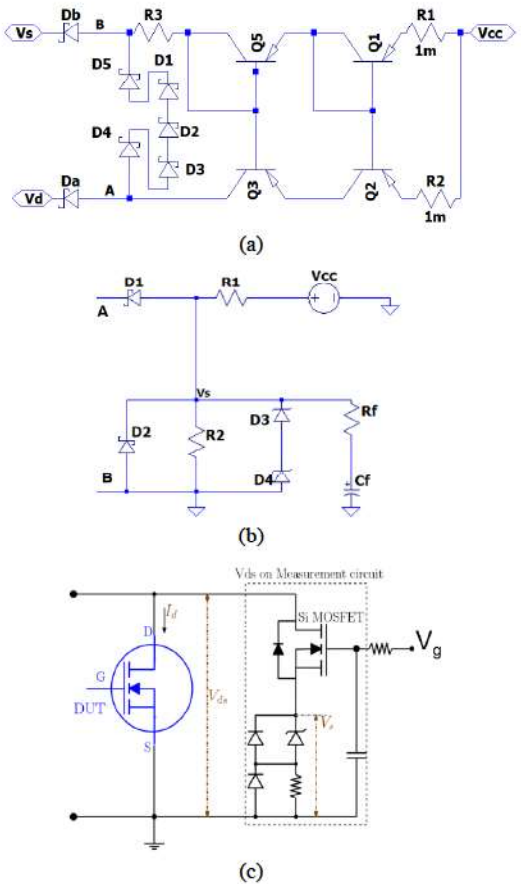


Fig. 1: On-State voltage measurement circuits. (a) Current-mirror-based VDS_{on} measurement circuit arrangement. (b) Diode-with-voltage-divider-based VDS_{on} measurement circuit. (c) FET-based VDS_{on} measurement circuit.

Table I: Comparison of three VDSon measurement circuits.

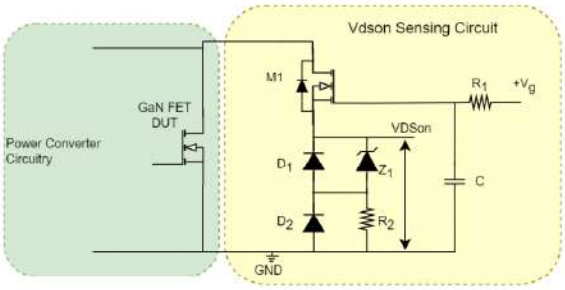
Components/ Performance indices	Measurement circuit		
	Current mirror based	Diode-with-Voltage-Divider based	FET based
Schottky diodes	Yes (7)	Yes (2)	Yes (2)
Zener diodes	No (0)	Yes (2)	Yes (1)
Additional source	Yes	Yes	Yes
Offset voltage	No	Yes (diode drop)	No
Simulated response time	31.5 ns	45 ns	20.1 ns
No. of BJTs/FETs	4	0	1

By comparing the three circuits' performance, the advantage of the current-mirror-based VDS_{on} measurement circuit is that it is temperature-independent as the sensed voltage is measured between identical diodes. However, the drawback is that the V_{AB} is a floating voltage with many components compared to other methods. Though the diode-with-voltage-divider-based circuit does not have any BJT or FET devices, the main drawback is that a diode voltage offset

needs to be subtracted and varies with the temperature. The FET-based circuit is simple and directly measures the VDS_{on} without any offset voltage. Components and performance-wise comparison of the three circuits are provided in Table I.

III. CONVENTIONAL GAN FETS' ON-STATE MEASUREMENT CIRCUIT OPERATION AND ANALYSIS

The conventional circuit used for measuring the on-state voltage of GaN FET is shown in Fig. 2(a). It consists of Silicon (Si) MOSFET, a Zener diode, two Schottky diodes, and resistors and capacitors. When the DUT is turned off, the source terminal voltage of the MOSFET (or the voltage node VDS_{on}) is clamped to (V_g – V_{gs} threshold voltage of the MOSFET), so the measured VDS_{on} is the Zener voltage (i.e., 5.1 V consider in this research). If the DUT is turned on, a low impedance path will be established between the DUT and the MOSFET; therefore, the MOSFET turns ON, and the DUT's VDS_{on} appears on the VDS_{on} node. For a proper selection of the components of this circuit, the MOSFET should withstand the OFF voltage that appears across the DUT. The MOSFET RDS_{on} should be higher than it is for the DUT, so the current will pass through the DUT, not the measurement MOSFET when both DUT and the MOSFET are conducted. The DC gate voltage (V_g) has to be slightly higher than the Zener diode voltage and the threshold V_{gs} of the measurement MOSFET. A capacitor of 10 nF is used across the gate-to-ground of the measurement MOSFET to stabilize the DC V_g. The Zener diode voltage should be a little higher than the threshold V_{gs} of the MOSFET. Both diodes (D1 and D2) have to be Schottky diodes with low output parasitic capacitance as much as possible. The resistor (R2) is a few tens of Ohm placed to



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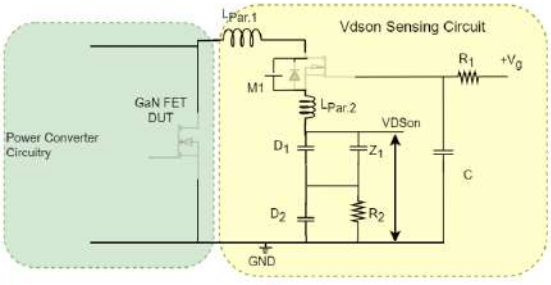
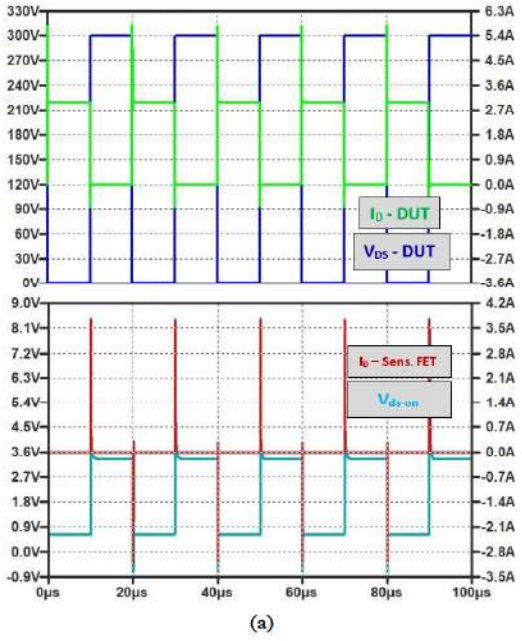


(b)

Fig. 2: Conventional circuit used for GaN FET *VDSon* measurement. (a) Circuit schematic. (b) Parasitic content in the circuit when both the DUT and the measurement MOSFET are OFF.



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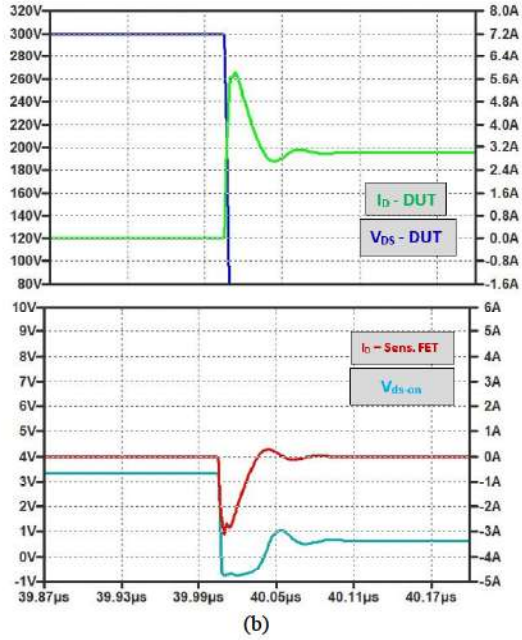


(b)

Fig. 3: Simulation voltage and current waveforms for the conventional GaN FET's VDS_{on} measurement circuit. (a) DUT current and voltage waveforms, drain current of the sensing FET, and the *VDSon*. (b)Zoomed-in waveforms.

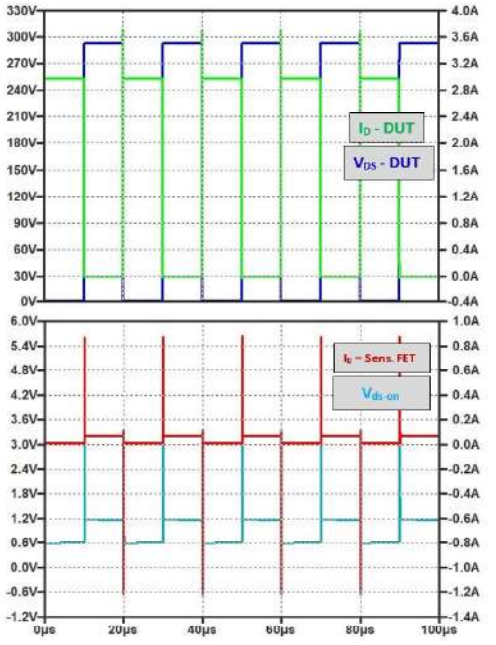
damp the imposed voltage ringing effects in the measured VDS_{on}, which is caused by the parasitic inductances and capacitances of the entire loop between the DUT and the measurement circuit (mainly measurement circuit connection, MOSFET, Zener diode, and the Schottky diodes) as shown in Fig. 2(b). The higher R2 is, the lower the ringing effects on the VDS_{on} and the higher the time delay for capturing the VDS_{on}. The DC V_g ranges between 6 to 8 v, based on the ringing results on the VDS_{on}, where the higher V_g increases the ringing effects on the VDS_{on}.

Switching ON and OFF of the DUT, the parasitic inductances and capacitances (shown in Fig. 2(b)) cause the charging and discharging of the components' capacitors (especially the Si MOSFET and the Schottky diodes) through the circuit inductances and resistances – this results in ringing and spikes in the measured VDS_{on} that can damage the measurement components as well as induce spikes and oscillation on the current waveform of the DUT, especially under hard switching operation, as shown in Fig. 3. The large output parasitic capacitance of Si MOSFET (M1) results in high voltage spikes at node VDS_{on} during DUT switching transitions. In other words, the smallest output capacitances of the measurement MOSFET and the Schottky diodes, the less ringing and overshoot appear on the measured VDS_{on} and voltage/current waveforms of the DUT. In addition, these diodes can cause a leakage current, which leads to a voltage drop across M1. Therefore, the hard switching operation of this circuit can significantly degrade the performance and lifespan of the GaN FET under long-term testing and reliability investigation.

To reduce the impact of the sensing circuit on the DUT as well as the oscillation in the measured VDS_{on}, M1 is substituted with another GaN FET. This modification significantly reduced the parasitic inductances and capacitance in the measurement circuit, which led to a significant improvement in switching transients' performance for both DUT and M1, even under hard-switching operation, as demonstrated in Fig. 4. The GaN FET used in the sensing scheme has significantly smaller parasitic inductances and capacitances. Using GaN FET in the measurement circuit, other circuit parameters are adjusted accordingly. The selected Zener diode is rated for 2.7 V, and V_g is 3 volts as the GaN FET has a lower V_{gs} threshold voltage compared to Si MOSFET. The resistor R2 is reduced as no high current flows through the Zener diode compared to the conventional circuit. It can be noticed from Fig. 3 and Fig. 4 that the overshot in I_D for the DUT is reduced from 86% to 20%. This modification reduces the sensing circuit's size and eliminates the reverse recovery phenomenon for the GaN DUT since the sensing FET has no body diode.

IV. PROPOSED BOOTSTRAP-BASED ON-STATE VOLTAGE MEASUREMENT CIRCUIT

Most of the presented circuits for measuring the VDS_{on} of the GaN FETs, including the circuit shown in Fig. 2, are mainly designed for low-side switches. For topologies with a high-side of source point of the FET floating, isolated power supplies, special differential sensing isolation, and other techniques have been adopted to measure the VDS_{on} of these switches. However, these approaches can make the sensing scheme complex, costly, and bulky and affect the performance of the DUTs. This paper presents a bootstrap-based VDS_{on} measurement circuit tested on an H-bridge DC-DC power converter as an example of power electronics topology with high and low-side FETs widely used for constructing various power converters. The proposed scheme of the bootstrap



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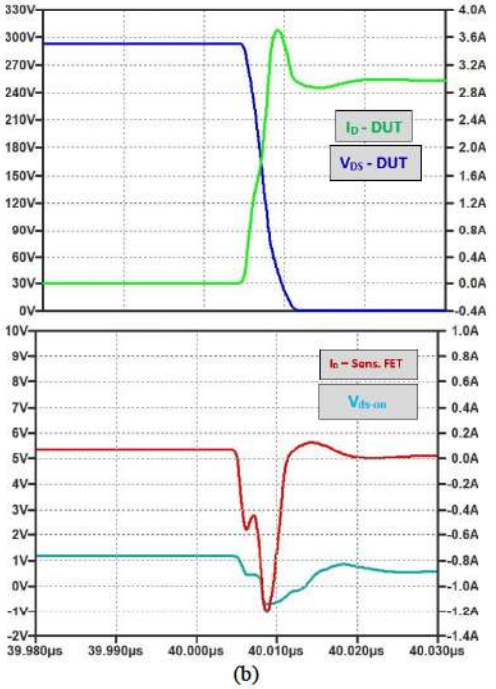


(b)

Fig. 4: Simulation voltage and current waveforms for the modified VDS_{on} measurement circuit with GaN FET in the measurement circuit. (a) DUT current and voltage waveforms, drain current of the sensing FET, and the VDS_{on}. (b)Zoomed-in waveforms.

circuit is depicted in Fig. 5. Since the bootstrap circuit is a well-established method/knowledge for powering the gate driver circuits of the high-side FETs, a similar concept is adopted for supplying the VDS_{on} measurement circuit across V_g and floating source node of the high-side FET, as shown in Fig. 5. This practice contributes to a size reduction of the measurement circuit and enhances the sensing scheme's reliability.

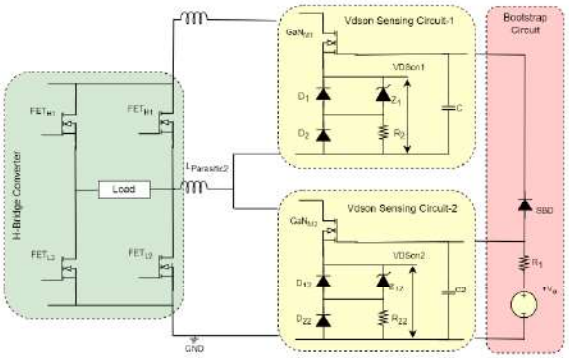
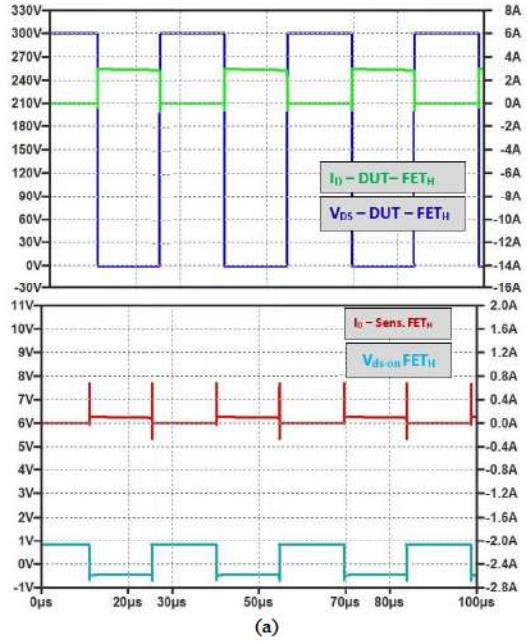


Fig. 5: GaN FET-based H-bridge with bootstrap voltage clamping circuit.

The operation of the proposed bootstrap-based VDS_{on} circuit is similar to that of a traditional bootstrap circuit. When the low-side FET is ON, the bootstrap capacitor (C) charges up through the Schottky barrier diode (SBD) limited by the resistor R1. When the low-side FET turns OFF, the bootstrap capacitor (C) powers up the high-side VDS_{on} measurement circuit. The waveforms of this operation are depicted in Fig. 6 for both the high-side and low-side GaN FETs under test. This measurement approach requires no voltage differential probs or isolated power supply for high-side FET VDS_{on} sensing.

V. HARDWARE SETUP AND RESULTS

The experimental setup for an accelerated thermal cycling test is depicted in Fig. 7. The testbed is a GaN-based H-bridge with four 650 V / 7.5 A e-mode GaN HEMTs with integrated driver circuits. The H-bridge is equipped with thermocouples, voltage, and current sensing circuits for continuous online monitoring of device degradation during the tests. Based on the VDS_{on} and I_D instantaneous measurement of individual GaN FETs, the RDS_{on} is calculated and correlated to the DUT's junction temperature. This process adopted wide thermal temperature cycling for faster degradation of the GaN FETs. More information on the degradation process is presented in [5,10]. A MicroLab Box DSpace (DS1102) unit is used to acquire the GaN device's performance. The conventional VDS_{on} measurement circuit is employed in the hardware setup. Fig. 8(a) shows the voltage and current waveforms for the GaN FETs during a single junction thermal cycle from 25 °C to 180 °C, with the switching frequency set to a few kHz to avoid issues raised by ringing/overshoots associated with high-frequency operation as well as to minimize the effect of hot-electrons trapping phenomena related to the GaN devices. Although the H-bridge converter is operated in hard switching, it can be noticed in Fig. 8(b) that the voltage and current waveforms are affected by ringing due to the VDS_{on} measurement circuit, even at a few kHz switching frequencies. Hence, the bootstrap-based VDS_{on} measurement method with GaN FET employed in the measurement circuit can help in reducing the spikes in the voltage and current waveforms of both the measurement FET and the DUT.



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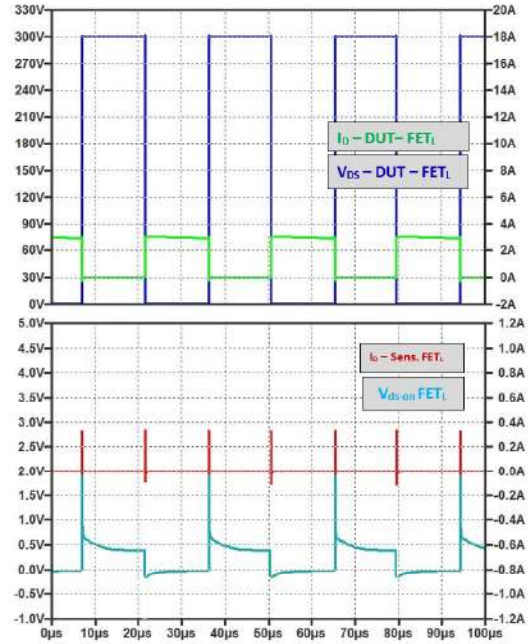


(b)

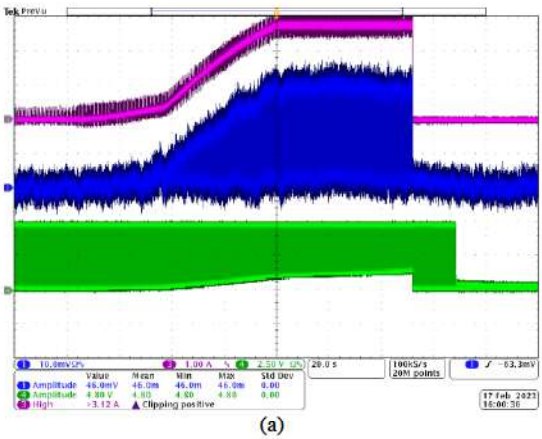
Fig. 6: Simulation waveforms for GaN FETs H-Bridge with high and low-side modified bootstrap-based *VDSon* measurement circuit. (a) High-side FET. (b) Low-side FET.

VI. CONCLUSION

This paper explicitly presented the challenges with the conventional GaN FET's VDS_{on} measurement circuit. The overshoot and ringing in the voltage and current waveforms of the measurement and DUT FET have been significantly damped by replacing the FET in the measurement circuit with the GaN device, even during the hard switching operation. This modification reduces the parasitic capacitance and inductance in the measurement circuit. The provided LTspice simulation and experimental results comprehensively analyze the conventional and the modified measurement circuits. A

bootstrap-based VDS_{on} measurement circuit was also designed and simulated for high-side VDS_{on} measurement. The bootstrap VDS_{on} measurement scheme uses no differential probes or isolated power supply for the high-side VDS_{on} measurement circuit. Hence, this approach can be helpful for health monitoring and conditioning in situ devices.

Fig. 7: Experimental setup for GaN-based H-bridge power converter with the conventional VDSon measurement circuit.



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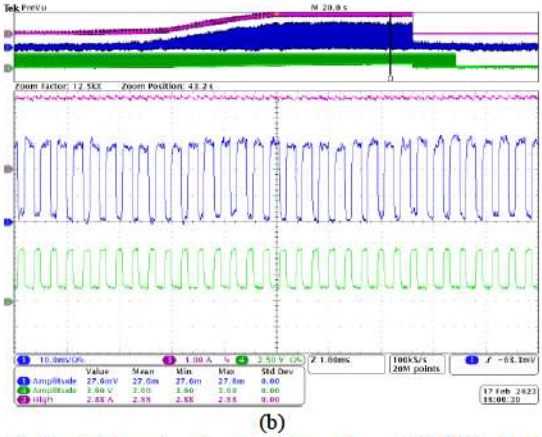

(b)

Fig. 8: Single thermal cycle waveforms where GaN FETs VDS_{on} is shown in green (Ch4), the current is in blue (Ch1), and the load current is in purple (Ch3). (a) Complete thermal cycle. (b) Zoomed-in area within the thermal cycle.

VII. ACKNOWLEDGMENT

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