



SparseAuto: An Auto-scheduler for Sparse Tensor Computations using Recursive Loop Nest Restructuring

ADHITHA DIAS, Purdue University, USA

LOGAN ANDERSON, Purdue University, USA

KIRSHANTHAN SUNDARARAJAH, Virginia Tech, USA

ARTEM PELENITSYN, Purdue University, USA

MILIND KULKARNI, Purdue University, USA

Automated code generation and performance enhancements for sparse tensor algebra have become essential in many real-world applications, such as quantum computing, physical simulations, computational chemistry, and machine learning. General sparse tensor algebra compilers are not always versatile enough to generate *asymptotically optimal code* for sparse tensor contractions. This paper shows how to generate asymptotically better schedules for complex sparse tensor expressions using kernel fission and fusion. We present generalized loop restructuring transformations to reduce asymptotic time complexity and memory footprint.

Furthermore, we present an auto-scheduler that uses a partially ordered set (poset)-based cost model that uses both time and auxiliary memory complexities to prune the search space of schedules. In addition, we highlight the use of Satisfiability Module Theory (SMT) solvers in sparse auto-schedulers to approximate the Pareto frontier of better schedules to the smallest number of possible schedules, with user-defined constraints available at compile-time. Finally, we show that our auto-scheduler can select better-performing schedules and generate code for them. Our results show that the auto-scheduler provided schedules achieve orders-of-magnitude speedup compared to the code generated by the Tensor Algebra Compiler (TACO) for several computations on different real-world tensors.

CCS Concepts: • **Software and its engineering** → **Source code generation; Domain specific languages.**

Additional Key Words and Phrases: Sparse Tensor Algebra, Loop Transformations, Fusion, Automatic Scheduling, Asymptotic Analysis

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1 Introduction

Tensor contractions are used in many real-world applications such as physical simulations, machine learning, computational chemistry, and quantum computing [Hirato 2003; Kossaifi et al. 2017; Markov 2008; Ran et al. 2017, 2020]. When most of the values in these tensors become zero, it is advantageous to use compact data formats to store only the non-zero values, and such tensors are known as *sparse tensors*. We can exploit the zeros in sparse tensors by skipping the computations over them (*i.e.*, $x + 0 = x$ and $x * 0 = 0$). Many important applications such as Graph Neural

Authors' Contact Information: [Adhitha Dias](mailto:Adhitha.Dias@purdue.edu), Purdue University, West Lafayette, USA, kadhitha@purdue.edu; [Logan Anderson](mailto:Logan.Anderson@purdue.edu), Purdue University, West Lafayette, USA, anderslt@purdue.edu; [Kirshanthan Sundararajah](mailto:Kirshanthan.Sundararajah@vt.edu), Virginia Tech, Blacksburg, USA, kirshanthans@vt.edu; [Artem Pelenitsyn](mailto:Artem.Pelenitsyn@purdue.edu), Purdue University, West Lafayette, USA, apelenit@purdue.edu; [Milind Kulkarni](mailto:Milind.Kulkarni@purdue.edu), Purdue University, West Lafayette, USA, milind@purdue.edu.



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Networks (GNN), Physical Simulation, and Quantum Chemistry [Hamilton et al. 2017; Hu et al. 2020; Rahman et al. 2021] make use of sparse tensor contractions.

Due to the *compressed data formats* that store the sparse tensors, their contractions are realized as *non-affine* loop nests, where bounds depend on the input, and accesses are indirect. The non-affine loop nests of sparse tensor contractions prevent us from directly applying classical affine loop transformation frameworks to reduce load imbalances and bad locality for performance enhancement. This challenge has given rise to specialized compilers for sparse tensor computations [Bik et al. 2022; Bik and Wijshoff 1993; Kjolstad et al. 2019, 2017; Kotlyar et al. 1997; Senanayake et al. 2020; Tian et al. 2021; Venkat et al. 2015] and various abstractions for the schedule — realization of computation (e.g., loop structure, parallelization etc.) — to separate it from the computation. Schedule abstractions (§ 2.4) make it convenient to realize a plethora of ways to materialize a computation using transformations such as loop reordering, loop fusion/fission, loop tiling, loop parallelization, etc.

Choosing a better-performing schedule for a sparse tensor contraction is not straightforward. Therefore, it is more challenging than finding a schedule for its dense counterpart, which is realized as *affine* loop nests (i.e., There exist well-studied analytical cost models of schedules and machines for dense tensor computations). The schedule selection heavily depends on sparse tensor inputs (number of non-zero values and sparsity structure), making it difficult to pick a performant one for sparse tensor computations. Hence, the simplest method to evaluate the cost of a schedule is to execute it on a given machine using the provided sparse tensor inputs to measure the time it takes to finish the execution. The sheer number of schedules makes it an arduous time-consuming process, rendering it impractical to execute all schedules in search of the best one. Also, it is important to note that there may not be a single best schedule for all sparse tensor inputs and machines, and some schedules may be *asymptotically* better than others.

The challenge in finding a performant schedule for sparse tensor contractions arises from two main factors: *vast space of schedules* and *heavy dependency on sparse tensor inputs*. We provide a systematic way to *completely* explore the vast space of schedule at compile-time rooted in transformations (i.e., loop reordering and loop/kernel fusion/fission), which makes it convenient to realize the schedule. The exploration of the schedule space is augmented with *machine-independent* pruning strategies and *symbolic sparse tensor input attributes* at compile-time to filter most of the schedules and keep a handful of schedules to be evaluated at run-time with *machine-dependent* parameters and *concrete sparse tensor input attributes* to select a performant schedule. As there are asymptotically superior schedules, the pruning strategy encompasses comparing schedules for *both* time and auxiliary memory complexity, which depends on the attributes of sparse tensor inputs. To the best of our knowledge, prior work does not optimize for both time and auxiliary memory complexity [Ahrens et al. 2022; Kanakagari and Solomonik 2023].

Consider this example of sparse tensor times matrix contraction: $A_{lmn} = \sum_{ijk} \mathbf{B}_{ijk} C_{il} D_{jm} E_{kn}$ ¹. This computation can be expressed using a simple linear loop nest with a time complexity of $O(\text{nnz}(\mathbf{B}_{ijk})LMN)$. Alternatively, the contraction can be expressed as $T_{ijn} = \sum_k \mathbf{B}_{ijk} E_{kn}$ and $A_{lmn} = \sum_{ij} T_{ijn} C_{il} D_{jm}$ — two separate computations with a total time complexity of $O(\text{nnz}(\mathbf{B}_{ijk})N + IJNLM)$ and a dense temporary T . Another schedule can be obtained from the observation that the outer loops of the first computation (producer) can be fused with the second computation (consumer) (i.e., loop fusion). This schedule reduces the overall time complexity to $O(N(\text{nnz}(\mathbf{B}_{ijk}) + \text{nnz}(\mathbf{B}_{ij})LM))$ ² and a scalar temporary, which is asymptotically superior to both of the previous schedules in time and memory complexity. The last schedule has a branching loop structure

¹Bold face letters denote sparse tensors.

² $\text{nnz}(\mathbf{B}_{ij})$ refers to iterating only the first two levels in the indexing arrays of $\mathbf{B}_{ij}$ without visiting the third dimension k .

(i.e., *imperfectly nested* loop nest) that is different from the other two schedules, which have simple loop structures (i.e., *perfectly nested* loop nests). However, the last schedule dominates the other two schedules in terms of both time and memory complexity (§ 3). Therefore, to explore schedules with multi-level branching loop structures, which are of asymptotically superior time and auxiliary memory complexity, we introduce the *extended representation of branched iteration graphs* [Dias et al. 2022] and a new *scheduling directive* to realize such schedules (§ 4). Furthermore, we explore the schedule space of a given sparse tensor computation and present strategies based on *partially ordered sets* (posets) that can be combined with user-defined constraints at compile-time to prune the schedule space (§ 5). Contributions of this paper are as follows:

Recursive extension of branched iteration graph We generalize the branched iteration graph (BIR) representation of SparseLNR [Dias et al. 2022] to support schedules with multiple levels of imperfectly nested loops and new *scheduling primitives* to realize the schedules by recursively applying loop/kernel fusion/fission with loop reorder.

Complete schedule space exploration We provide a strategy to explore the schedules of a given sparse tensor contraction *guaranteed* to cover the *complete* space of schedules with loop structures, including multi-level branching (i.e., multiple levels of imperfectly nested loops), attainable using loop/kernel fusion/fission.

Novel auto-scheduler We introduce a novel *poset-based* auto-scheduler to prune the space of schedules to create a Pareto frontier wrt. *both* time and auxiliary memory complexity. We use a Satisfiability Modulo Theory (SMT) solver to compare the symbolic time and memory complexity with *user-defined* constraints.

The rest of the paper is organized as follows. We provide the necessary background in Section 2 and in Section 3, we motivate the problem. The multi-level branched iteration graph and the scheduling primitives are introduced in Section 4. We discuss schedule exploration and selection in Section 5. Evaluation of our auto-scheduler is presented in Section 6. We conclude the paper in Section 8 with a discussion.

2 Background

This section discusses the necessary background on sparse tensor access constraints, tensor index notation, iteration graph representation, and scheduling primitives to understand the challenge in auto-scheduling for sparse tensor contraction.

2.1 Sparse Tensor Access Constraints

There are several compressed data formats used to store sparse tensors: Compressed Sparse Row (CSR), Sorted Coordinate (Sorted COO), Compressed Sparse Fiber (CSF), etc., to name a few. These formats are abstracted by *level format* [Chou et al. 2018], a tree structure that shows the order in which index arrays must be traversed to retrieve an element. The *sparse tensor access constraints* are imposed by the order of access of the index arrays in compressed data formats. For example, if A_{ij} is in CSR format, the row index should be traversed to get to the column index, which results in a dependency between i and j , the indices traverse rows and columns of A , respectively. Therefore, the loops i and j belong to cannot be freely reordered. TACO Format Abstraction [Chou et al. 2018] describes the level formats in detail.

2.2 Tensor Index Notation for Tensor Contractions

The notation that describes tensor contraction operations is based on the Einstein Summation (Einsum) convention. This notational convention implies summation over a set of repeated indices. For example, the expression $X(i, k) = A(i, j) \cdot B(j, k)$ implies summation over the repeated index

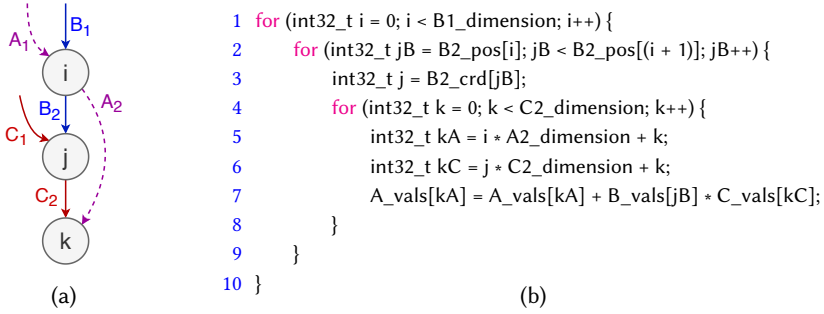


Fig. 1. An example of an iteration graph for sparse matrix-matrix multiplication and corresponding code.

j and equivalent to the standard mathematical notation $A_{ik} = \sum_j B_{ij}C_{jk}$ ³. We use both these notations interchangeably in the text. Since this computation can be performed using a simple linear triply nested loop, its iteration time complexity is $O(IJK)$, where I , J , and K are the loop bounds. If B is sparse, then the iteration time complexity is $O(\text{nnz}(B_{ij})K)$, where nnz is the number of non-zero elements.

2.3 Iteration Graph

Consider the example sparse matrix-matrix multiplication (SpMM), $A_{ik} = \sum_k B_{ij}C_{jk}$. An iterator that iterates through all of i , j , and k can read each value of B_{ij} , C_{jk} , multiply each value sharing the same j , and store the result in A_{ik} . An example iteration graph is shown in Figure 1a, and this internal representation (IR) is used to generate code in Figure 1b. The nodes in the iteration graph represent indices in the Einsum notation. This is an acyclic graph where the edges represent the dimensions of tensors and how they map to indices. Since B is sparse, B_1 and B_2 , incidents on indices i and j must not change the order, and other indices can appear in any order as they traverse dense tensors (e.g., C_1 and C_2). No other sparse tensor access constraints (§ 2.1) are imposed. TACO [Kjolstad et al. 2017] describes the concept of iteration graphs in detail.

2.4 Scheduling Primitives

A schedule describes one way of realizing a computation, and multiple schedules can realize the same computation. For example, we can change the loop order in Figure 1 to get the order i, k, j instead of i, j, k . TACO and Sparse Iteration Space Framework [Senanayake et al. 2020] describe the importance of abstractions to separate the computation from the schedule. The algorithmic and scheduling languages describe the computation and schedule, respectively, and scheduling primitives form the scheduling language. Some of the scheduling primitives are as follows: *reorder* to reorder the loops; *split* to split a loop for tiling; *collapse* to collapse one loop onto another; *parallelize* and *vectorize* for parallel execution. TACO-Workspaces [Kjolstad et al. 2019] introduces *precompute* to add dense intermediaries to schedules. In Section 4, we introduce a new scheduling primitive called **looppfuse**, which can produce loop nests with branched loops (i.e., imperfectly nested loops) combined with the **reorder** directive.

3 Overview

It may not be straightforward to decide whether to apply transformations across multiple kernels. The decision depends both on the iteration complexity of the final loop nests and the working set

³This is the matrix-matrix multiply operation.

<pre> 1 for perm(l,m,n,i,j_pos,k_pos): 2 A(l,m,n)+=B(i,j,k)*C(i,l)*D(j,m)*E(k,n) (a) $A_{lmn} = \sum_{ijk} \mathbf{B}_{ijk} \cdot C_{il} \cdot D_{jm} \cdot E_{kn}$ Time: $LMN \cdot \text{nnz}(B)$, Memory: 0 Loop Depth: 6, Memory Depth: 0 </pre>	
<pre> 1 for perm(m, l): 2 T<k> = 0 3 for i, j_pos, k_pos: 4 T(k) += B(i,j,k)*C(i,l)*D(j,m) 5 for perm(n, k): 6 A(l,m,n) += T(k)*E(k,n) (b) $A_{lmn} = \sum_k (\sum_{ij} \mathbf{B}_{ijk} \cdot C_{il} \cdot D_{jm}) \cdot E_{kn}$ Time: $LM \cdot (\text{nnz}(B) + NK)$, Memory: K Loop Depth: 5, Memory Depth: 1 </pre>	<pre> 1 for l: 2 T<k,j> = 0 3 for i, j_pos, k_pos: 4 T(k,j) += B(i,j,k)*C(i,l) 5 for perm(j, m, k, n): 6 A(l,m,n) += T(k,j)*D(j,m)*E(k,n) (c) $A_{lmn} = \sum_{jk} (\sum_i \mathbf{B}_{ijk} \cdot C_{il}) \cdot D_{jm} \cdot E_{kn}$ Time: $L \cdot (\text{nnz}(B) + JMKN)$, Memory: KJ Loop Depth: 5, Memory Depth: 2 </pre>
<pre> 1 for l: 2 T<k,j> = 0 3 for i, j_pos, k_pos: 4 T(k,j) += B(i,j,k)*C(i,l) 5 for perm(m, k): 6 t = 0 7 for j: 8 t += T(k,j)*D(j,m) 9 for n: 10 A(l,m,n) += t*E(k,n) (d) $A_{lmn} = \sum_k (\sum_j (\sum_i \mathbf{B}_{ijk} \cdot C_{il}) \cdot D_{jm}) \cdot E_{kn}$ Time: $L \cdot (\text{nnz}(B) + MK(J + N))$, Memory: KJ Loop Depth: 4, Memory Depth: 2 </pre>	<pre> 1 for l: 2 T<j,k> = 0 3 for i, j_pos, k_pos: 4 T(k,j) += B(i,j,k)*C(i,l) 5 T<m,k> = 0 6 for perm(j, m, k): 7 T(m,k) += T(j,k)*D(j,m) 8 for perm(m, k, n): 9 A(l,m,n) += T(m,k)*E(k,n) (e) $A_{lmn} = \sum_k (\sum_j (\sum_i \mathbf{B}_{ijk} \cdot C_{il}) \cdot D_{jm}) \cdot E_{kn}$ Time: $L \cdot (\text{nnz}(B) + MK(J + N))$, Memory: $KJ + MK$ Loop Depth: 4, Memory Depth: 2 </pre>

Fig. 2. Different schedules of executing $A_{lmn} = \sum_{ijk} \mathbf{B}_{ijk} \cdot C_{il} \cdot D_{jm} \cdot E_{kn}$. Here, the code snippet 2a has a perfectly nested loop structure while all the other code snippets has a nested loop structure. Here, j_pos refers to the non-affine loop associated with the index j . The loop j_pos is non-affine because $\mathbf{B}_{ij}$ is sparse. The code snippets 2b and 2c has one level of branching whereas the code snippets 2d and 2e has a branch nesting depth of two.

sizes.⁴ If the working set sizes are small and fit into the cache then, it is better to use the version with lower iteration complexity. Otherwise, it is better to use the schedule with lower auxiliary memory. Hence, an auto-scheduler that only looks at the iteration complexity or only the auxiliary memory complexity may choose the wrong schedule as the final output or prune a good schedule from the search space in the process.

3.1 Motivating Example

There may be many schedules to perform a tensor contraction, and which one to choose depends on your viewpoint. Consider the following example involving a sparse tensor $\mathbf{B}$:

$$A(l, m, n) = \mathbf{B}(i, j, k) * C(i, l) * D(j, m) * E(k, n)$$

⁴Iteration complexity refers to the number of total iterations in a loop nest required to complete the computation. For example, iteration complexity of the kernel in Figure 2a is $LMN \cdot (\text{nnz}(B))$

Figure 2a refers to performing the computation using a simple loop nest of depth 6. The same computation can be written as in figures 2b, 2c, 2d, and 2e with branching loop nests of depth 4 or 5. In this section, we will discuss the performance of these different schedules. We will evaluate all the schedules with the same loop structure, but with different index ordering and report the best one. For the loop structure in Figure 2d, we will evaluate both the inner loop order of m, k and k, m . Similarly, for Figure 2b, we will evaluate four different loop orders, two of them by interchanging the inner loops n, k and two of them by interchanging the outer loops l, m .

From the asymptotic time complexity viewpoint, an auto-scheduler might lean towards pruning Schedule 2a. This is due to its loop nesting depth of 6 and time complexity of $O(\text{nnz}(B_{IJK})LMN)$, in contrast to the schedule in Figure 2b with a loop nesting depth of 5 and asymptotic time complexity of $O(\text{nnz}(B_{IJK})LM + LMNK)$ or the schedule in Figure 2d with a loop nesting depth of 4 and asymptotic time complexity of $O(\text{nnz}(B_{IJK})L + LMK(J + N))$. Notably, the schedule in Figure 2e has the same asymptotic time complexity as the schedule in Figure 2d, while the asymptotic time complexity of the schedule in Figure 2c is $O(\text{nnz}(B_{IJK})L + LJMKN)$.

These schedules can be placed on a asymptotic time complexity vs. auxiliary memory complexity space plot as shown in Figure 3, relative to each other. From the perspective of asymptotic time complexity, an auto-scheduler might favor either the schedule in Figure 2d or Figure 2e, both having a loop depth of 4, the lowest among the five schedules in Figure 2. Comparing these two schedules, Figure 2d uses one 2D auxiliary memory for storing intermediate results between branched loop nests, while Figure 2e uses a 2D and a 1D auxiliary memory. Consequently, the former has lower memory complexity than the latter. In summary, the schedule in Figure 2d dominates Figure 2e, as both schedules share the same asymptotic time complexity, but the former is better in terms of auxiliary memory complexity.

Comparing the schedules in Figures 2d and 2c from the asymptotic memory complexity perspective, both exhibit an auxiliary memory complexity of $O(KJ)$. The time complexity of the former, Figure 2d, is superior with $O(J + N)$ being better than $O(JN)$ for larger values of J and N . Consequently, Figure 2d dominates Figure 2c. For the sake of brevity, comparisons involving Figures 2e and 2c with other schedules are omitted in the following paragraphs.

Consider the comparison of the schedules in Figures 2a, 2b, and 2d when the bounds change in the range as follows; $1 \leq I \leq 1800$, $1 \leq J \leq 1600$, $400 \leq K \leq 4000$, $8 \leq L \leq 256$, $8 \leq M \leq 256$, $8 \leq N \leq 256$, and $0.001 \leq \text{sparsity}(B) \leq 0.01$. Note that the schedule in Figure 2a dominates both the schedules in Figures 2b and 2d in terms of the auxiliary memory usage because no auxiliary memory is used in the Schedule 2a. Although the loop depth is four for the schedule in Figure 2d, within the given ranges of bounds and the sparsity of B , we cannot claim that it is the best in all cases. Let us look at some cases by changing the loop bounds and sparsity for tensor B . The evaluation configuration is explained in Section 6.

Case ①: Lowest loop depth schedule (Figure 2d) is the best In this case, we set the loop bounds for the schedules in Figure 2 to specific values: $I = 1800$, $J = 800$, $K = 1000$, $L = 64$, $M = 16$, $N = 32^5$, and $\text{sparsity}(B) = 0.08$. Under these conditions, the iteration time complexities follow the

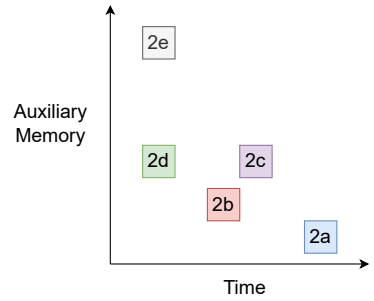


Fig. 3. Relative placement of schedules from Figure 2 based on asymptotic time vs. auxiliary memory complexities.

⁵ I, J, K, L, M , and N are the loop bounds of loops with indices i, j, k, l, m , and n , respectively.

inequality $\Phi(d)^6 < 7.5 * \Phi(d) \approx \Phi(b) < 237.5 * \Phi(d) \approx \Phi(a)$. The corresponding execution times follow the inequality $\Psi(d)^7 = 2.48s < \Psi(b) = 6.26s < \Psi(a) = 32.40s$. The schedule in Figure 2d exhibits the lowest loop depth and iteration time complexity. An auto-scheduler that factors in loop depth could choose the best schedule in this case.

Case ②: Effect of the size of auxiliary memory Adjusting the loop bounds to $J = 1600$, $K = 2000$ and $\text{sparsity}(B) = 0.02$ while maintaining other loop bounds as in the previous example, the schedule in Figure 2d now incurs an auxiliary temporary memory requirement of 12.21MB (compared to 3.05MB in Case ①). This consumes more than 50% of the last-level cache (LLC). The iteration time complexities follow the inequality: $\Phi(d) < 3 * \Phi(d) \approx \Phi(b) < 92.5 * \Phi(d) \approx \Phi(a)$. Execution times for the schedules follow the inequality, $\Psi(b) = 8.60s < \Psi(d) = 10.20s < \Psi(a) = 33.51s$. The schedule in Figure 2d, with the minimum loop depth, exhibits the lowest iteration time complexity as in the previous example, but the schedule in Figure 2b, with a loop depth of 5, performs better. It is evident from this case that a good auto-scheduler must consider the sizes of the auxiliary memory arrays used in the computation. Consequently, an auto-scheduler solely reliant on loop depth would fail in this scenario.

Case ③: Highest loop & lowest memory depth schedule (Figure 2a) is the best Setting loop bounds and sparsity as $I = 1$, $J = 200$, $K = 4000$, $L = 256$, $M = 200$, $N = 196$, and $\text{sparsity}(B) = 0.002$, the execution times of the schedules in Figure 2a, Figure 2b, and Figure 2d follows the inequality: $\Psi(a) = 4.9ms < \Psi(b) = 9.1ms < \Psi(d) = 282.5ms$. This scenario is an example where the schedule with the highest loop depth (Schedule a) executes the fastest. An auto-scheduler that factors in loop depth would discard this schedule in favor of the schedules with lower loop depths. This case highlights the need for a robust auto-scheduler to consider factors beyond loop depth.

Case ④: Neither the lowest loop depth, nor the highest loop depth schedule (Figure 2b) is the best Setting loop bounds and sparsity as $I = 265$, $J = 1207$, $K = 479$, $L = 251$, $M = 234$, $N = 42$, and $\text{sparsity}(B) \approx 0.0033$, Figure 2b performs the fastest at $\Psi(b) = 513ms$, followed by $\Psi(d) = 1.14s$ for Figure 2d, and $\Psi(a) = 1.66s$ for Figure 2a. In this scenario, auxiliary memories account for less than 12% of the LLC. For these values, $\Phi(a) = 1.13 \times \Phi(b)$ and $\Phi(d) = 40.4 \times \Phi(b)$. Execution times align with iteration complexities, and auxiliary memory usage is reasonably modest. Unlike previous cases, where the best loop or memory depth proved to be the most efficient, this instance underscores the need for schedulers to consider multiple factors beyond loop and auxiliary memory depth when pruning the search space.

3.2 Our approach: SparseAuto

The insights drawn from the motivating example and our approach to schedule selection can be summarized as follows.

Multi-Level Branched Loop Nests Nested loop computations with reduced loop depth (as in Case ①) are crucial. However, existing scheduling languages lack support for multi-level branched loop nests. To address this, we extend the branched iteration graph (BIG) [Dias et al. 2022; Kjolstad et al. 2017] to accommodate recursive, multi-level branched iteration graphs with multi-dimensional temporary buffers. We also enhance the scheduling language to support recursive fusion by adapting TACO's code generation strategies.

Time and Auxiliary Memory Complexities Both time and auxiliary memory complexities contribute to the schedule's execution time. An effective auto-scheduler needs to consider both

⁶ $\Phi(x)$ refers to the iteration time complexity of the schedule in Figure 2x for concrete bounds in the given Case.

⁷ $\Psi(x)$ refers to the execution time of the schedule in Figure 2x.

aspects when selecting a schedule (as seen in Cases ②–④). If a schedule's auxiliary memory takes up a large portion of the last-level cache, it tends to perform worse than the alternatives (as observed in Case ②). To address this, we introduce an auto-scheduler that employs an SMT solver. The solver is guided by the constraints of sparse computations and reasons about the partial orders of time and auxiliary memory complexity. This approach effectively prunes the search space, leading to the selection of schedules that dominate others in both time and memory complexity.

4 Design of the Transformation

Tensor contractions can be materialized using a simple linear loop nest where there would be a corresponding loop for each of the indices in the Einsum expression. This loop nest is represented as a linear iteration graph (LIG) as explained in Section 4.1, which is used for sparse code generation. However, this simple loop nest must respect the sparse tensor access constraints. For example, if a sparse tensor is in CSR format, the row should be accessed first. In this section, we describe an algorithm to recursively generate a branched iteration graph (BIG), the transformation required to convert a LIG into a multi-level BIG (§ 4.2), and how this transformation can cover a plethora of possible loop nests for the computation (§ 4.5).

4.1 Linear Iteration Graph (LIG) —Equivalence Class of Tensor Contractions

Consider a tensor contraction:

$$O(idx_{out}) = \sum_{idx_{contract}} I_1(idx_1) * \dots * I_i(idx_i) * \dots * I_n(idx_n).$$

Here, $I_1 \dots I_n$ denote the input tensors; O denotes the output tensor; $idx_{contract}$ denotes the indices that need to be contracted from the tensor expression. The example tensor contraction can be materialized in several ways, two of which are as follows (access indices are omitted for brevity):

<pre> 1 loop₁ ... loop_i ... loop_j ... loop_n: 2 O += I₁ * ... * I_i * ... * I_m * ... * I_e </pre>	<pre> 1 loop₁ ... loop_j ... loop_i ... loop_n: 2 O += I₁ * ... * I_m * ... * I_i * ... * I_e </pre>
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There are two main differences between the two materializations: loops i and j are swapped, as well as tensors I_l and I_m in the expression. Therefore, the orders of accessing elements of input tensors and storing elements of the output tensor differ. But in general, any permutation of $loop_1, loop_2, \dots, loop_n$, and any permutation of $I_1, \dots, I_n$ yields the correct output tensor O , when we complete all the iterations. This observation also holds when some of the tensors are sparse, although the index order must satisfy the sparse tensor access constraints. Overall, materializations like the ones above belong to an *equivalence class* because they produce the same output.

We define a **linear iteration graph (LIG)** as a loop nest with no two loops having the same depth from the root of the nest and an index order that respects all the sparse tensor access constraints. Hence, we consider any permutation of the loops and input tensors that do not violate the sparse access constraints as a representative of an equivalence class since it produces the same result for a given tensor contraction.

4.2 Multi-level Branched Iteration Graphs (BIG)

In this section, we describe the multi-level BIG transformation. We demonstrate how the algorithm works for the example tensor contraction from Section 3 and by showing how the LIG in Figure 5 transforms into a BIG (5a → 5b and 5a → 5c → 5d → 5e).

The tensor contraction $A(l, m, n) = B(i, j, k) * C(i, l) * D(j, m) * E(k, n)$ has a default iteration graph (Figure 5a) which implies generated code in Figure 2a. The IR of this iteration graph is shown in the listing below:

```

1  forall(l, forall(m, forall(n, forall(i, forall(j, forall(k, A(l,m,n) += B(i,j,k) * C(i,l) * D(j,m) * E(k,n)))))))

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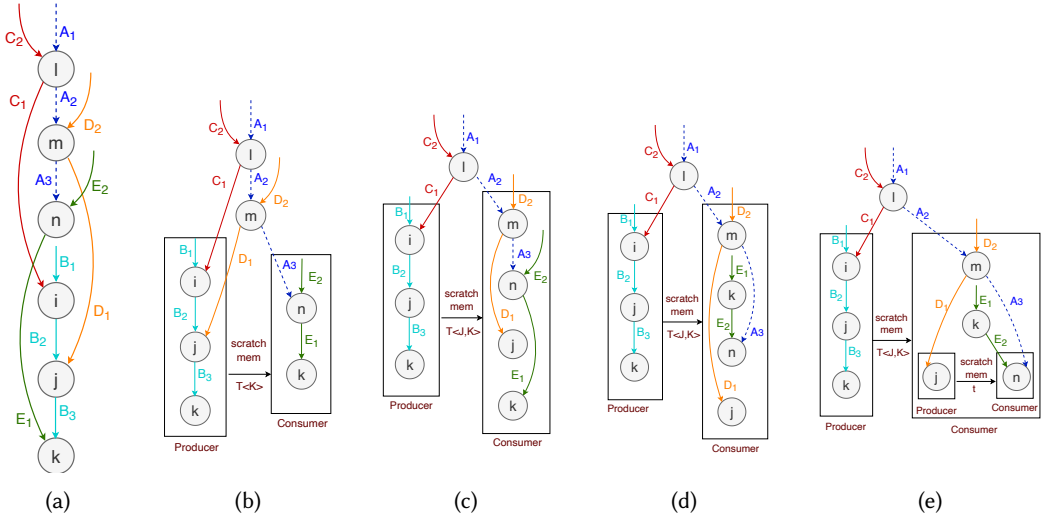


Fig. 5. loopfuse transformation performed on $A_{lmn} = \sum_{ijk} B_{ijk} C_{il} D_{jm} E_{kn}$. (a) TACO default kernel, (b) Fused kernel with K extra memory, (c) Fused kernel with JK extra memory, (d) 5c with reordered consumer branch, and (e) Multi-level nesting after fusing inner branch of 5d.

Transform Iteration Graph 5a $\rightarrow$ 5b Let us split the computation into two parts, the producer and the consumer. The first one, $T(idx_{temp}) = \sum B(i, j, k) * C(i, l) * D(j, m)$, produces the intermediate temporary tensor T with indices idx_{temp} , which is consumed in the second one, $A(l, m, n) = T(idx_{temp}) * E(k, n)$, to generate the output A . Here, $idx_{temp} = \{l, m, k\}$ is obtained by evaluating: $\text{Indices}(B(i, j, k) * C(i, l) * D(j, m)) \cap (\text{Indices}(A(l, m, n)) \cup \text{Indices}(E(k, n)))$. Hence, the auxiliary memory required is $O(LMK)$.

The split computations from the original one have iteration graphs with the following index orders: $\textcircled{1} \rightarrow \textcircled{m} \rightarrow \textcircled{i} \rightarrow \textcircled{j} \rightarrow \textcircled{k}$ for the producer and $\textcircled{1} \rightarrow \textcircled{m} \rightarrow \textcircled{n} \rightarrow \textcircled{k}$ for the consumer. These ones preserve the index order in the original iteration graph $\textcircled{1} \rightarrow \textcircled{m} \rightarrow \textcircled{n} \rightarrow \textcircled{i} \rightarrow \textcircled{j} \rightarrow \textcircled{k}$ (Figure 5a). As both iteration graphs share the same indices l and m at the beginning, they can be fused into the BIG in Figure 5b, facilitating code generation in Figure 2b. Since the unfused sections of the producer and consumer graphs include i, j, k and n, k respectively, the fused iteration graph would require extra memory of K , obtained from $\{i, j, k\} \cap \{n, k\}$, to pass the intermediate results between the two computations. Notably, only an auxiliary memory of size K is required after fusion, compared to the one with size LMK before fusion.

Transform Iteration Graph 5a $\rightarrow$ 5c The original tensor contraction can be split into two computations in a different way. For example, $T(idx_{temp}) = B(i, j, k) * C(i, l)$ and $A(l, m, n) = T(idx_{temp}) * D(j, m) * E(k, n)$ where $idx_{temp} = \{l, j, k\}$. This would result in the producer and consumer iteration graphs $\textcircled{1} \rightarrow \textcircled{i} \rightarrow \textcircled{j} \rightarrow \textcircled{k}$ and $\textcircled{1} \rightarrow \textcircled{m} \rightarrow \textcircled{n} \rightarrow \textcircled{j} \rightarrow \textcircled{k}$, respectively. Since they have a common index l at the beginning of the iteration graph, they can be fused to generate the BIG in Figure 5c. Fusing the iteration graph reduces the auxiliary memory requirement to JK as opposed to the LJK before. After fusion, the IR is shown in the listing below (notice the addition of the temporary $t1$ and the where clause to combine the producer and consumer computations):

```

1 forall(l, where(
2     forall(m, forall(n, forall(j, forall(k, A(l,m,n) += t1(j,k) * D(j,m) * E(k,n))))),
3     forall(i, forall(j, forall(k, t1(j,k) += B(i,j,k) * C(i,l))))))

```

Algorithm 1 Multi-level BIG Transformation**Input:** Valid Iteration Graph $G_I^{complete}$ **Input:** Path to Inner Iteration graph $path : Vector$ **Input:** Split Position $i : Int$ **Input:** Is Producer On the Left? $pol : bool$ **Output:** Multi-level BIG G'_I

```

1:  $G_I^{old} = GetInnerGraphUsingPath(G_I^{complete}, path)$ 
2:  $comp = GetInnerComputation(G_I^{old})$  ▷ computation:  $A_{out}+ = A_1 * A_2 * .. * A_i * ... * A_n$ 
3:  $expr_{producer} = (pol == True) ? A_1 * ... * A_i : A_{i+1} * ... * A_n$ 
4:  $expr_{consumer} = (pol == False) ? A_{i+1} * ... * A_n : A_1 * ... * A_i$ 
5:  $I_{temp} = GetIndices(expr_{consumer}) \cap (GetIndices(expr_{producer}) \cup GetIndices(A_{out}))$ 
6:  $ProducerExpr := T'(I_{temp})+ = expr_{producer}$ 
7:  $ConsumerExpr := A_{out}+ = (pol == True) ? T'(I_{temp}) * expr_{consumer} : expr_{consumer} * T'(I_{temp})$ 
8:  $List_{I-Prd} = GetIndicesInOrder(ProducerExpr, G_I^{old})$ 
9:  $List_{I-Con} = GetIndicesInOrder(ConsumerExpr, G_I^{old})$ 
10: Define:  $I_{fusible} = \emptyset$ 
11: for each  $i \in G_I^{old}$  do
12:   if  $i \in List_{I-Prd}$  and  $i \in List_{I-Con}$  then
13:      $I_{fusible} = I_{fusible} \cup i$ 
14:   else break;
15: Define:  $I_{shared} = \{List_{I-Prd} \cap List_{I-Con}\} \setminus I_{fusible}$ 
16: Define:  $T(I_{shared})$ 
17:  $ProducerExpr := T(I_{shared}) = expr_{producer}$ 
18:  $ConsumerExpr := A_{out}+ = (pol == True) ? T(I_{temp}) * expr_{consumer} : expr_{consumer} * T(I_{temp})$ 
19:  $G_I^{new} = GraphRewrite(G_I^{old}, I_{fusible}, ProducerExpr, ConsumerExpr)$ 
20: return  $GraphReplace(G_I^{complete}, G_I^{new}, G_I^{old})$ 

```

Transform Iteration Graph 5c $\rightarrow$ 5d We notice that, after fusion, each of the unfused sections of the producer and consumer iteration graphs can be treated as separate iteration graphs by keeping all the fused indices fixed in the computation. For example, take the consumer computation, $A(l, m, n) = T(l, j, k) * D(j, m) * E(k, n)$. We can rewrite the computation as $A(_, m, n)+ = T(_, j, k) * D(j, m) * E(k, n)$ by fixing l , with corresponding iteration graph $(m) \rightarrow (n) \rightarrow (j) \rightarrow (k)$. This can be split into two computations: $T'(m, k)+ = T(_, j, k) * D(j, m)$ and $A(_, m, n)+ = T'(m, k) * E(k, n)$, with corresponding iteration graphs $(m) \rightarrow (j) \rightarrow (k)$ and $(m) \rightarrow (n) \rightarrow (k)$, respectively. Both of these iteration graphs have the same first index (m) that can be fused. The iteration graph in this configuration (not shown in Figure 5) would be able to generate the code in Figure 2e. This configuration would require auxiliary memory of size K because the unfused part of each iteration graph shares the common index $\{k\} = \{j, k\} \cap \{n, k\}$. The iteration graph in Figure 5c can be transformed to the iteration graph in Figure 5d with the inner consumer index order $(m) \rightarrow (k) \rightarrow (n) \rightarrow (j)$, by reordering the consumer part of Figure 5c.

Transform Iteration Graph 5d $\rightarrow$ 5e Splitting the consumer computation as described previously yields the producer and consumer iteration graphs $(m) \rightarrow (k) \rightarrow (j)$ and $(m) \rightarrow (k) \rightarrow (n)$, respectively, which can be fused to generate the multi-level BIG in Figure 5e. Since the unfused sections of the producer and consumer graphs do not share any common indices, it only requires a scalar auxiliary memory to pass the intermediate results between the producer and consumer. The

final IR is shown in the listing below (notice the use of two temporaries $t1$ and $t2$, and the nested combination of where clauses):

```

1 forall(l, where(
2   forall(m, forall(k, where(
3     forall(n, A(l,m,n) += t2 * E(k,n)),
4     forall(j, t2 += t1(j,k) * D(j,m))))),
5   forall(i, forall(j, forall(k, t1(j,k) += B(i,j,k) * C(i,l))))))

```

4.3 LIG to BIG Transformation Algorithm

Algorithm 1 shows the pseudo-code for the transformation described previously in Section 4.2. This algorithm takes several inputs: the original iteration graph (LIG or BIG), the *path* to an inner producer/consumer section, the position to split (*Split Position* : i), the input tensors in the contraction, and a boolean flag to indicate whether the producer expression is on the left or the right after the split. Input variable *path* is used in line 1 to access the inner producer/consumer graph sections, which helps to apply the transformation *recursively* to the inner linear graph sections.

The split operation occurs in lines 2–4. For example, given the expression $A = B * C * D$ and $i = 2$, the splits are $T = B * C$ and $A = T * D$. If $i = 1$, then the splits are $T = B$ and $A = T * C * D$. The algorithm initially deduces the indices of the temporary resulting from the split (line 5) using the equation $Indices(Consumer) \cap (Indices(Producer) \cup Indices(Output))$. This equation calculates the indices in the producer that also appear in either the consumer or the output. The algorithm generates corresponding split expressions in lines 6–7. Subsequently, the producer and consumer graphs are computed in lines 8–9, preserving the index order of the original graph. Then, the algorithm determines the fusible outer loops (lines 10–14) and shared indices (lines 15–16). Finally, it produces the expressions for the producer and consumer in the fused iteration graph in lines 17–18, and the original iteration graph is replaced with the fused iteration graph in lines 19–20. One step of the transformation is linear time with respect to the number of indices in the graph.

4.4 Scheduling Language

Figure 6 shows the implementation of the transformations described in Section 4.2 using the scheduling language. The schedule description in Figure 6a can be used to transform the iteration graph in Figure 5a to the one in Figure 5b. The schedule description in Figure 6b can be used to transform the original iteration graph in Figure 5a to the one in Figure 5e by doing multiple transformations.

- **loopfuse** scheduling directive splits and fuses LIGs. It takes three parameters:
 - **path** identifies linear graph sections, consumer or producer sections, of a BIG. The path parameter must direct to a linear graph section for the transformation to be applied. Here, $\{\}$ means accessing the root of an iteration graph, $\{0\}$ means accessing the producer section, and $\{1\}$ means accessing the consumer section. If the BIG has multiple levels, $\{0, 1\}$ would access the producer of the first level and then the consumer of the second level.
 - **loc** specifies the split position in the inner computation. For example, if the inner computation is $A = B * C * D$ and $loc=2$, then the split is $T = B * C$ and $A = T * D$, and if $loc=1$, then the split is $T = B$ and $A = T * C * D$.
 - **pol** designates the first or second half of the contraction as the producer. If $pol=True$, then the producer is on the left, and the consumer is on the right, and if $pol=False$, then vice versa. For example, if the expression is $A = B * C * D$, $loc=2$ and $pol=True$, then the split is $T = B * C$ and $A = T * D$, and if $pol=False$, then the split is $T = C * D$ and $A = B * T$.
- **reorder** scheduling directive reorders indices of a linear graph section. It takes two parameters:

<pre> 1 A(l,m,n) = B(i,j,k)*C(i,l)*D(j,m)*E(k,n); 2 // Index stmt of 5a 3 IndexStmt stmt = A.getAssignment(). concretize(); 4 // Apply transformation 5 stmt = stmt // 5a -> 5b 6 .loopfuse(loc = 2, pol = True, path = {}); </pre>	<pre> 1 A(l,m,n) = B(i,j,k)*C(i,l)*D(j,m)*E(k,n); 2 // Index stmt of 5a 3 IndexStmt stmt = A.getAssignment().concretize(); 4 // Apply transformation 5 stmt = stmt 6 .loopfuse(loc = 3, pol = True, path = {}) // 5a -> 5c 7 .reorder(order = {m, k, n, j}, path = {1}) // 5c -> 5d 8 .loopfuse(loc = 2, pol = True, path = {1}); // 5d -> 5e </pre>
(a) 5a → 5b	(b) 5a → 5c → 5d → 5e

Fig. 6. Transformation on the loop contraction

<pre> 1 loops P: 2 T(S)+ = CompP 3 loops C: 4 A(..)+ = T(S) * CompC </pre>	<pre> 1 T(S) = $\sum_{P \setminus S} CompP$ 2 loops C: 3 A(..)+ = T(S) * CompC </pre>	<pre> 1 loops C: 2 A(..)+ = 3 ($\sum_{P \setminus S} CompP$) * CompC </pre>
(a)	(b)	(c)
<pre> 1 loops C: 2 A(..)+ = 3 ($\sum_{P \setminus S} CompP * CompC$) </pre>	<pre> 1 loops C ∪ (P \ S): 2 A(..)+ = CompP * CompC </pre>	
(d)	(e)	

Fig. 7. Moving producer computation to the consumer to obtain a LIG.

- **path** identifies an inner linear graph section.
- **order** specifies the new order of the indices in the linear graph section.

The `reorder` and `loopfuse` directives can be used together to obtain the desired multi-level BIG. These two directives can be used in conjunction to generate all possible loop trees for a given tensor contraction.

4.5 Completeness of the algorithm

This section provides a proof sketch for the completeness of Algorithm 1: we argue that the algorithm can generate all possible loop structures for a given tensor contraction using the `loopfuse` and `reorder` scheduling directives.

Constraints Two essential constraints ensure the validity of BIG constructed by Algorithm 1 and the equivalence of the BIG to the initial LIG. First, the BIG must not violate any sparse tensor access constraints present in the initial computation. For instance, in all the iteration graphs in Figure 5, the iteration order $B_1 \rightarrow B_2 \rightarrow B_3$ (i.e., $i \rightarrow j \rightarrow k$), is consistently maintained when contracting the sparse tensor B with other tensors. Second, a permutation of indices in producer and consumer loops is required to establish identical orders of shared indices (i.e., indices in the temporary tensor).

The second constraint can be understood as follows. Let i and j be the indices present in the temporary tensor. Let P and C be the sets of all valid (in the sense of the first constraint) permutations of indices in the loops of producer and consumer, respectively. Let the focus be on $i \rightarrow \dots \rightarrow j$ and $j \rightarrow \dots \rightarrow i$ in P and C sets. Let *condition1* be $i \rightarrow \dots \rightarrow j$ in P and $i \rightarrow \dots \rightarrow j$ in C , and *condition2* be $j \rightarrow \dots \rightarrow i$ in P and $j \rightarrow \dots \rightarrow i$ in C . If either *condition1* or *condition2* is satisfied, then we say that the BIG is valid. If neither *condition1* nor *condition2* is satisfied, then we say the second constraint is violated and the BIG is invalid. The temporary tensors introduced by the Algorithm 1 are dense. Hence, they do not impose extra constraints, and establishing identical orders of shared indices is not impeded by the temporaries.

Equivalence of BIG and LIG In the context of reasoning about LIGs and BIGs, having a transformation from BIG to LIG, complementary to the one performed by Algorithm 1, proves beneficial. This transformation involves examining the innermost subtree (with no nested subtrees inside of it), as illustrated in Figure 7. Denoting shared indices between the producer and consumer as S , producer loops as P , and consumer loops as C , the transformation requires an order of S complying with sparse tensor access constraints in both P and C , adhering to the second constraint. By keeping the outer loops constant in inner branch computations (details omitted for simplicity), the BIG illustrated in Figure 7a is realized. The contraction for T is depicted in Figure 7b, where $P \setminus S$ denotes contracted indices. Substituting $T(S)$ inside the consumer (Figure 7c), the consumer computation ($Comp_c$) is moved inside the summation operation, ensuring none of its indices contain the ones in $P \setminus S$ (Figure 7d). Further, contracting indices are reintegrated into consumer graph loops (Figure 7e), satisfying all constraints and resulting in a LIG. This recursive process applies to multi-level BIGs, yielding a LIG equivalent to the initial BIG.

Fineteness of the space A conservative upper bound on the number of BIGs can be established by considering the number of input tensors in the tensor contraction (n), and the number of indices in the tensor contraction (m). The input tensors can be permuted in $n!$ ways. A BIG can be built by recursively splitting the computation into producer and consumer sections. Since the number of input tensors are n , the number of binary trees that can be built is bounded by 2^n . The indices can be permuted in $m!$ ways. Since there are 2^n splits, indices can be permuted at each split giving $m!^{2^n}$ permutations. At each split operation, there is a choice to fuse the indices or not. Since the number of indices is m , the number of ways to fuse the indices is bounded by $m + 1$ for each of those binary trees. Therefore, the total number of BIGs is bounded by $n! \times 2^n \times m!^{2^n} \times (m + 1)$.

Completeness Consider the different schedules for a given tensor contraction as points in a space. If you can reach a schedule from another, then they are connected in this space. We established that a BIG can be linearized. Therefore, every BIG is connected to a LIG. As outlined in Section 4.1, LIG schedules are equivalent, and we end up connecting all the points. Focusing on the linearization procedure for a BIG, the movement of T from producer to consumer involves reordering the loops of producer and consumer such that after reordering the loops, the shared indices have the same relative ordering. T consists of some input tensors in the original tensor contraction. In other words, input tensors in the producer computation are some combination of the input tensors. This combination can be obtained by permuting the input tensors in the original expression and splitting from a specific position. Since each valid BIG can be transformed to a LIG, it is possible to traverse in the direction of LIG to BIG by using the transformation in Sections 4.2–4.4. Therefore, by (1) permuting all schedules in our equivalence class, (2) applying the transformation in Section 4.2 to obtain BIGs, and (3) recursively applying (1) and (2) on inner producer and consumer sections, we can generate all possible iteration graphs (loop structures of schedules) for that computation.

5 Auto-Scheduler

We build an auto-scheduler that, given a tensor contraction, explores the schedule space and chooses a memory- and time-efficient schedule. The main function of the scheduler is pruning the schedule space. The scheduler decides on what schedules to prune by creating a Pareto frontier of schedules using partially ordered sets of time and memory complexity.

The complete pruning pipeline is shown in Figure 8. The pipeline starts by generating schedules in the search space (§ 5.1). The following stages are divided into two parts. The first three stages are executed during compile-time with symbolic expressions (§ 5.2), and the last two stages are executed with concrete expressions at run-time (§ 5.3). We add the language support as an extension

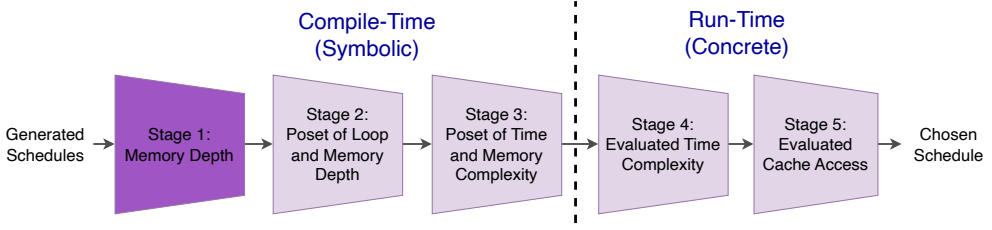


Fig. 8. Pruning stages of the auto-scheduler. Stage 1 uses an absolute measure to filter schedules without comparing them to each other. Stages 2 through 5 compare a schedule against others for pruning.

to the TACO/SparseLNR compilers. We implement the auto-scheduler in Python. The abstract schedules selected by the auto-scheduler is then described using the language definition provided in the Section 4.

5.1 Schedule Generation

For a given expression and a LIG, we generate all the loop index orders that conform to the sparse tensor access constraints. Then, we split the tensor contraction at different positions for all those index orders. Once tensor contraction is split, we infer the temporary indices and call the same function recursively for both the consumer and producer sub-computations. After those sub-computations return the consumer schedules C_{sch} and producer schedules P_{sch} , we combine those two schedule spaces as $P_{sch} \times C_{sch}$ to create super schedules that completely describe the initial computation. If the producer and consumer sections can be fused as explained in Section 4.2, we merge the sub-computations to create fused schedules, which we add to the list of schedules.

Consider the previous example (§ 3-4). First, we create different permutations of input tensors. Since tensor contractions are commutative in Einsum notation, $A(l, m, n) = B(i, j, k) * C(i, l) * D(j, m) * E(k, n)$ is equivalent to $A(l, m, n) = B(i, j, k) * E(k, n) * C(i, l) * D(j, m)$. For each of these permutations, we create permutations of indices that conform to sparse tensor access constraints. These two steps combined create the complete set of LIGs (§ 4.1). For each LIG, we split the input tensors at different positions to generate producers and consumers.

There are two ways in which we can split the input tensors. $A = B * C * D * E$ can be split as (a) $T = B * C$, and $A = T * D * E$: the result of the producer is directly used in consumer, and (b) $T1 = B * C$, $T2 = D * E$, and $A = T1 * T2$: the consumer expects results of two producers. This procedure can be repeated (*recursive application of the algorithm*) on the producer and consumer sub-computations. Out of these two ways, the first one is more interesting because it opens up avenues for loop fusion. If the producer and consumer graphs contain the same indices, then we can fuse them. Consider $A(l, m, n) = B(i, j, k) * C(i, l) * D(j, m) * E(k, n)$ with index order $l \rightarrow m \rightarrow n \rightarrow i \rightarrow j \rightarrow k$, split between C , and D . The fusion of them would result in $l \rightarrow \langle T(j, k); producer : i \rightarrow j \rightarrow k : T(j, k) + = B(i, j, k) * C(i, l), consumer : m \rightarrow n \rightarrow j \rightarrow k : A(l, m, n) + = T(j, k) * D(i, l) * E(k, n) \rangle$ (§ 4.2). After the fusion operation, we remove the fused indices in the inner computation, for example, $A(_, m, n) + = T(j, k) * D(i, _) * E(k, n)$, to recursively call the schedule generation procedure, and combine the results with the outer loops.

5.2 Symbolic Stages

Stage 1: Memory-Depth-Based Pruning The first pruning stage analyzes the dimensions of the temporary tensors used in the schedule. For example, Schedule 2a does not use any temporaries, and hence, its memory depth is 0. In Schedule 2b, the temporary $T\langle K \rangle$ has the memory depth of 1, whereas Schedules 2d and 2e have the memory depth of 2 since they employ 2D temporary tensors. If we split the computation as before to $T_{jkl} = B_{ijk} * C_{il}$ and $A_{lmn} = T_{jkl} * D_{jm} * E_{kn}$ but do not fuse

(see Figure 5b for the fused version), the memory depth would be 3. The memory depth 3 is too high for most realistic scenarios, and hence, we use it as a threshold to prune schedules like that.

The memory-depth-based heuristic goes first in the pruning pipeline because it usually discards many unrealistic schedules. At the end of this stage, we compute the symbolic iteration time and auxiliary memory complexity for each of the schedules. Then, we allocate the schedules into groups using the symbolic (time, auxiliary memory) complexity tuples.

We note that this stage can be replaced by a more sophisticated memory-volume-based pruning mechanism that uses an SMT solver. With such an approach, the user can provide a heuristic upper bound value on the total auxiliary memory use. This type of pruning would guarantee that the schedules with higher depth but lesser auxiliary memory are not pruned and the schedules with lesser depth but higher auxiliary memory are pruned. However, this would require further exploration on how to select the upper bound value which often depends on the execution environment (*i.e.*, machine parameters, such as cache size, etc.). Moreover, a memory-based pruning stage capable of reasoning about the actual volume of auxiliary memory will require the complete information about the loop bounds. Knowing either piece of information—machine parameters or loop bounds—blurs the boundary between compile-time and run-time stages and goes beyond our approach. We leave this idea for future work.

Stage 2: Poset of Loop- and Memory-Depth-Based Pruning In Section 3, we explain that using only the loop depth could prune potentially useful schedules. Therefore, at this stage, we consider both the loop depth and memory depth for pruning to create a Pareto frontier of schedules for the next stage. We use a poset to remove the schedules that are worse in terms of both loop depth and memory depth. The poset-based pruning mechanism ensures that pruned schedules contain linear loop nest schedules (with no branches), including the default TACO schedule, as long as there are no other schedules with a scalar auxiliary memory and lesser time complexity. This guarantees that we end up with a superior schedule when compared to the default schedule, if such a schedule exists. The memory depth heuristic we use in Stage 1 (Section 5.2) ensures that we do not prune schedules that are likely to have lesser loop depth than the fused simple linear loop nest schedules.

The poset-based pruning mechanism can be formally written as follows. This stage removes a schedule s from the set of schedules S (received from Stage 1) if there exists $c \in S$ such that

$$(L(s) > L(c) \wedge M(s) \geq M(c)) \vee (L(s) \geq L(c) \wedge M(s) > M(c))$$

where $L(s)$ and $M(s)$ are the loop and memory depths of the schedule s , respectively.

This type of pruning ensures that we do not remove schedules that are likely to be better in the Pareto frontier of schedules. We allocate each schedule to a different (time, memory) bucket at the end of this stage. In other words, the schedules in a bucket have the same iteration time and memory complexity but differ in the order of loops.

Stage 3: Poset of Time- and Memory-Complexity-Based Pruning Using an SMT-Solver

In some cases, the user (*e.g.*, performance engineer) may know during the compile-time some information about the loop bounds or sparsities of the tensors used in the computation. For example, if it is a graph neural network computation, the user may know that the feature size of the nodes is in the range of $[16, 256]$, or the graph size is in the order of $10M$ and the sparsity of the graph is in the range of $[0.001, 0.01]$. Then, they can provide those ranges, and the auto-scheduler can use an SMT solver to reason about the time and auxiliary memory complexities of the schedules using symbolic cost expressions that it builds for every schedule (§ 3). Note that we assume that the tensors have uniform sparsities.

There are three types of constraints that we can provide the SMT solver;

```

1 # Definition of Range (R), Inferred (I), and User-Defined (U) constraints
2 R = (i >= 1e3) ∧ (i <= 1e6) ∧ (sparsity_B >= 0.001) ∧ (sparsity_B <= 0.01) ∧ (nnz_B <= 10e4) ∧ ...
3 I = (j_pos < j) ∧ (k_pos < k) ∧ (nnz_B < i*j*k) ∧ ...
4 U = (10*j < k) ∧ ...
5
6 # Obtain time and auxiliary memory complexities of schedules in Figure 5a (s1) and Figure 5e (s2)
7 t1 = l*m*n*nnz_B; m1 = 0; t2 = l*nnz_B + l*m*k*j + l*m*k*n; m2 = j*k;
8
9 # Formulation of the Pareto frontier:
10 c1 = (t1 >= t2); c2 = (m1 > m2); c3 = (t1 > t2); c4 = (m1 >= m2)
11 cond1 = R ∧ I ∧ U ∧ ((c1 ∧ c2) ∨ (c3 ∧ c4));
12 cond2 = R ∧ I ∧ U ∧ ((¬c1 ∧ ¬c2) ∨ (¬c3 ∧ ¬c4));
13
14 if (cond1 is SAT and cond2 is UNSAT): # s1 is dominated by s2. Remove s1 from the Pareto frontier.
15 else if (cond1 is UNSAT and cond2 is SAT): # s2 is dominated by s1. Remove s2 from the Pareto frontier.
16 else: # s1 and s2 are incomparable. Keep both s1 and s2 in the Pareto frontier.

```

Listing 1. Formulation of the Pareto frontier using the SMT solver.

- (1) **Range constraints:** the range in which dense loop bounds and sparsities can vary (e.g., line 2 in Listing 1).
- (2) **Inferred constraints:** non-zero values in a sparse tensor are always less than the number of elements in its dense representation, and the non-affine loop that iterates through the sparse tensor will vary between 0 and the dense loop bound that defines the sparse tensor (e.g., line 3 in Listing 1).
- (3) **User-defined constraints:** other special constraints that the user may know about the loop bounds or sparsities. For instance, the user may know that one loop bound is twice of another (e.g., line 4 in Listing 1).

After providing the constraints known at compile-time, we check if one schedule is dominated by at least another schedule in terms of both iteration time and auxiliary memory complexity; if so, we remove that schedule from the Pareto frontier (See line 10 in Listing 1). In other words, the system removes a schedule (s) if there exists at least one schedule (c) in the schedule space such that for all possible loop bounds and sparsities, the time and memory complexities of s are worse than or equal to c and there is no set of loop bounds and sparsities for which the time and memory complexities of s are better than c . The system does not remove a schedule if there exists at least one set values of loop bounds and sparsities for which the time and memory complexities of s are better than c . This guarantees that the system does not over-prune the schedules.

This procedure can be formally written as follows. Let user-defined constraints of loop bounds and sparsities be Φ , let Z3 be the SMT solver, and the schedules from Stage 2 be S . Provide Φ to Z3. Remove s from S if $\exists c \in S$ s.t.

$\exists$ loop bounds and sparsities s.t.

$$(T(s) > T(c) \wedge N(s) \geq N(c)) \vee (T(s) \geq T(c) \wedge N(s) > N(c))$$

$\nexists$ loop bounds and sparsities s.t.

$$(T(s) \leq T(c) \wedge N(s) < N(c)) \vee (T(s) < T(c) \wedge N(s) \leq N(c))$$

Here, $T(s)$ and $N(s)$ denote the symbolic iteration time and auxiliary memory complexities of the schedule s , respectively.

An auto-scheduler could have this stage alone without the previous stage in Section 5.2. But, when any of the above conditions are *unsat*, the Z3 solver takes a long time to return. The previous stage compares a lot more schedules than this stage. Therefore, using a poset-based pruning strategy with absolute depth values, which is computationally efficient, is beneficial compared to using an SMT solver alone. Nonetheless, this stage is important because we can further reduce the number of schedules evaluated at run-time with the information available at compile-time.

Furthermore, the user could use this stage alone by removing both the memory depth-based and poset-based pruning stages. Although this removes the dependency on using memory depth as a heuristic to prune the schedules, it takes a long time for the solver to prune the schedule and does not work when the number of generated schedules is large.

5.3 Concrete Stages

Stage 4: Evaluated Time-Complexity-Based Pruning At the first stage of filtration at run-time, we evaluate the symbolic cost expressions with real values available at the run-time and select schedules that have the least iteration time complexity such that the auxiliary memory requirement is less than 50% of the last level cache (LLC) from the Pareto frontier. We take 50% as a rough margin for the selection criterion, assuming that 50% of LLC is available for the other input and output tensors in the computation. Multiple schedules with the same iteration time complexity can exist due to the same branched loop nest structure with different loop reorderings. These schedules are then passed to the next stage for further pruning.

Stage 5: Evaluated Cache-Access-Based Pruning At the second stage of run-time filtration of schedules, we prune the schedules based on cache behavior. We have included this stage here for completeness, and it is not our primary focus. Many remaining schedules may share equivalent time and memory complexity due to loop reorderings, such as the loop orders l, m , and m, l in the outer loops of Figure 2b. Since some schedules have the same time and memory complexity, if one of those schedules is not filtered away by previous stages, both of them will remain unpruned. Thus, we have a simple model that assigns a cache access cost to each schedule. This cache model takes two criteria into account. One, it looks at the leaves in the BIG and the leaf loop index. If the leaf loop index is i and if a tensor in the expression at that leaf branch has i as the last index (e.g., $B(j, i)$) or index i is not present in the tensor (e.g., $B(j, k)$), then the cost of access is zero. If i is present and not in the last accessed index (e.g., $B(i, j)$), then we take the cache access cost as J since elements are accessed J locations apart. We assign costs to all the leaves in the BIG and sum those to calculate a final cache access cost. We consider the last index of the leaves in the BIG because it has the highest impact on temporal and spatial cache locality. Two, we give precedence to the schedules that have the same index order as the loop order in the iteration graph. For instance, if tensors in the computation have $B(i, j)$ and $C(j, k)$, it would favor the loop order i, j, k over k, j, i . If both these criteria are the same for two schedules, we randomly pick one of them.

6 Evaluation

We assess SparseAuto using a collection of sparse tensor kernels in comparison to the schedules from TACO. We compare the results of SparseAuto with Pigeon [Ahrens et al. 2022] and SpTTN-Cyclops [Kanakagari and Solomonik 2023] qualitatively and quantitatively when applicable.

Experimental Setup. We conducted the experiments on a machine with four Non-Uniform Memory Access (NUMA) nodes of Intel(R) Xeon(R) CPU E5-4650 8-core processor (32-cores in total), operating at 2.70 GHz, with 32KB L1 data cache, 256KB L2 cache per core, and 80MB LLC shared between 4 NUMA nodes. Code compilation utilized GCC 11.4.0 with optimization flags -O3

Table 1. Tensors and matrices used in the evaluation from various matrix and tensor collections

Tensor	Size of file on disk	Dimensions	Non-zeros	Sparsity
bcstk17	5.4 MB	$11K \times 11K$	429K	4E-3
pdb1HYS	55.0 MB	$36K \times 36K$	4.34M	3E-3
rma10	59.0 MB	$47K \times 47K$	2.37M	1E-3
cant	57.0 MB	$62K \times 62K$	4.01M	1E-3
consph	83.0 MB	$83K \times 83K$	6.01M	9E-4
cop20k_A	27.0 MB	$12K \times 12K$	2.62M	2E-4
shipsec1	83.0 MB	$140K \times 140K$	7.81M	2E-4
scircuit	28.0 MB	$171K \times 171K$	959K	3E-5
mac_econ_fwd500	32.0 MB	$207K \times 207K$	1.27M	9E-5
webbase-1M	68.0 MB	$1.00M \times 1.00M$	3.11M	3E-6
circuit5M	2.1 GB	$5.56M \times 5.56M$	59.52M	2E-6
vast-2015-mc1-3d	431.0 MB	$165K \times 11K \times 2$	26.02M	8.36E-08
darpa1998	575.0 MB	$22K \times 22K \times 23.7M$	28.42M	2.50E-06
nell-2	1.5 GB	$12K \times 9K \times 288K$	76.88M	5.73E-05
flickr-3d	2.6 GB	$320K \times 2.82M \times 1.60M$	112.89M	3.92E-11

--ffast-math. The process involved a warm-up run, followed by 31 executions of the kernel computation. The results reported are the median values, accompanied by the corresponding standard deviation across the 31 runs. Parallel executions were performed on 32 threads using OpenMP.

Datasets. In the evaluation, we employ numerous real-world tensors sourced from the SuiteSparse Collection [Davis and Hu 2011], Network Repository [Rossi et al. 2015], Formidable Repository of Open Sparse Tensors and Tools [Smith et al. 2017], and the 1998 DARPA Intrusion Detection Evaluation Dataset [Lippmann et al. 2000]. The tensors and matrices used in the evaluation are shown in Table 1. These tensors span a wide range of sizes and sparsities. Sparse inputs to the kernels used the Compressed Sparse Fiber (CSF) format.

Kernels. We compare the performance of SparseAuto and TACO using kernels in Table 2. The kernel naming conventions are as follows: $\langle SDDMM, SpMM \rangle$ indicates that the kernel is a combination of *SDDMM* and *SpMM*, and the kernel can be decomposed into these two sub-kernels, each capable of being executed sequentially. The evaluation incorporates various combinations of the following kernels. *SDDMM* Sampled Dense-Dense Matrix Multiplication and *SpMM* Sparse Matrix-Matrix Multiplication are used in graph neural networks. In this context, the *SDDMM* operation is used in computing attention values along the edges of a graph, then *SpMM* is used after the *SDDMM* operation to transform the feature vector of each node, and the *GEMM* operation is used for multiplication with a weight matrix [Dias et al. 2022]. $\langle 3D\ TTMC \rangle$ Tensor-Times Matrix Contractions are used in Tucker Decompositions [Tucker 1966]. Matrizied Tensor Times Khatri-Rao product (*MTTKRP*) is used in sparse computations such as signal processing and computer vision [Choi et al. 2018]. Sparse Tensor Times Matrix (*SpTTM*) operation is used in data mining and data analytics applications and is a sub-computation in Tucker Decomposition [Tucker 1966].

Number of schedules and overheads of each stage. Table 3 shows the schedule counts of each stage in the pruning pipeline, and Table 4 shows the corresponding execution times for each of these stages. These tables expose a correlation between execution times and the number of schedules to process. Also, Table 4 shows that Depth Poset-based pruning (Stage 2) helps to save on expensive SMT work (Stage 3) because the column Stage 3 (Skipping Stage 2) is always longer than Stage 2 and 3 combined.

Table 2. Chosen schedules after the SMT solver-based pruning stage. Naming convention: $\mathbf{B}$ denotes sparse tensor B , and $\mathbf{j}'$ denotes the index of a non-affine loop. Different kernels inside the angle brackets denote that the fused computation can be separated into those kernels. The inner branches of the loop nests are written as $\langle \text{Temporary}; \text{Producer}, \text{Consumer} \rangle$.

Kernel	Description	Chosen Schedules After Z3 Pruning
① : $\langle \text{SDDMM}, \text{SpMM} \rangle$	$A_{il} = \sum_{jk} \mathbf{B}_{ij} C_{ik} D_{jk} E_{jl}$	$i, \mathbf{j}' \langle t; k : t+ = \mathbf{B}_{ij} C_{ik} D_{jk}, l : A_{il}+ = t E_{jl} \rangle$ $i \langle T_i; \mathbf{j}' \langle t; k : t+ = \mathbf{B}_{ij} C_{ik} D_{jk}, l : T_l+ = t E_{jl} \rangle, m, l : A_{im}+ = T_l F_{lm} \rangle$
② : $\langle \text{SDDMM}, \text{SpMM}, \text{GEMM} \rangle$	$A_{im} = \sum_{jkl} \mathbf{B}_{ij} C_{ik} D_{jk} E_{jl} F_{lm}$	$i, \mathbf{j}' \langle t; k : t+ = \mathbf{B}_{ij} C_{ik} D_{jk}, m, l : A_{il}+ = t E_{jl} F_{lm} \rangle$ $i, l \langle t; \mathbf{j}', k : t+ = \mathbf{B}_{ij} C_{ik} D_{jk} E_{jl}, m, l : A_{il}+ = t F_{lm} \rangle$
③ : $\langle \text{SpMMH}, \text{GEMM} \rangle$	$A_{il} = \sum_{jk} \mathbf{B}_{ij} C_{jk} D_{jk} E_{kl}$	$i, \mathbf{j}' \langle t; k : t+ = \mathbf{B}_{ij} C_{jk} D_{jk}, l : A_{il}+ = t E_{jl} \rangle$
④ : $\langle \text{SpMM}, \text{GEMM} \rangle$	$A_{il} = \sum_{jk} \mathbf{B}_{ij} C_{jk} D_{kl}$	$i, k \langle t; \mathbf{j}' : t+ = \mathbf{B}_{ij} C_{jk}, l : A_{il}+ = t D_{kl} \rangle$
⑤ : $\langle \text{3D TTMC} \rangle$	$A_{lmn} = \sum_{ijk} \mathbf{B}_{ijk} C_{il} D_{jm} E_{kn}$	$i, \mathbf{j}', n \langle t; \mathbf{k}' : t+ = \mathbf{B}_{ijk} E_{kn}, m, l : A_{lmn}+ = t C_{il} D_{jm} \rangle$ $i, n \langle T_m; \mathbf{j}' \langle t; \mathbf{k}' : t+ = \mathbf{B}_{ijk} E_{kn}, m : T_m+ = t D_{jm} \rangle, m, l : A_{lmn}+ = T_m C_{il} \rangle$ $i, m, n \langle t; \mathbf{j}', \mathbf{k}' : t+ = \mathbf{B}_{ijk} D_{jm} E_{kn}, m, l : A_{lmn}+ = t C_{il} \rangle$
⑥ : $\langle \text{SpTTM}, \text{TTM} \rangle$	$A_{ilm} = \sum_{jk} \mathbf{B}_{ijk} C_{jl} D_{km}$	$i, \mathbf{j}' m \langle t; \mathbf{k}' : t+ = \mathbf{B}_{ijk} D_{jk}, l : A_{il}+ = t C_{jl} \rangle$
⑦ : $\langle \text{SpTTM}, \text{SpTTM} \rangle$	$A_{ijm} = \sum_{jk} \mathbf{B}_{ijk} C_{kl} D_{lm}$	$i, \mathbf{j}' l \langle t; \mathbf{k}' : t+ = \mathbf{B}_{ijk} C_{kl}, m : A_{il}+ = t D_{lm} \rangle$
⑧ : $\langle \text{MTTKRP}, \text{GEMM} \rangle$	$A_{im} = \sum_{jk} \mathbf{B}_{ikl} C_{lj} D_{kj} E_{jm}$	$i, \mathbf{j}' \langle t; \mathbf{k}' l : t+ = \mathbf{B}_{ijk} C_{kl} D_{kj}, m : A_{il}+ = t E_{jm} \rangle$

Table 3. The number of schedules after each stage in the pruning pipeline. The numbers in the parenthesis denote the number of different (time complexity, auxiliary memory complexity) pairs. Stage 3 (Skipping Stages 1 & 2) is time-limited to 24 hours per kernel.

Kernel	Generated Schedules	Stage 1 Mem Depth	Stage 2 Depth Poset	Stage 3 SMT Solver	Stage 3 (Skipping Stage 2)	Stage 3 (Skipping Stages 1 & 2)
① :	16 169	1472 (255)	1 (1)	1 (1)	1 (1)	1 (1)
② :	145 448 232	207 129 (18 277)	224 (43)	8 (3)	32 (4)	timeout
③ :	7426	692 (133)	2 (1)	2 (1)	2 (1)	2 (1)
④ :	258	128 (34)	2 (1)	2 (1)	2 (1)	2 (1)
⑤ :	14 701 776	30 203 (2541)	101 (26)	16 (3)	16 (3)	timeout
⑥ :	2561	352 (60)	3 (1)	3 (1)	3 (1)	3 (1)
⑦ :	109	46 (13)	1 (1)	1 (1)	1 (1)	1 (1)
⑧ :	58 127	4715 (728)	5 (2)	2 (1)	2 (1)	timeout

Table 5 shows the time taken for the two run-time stages, including the code generation and compilation times. While we execute the codegen and compilation at run-time (for SparseAuto and TACO alike), both can be done offline, at compile-time, as an optimization. The optimization can work by maintaining a mapping from schedules chosen at compile-time to the corresponding compiled functions. Using this mapping, we can lookup the code for the schedule we deem the best. Ultimately, the time taken for the codegen and compilation is not a concern in practice.

Table 4. Time taken by each compile-time stage. Stage 3 (Skipping Stages 1 & 2) has the timeout of 24 hours.

Kernel	Schedule Generation (16 threads)	Stage 1 Mem Depth	Stage 2 Depth Poset	Stage 3 SMT Solver	Stage 3 (Skipping Stage 2)	Stage 3 (Skipping Stages 1 & 2)
① :	631.4 ms	13.0 ms	1723.2 ms	121.5 ms	2877.4 ms	5.6 s
② :	10740.5 s	167.5 s	454.1 s	1.5 s	1538.9 s	timeout
③ :	475.9 ms	3.7 ms	896.7 ms	48.0 ms	2623.4 ms	1.7 s
④ :	54.6 ms	0.5 ms	56.6 ms	49.7 ms	327.0 ms	0.8 s
⑤ :	864.3 s	71.9 s	25.8 s	1.5 s	4567.1 s	timeout
⑥ :	304.6 ms	6.2 ms	238.2 ms	50.0 ms	1244.2 ms	5.4 s
⑦ :	35.3 ms	0.3 ms	46.6 ms	48.3 ms	486.7 ms	0.9 s
⑧ :	4.2 s	57.8 ms	4.7 s	123.2 ms	204.1 s	timeout

Table 5. Time taken by each run-time stage including the code generation and compilation times.

Kernel	Run-time Filtration			Build Time		
	Stage 4 (us)	Stage 5 (us)	Total (us)	Codegen (ms)	Compile (ms)	Total (ms)
① :	185.2	111.1	296.2	10.9	163.4	174.3
② :	265.1	94.6	359.7	12.0	364.2	376.1
③ :	159.6	111.3	270.9	12.1	174.4	186.5
④ :	161.6	125.9	287.5	12.1	174.6	186.8
⑤ :	220.3	209.4	429.7	16.5	251.6	268.1
⑥ :	158.0	115.9	274.0	14.9	205.2	220.1
⑦ :	198.0	82.3	280.3	11.6	189.3	200.8
⑧ :	198.0	101.6	299.6	15.2	173.0	188.2

6.1 Performance Comparison with TACO

Table 2 shows the selected kernels after the compile-time pruning stages. Table 3 shows the number of schedules after each stage in the pruning pipeline. Furthermore, we bypass the second stage in the pruning pipeline and directly apply the SMT solver-based pruning in Stage 3 to the output from Stage 1. We observe that for kernel ②, the number of schedules spared when Stage 2 is bypassed is 32 compared to the 8 schedules spared with Stage 2. For other kernels, the number of final schedules is the same with or without Stage 2. This indicates the effectiveness of the Depth Poset-based pruning in Stage 2. We also see that some of the schedules in Stage 2 are pruned in Stage 3, indicating the effectiveness of the SMT solver-based pruning in Stage 3.

Figure 9 shows the execution times and speedups of the selected schedules against the default TACO schedule. We observe orders of magnitude better performance compared to TACO. Although we do not reason about the effects of parallel execution in our auto-scheduler, we report the parallel performance of schedules by parallelizing the outer loops using OpenMP for completeness. We observe that parallel executions of the schedules have similar gains over TACO. We report only the serial execution times for $\langle SpTTM, SpTTM \rangle$ because the output of the kernel is sparse.

6.2 Performance Comparison with Auto-Schedulers from Prior Work

Comparison with Pigeon [Ahrens et al. 2022]. Pigeon introduces an auto-scheduler based on the time complexity of the schedule. They explore the search space with data layout transforms and transposes of sparse tensors, targetting an offline schedule selection. Given A_{ij} , they would consider schedules having both A_{ij} , and A_{ji} , with corresponding index orders of i, j and j, i in

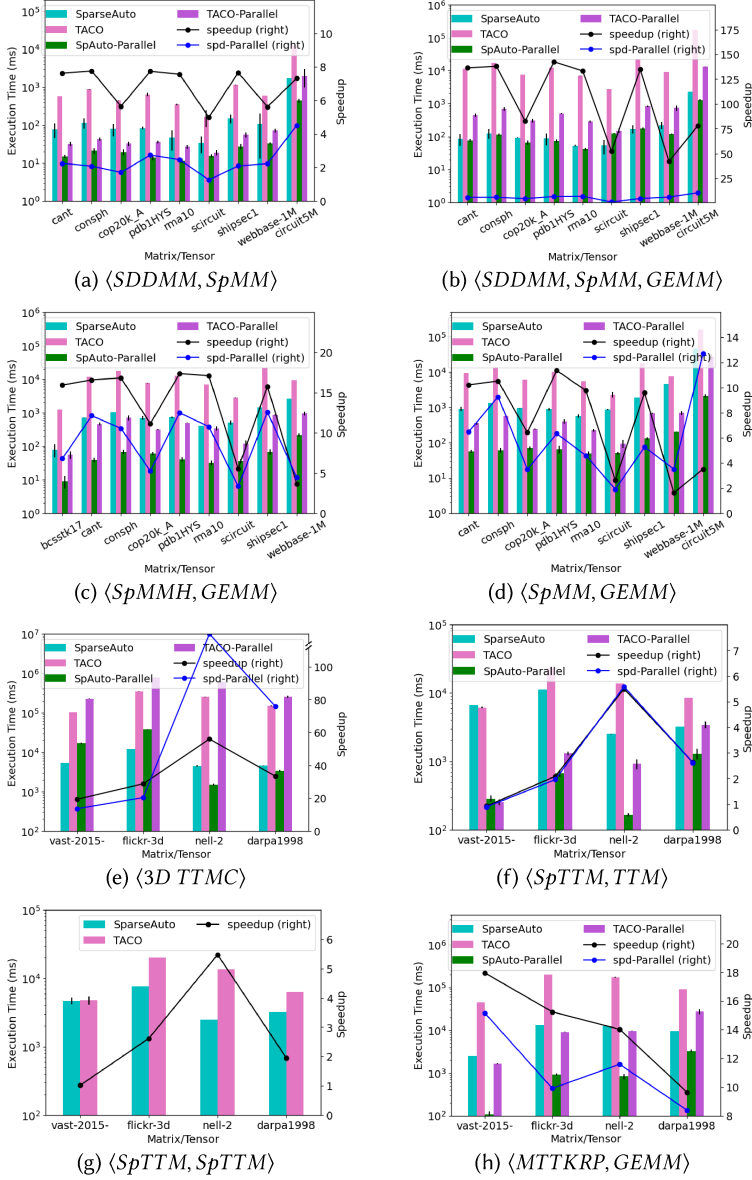


Fig. 9. Performance Comparison with TACO.

the generated schedules, whereas SparseAuto does not explore the schedules having the index order of j, i because this requires original A_{ij} to be transposed. We remove the schedules with transpositions in Pigeon to make a fair comparison in this study.

Considering the schedule space without transpositions, we search a larger space because of the recursive application of loop/kernel fusion/fission. Pigeon only explores one level of imperfectly nested loops. $\langle TTM \rangle$ and $\langle SDDMM, SpMM, GEMM \rangle$ kernels in Table 2 contains schedules with multiple levels of imperfect nesting. However, we could not compare the performance of these two kernels against Pigeon as their schedule generation timed out after 48 hours.

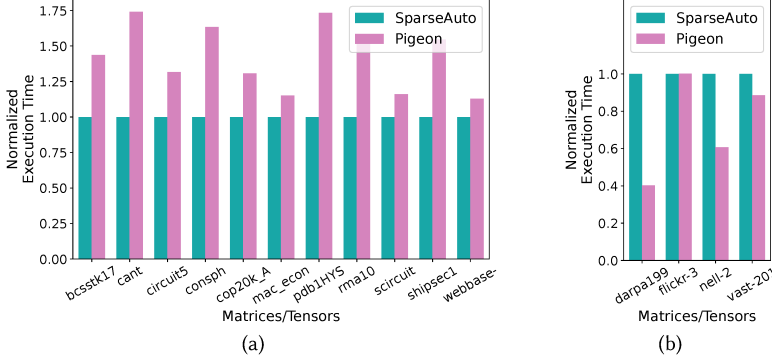


Fig. 10. Performance comparison of SparseAuto and Ahrens *et al.* [Ahrens et al. 2022] for $\langle SpMM, GEMM \rangle$ and $\langle SpTTM, SpTTM \rangle$ kernels.

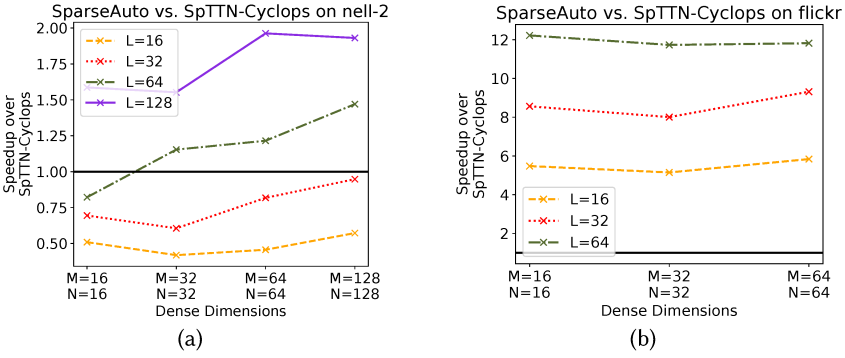


Fig. 11. Performance Comparison with SpTTN-Cyclops [Kanakagari and Solomonik 2023] of TTM kernel by varying dense dimensions L , M , and N .

$\langle SDDMM, SpMM \rangle$ kernel gave similar performance for both SparseAuto and Pigeon. We could not compare against $\langle SpMMH, GEMM \rangle$, $\langle MTKRP, GEMM \rangle$, $\langle SpTTM, TTM \rangle$ due to reasons such as all selected schedules that can be evaluated on TACO having data layout transforms and transposes, incorrect schedules and errors according to our experiments. We compare the performance of $\langle SpMM, GEMM \rangle$, and $\langle SpTTM, SpTTM \rangle$ kernels in Figure 10. We observe that SparseAuto outperforms Pigeon in $\langle SpMM, GEMM \rangle$ kernel, and Pigeon outperforms SparseAuto in $\langle SpTTM, SpTTM \rangle$ kernel. In $\langle SpTTM, SpTTM \rangle$, the innermost loop is the non-affine loop in SparseAuto selected schedule. Hence, SparseAuto schedule has worse cache access patterns compared to the Pigeon schedule.

Comparison with SpTTN-Cyclops [Kanakagari and Solomonik 2023]. This case study shows the effect of auxiliary memory on performance. We contrast our chosen schedule with SpTTN-Cyclops's selected schedule of the $\langle 3D TTM \rangle$ kernel, and evaluate on the flickr and nell-2 datasets (refer to Figure 11). Their auto-scheduler, not optimized for memory, results in a schedule $i \langle T2_{mn}; j' \langle T1_n; k', n : T1_n + = B_{ijk} E_{kn}, m, n : T2_{mn} + = T1_n D_{jm} \rangle; l, m, n : A_{lmn} + = T2_{mn} C_{il} \rangle$ with one 2D and one 1D intermediate temporaries. In contrast, our schedule $i, n \langle T_m; j' \langle t; k' : t + = B_{ijk} E_{kn}, m : T_m + = t D_{jm} \rangle; m, l : A_{lmn} + = T_m C_{il} \rangle$ utilizes only one scalar and one 1D intermediate temporaries. Our schedule tends to outperform when temporary sizes (dictated by M and N dimensions) are large and temporaries are accessed more frequently (dictated by L). For smaller temporaries and fewer temporary access frequencies, SpTTN-Cyclops tends to perform better. It's

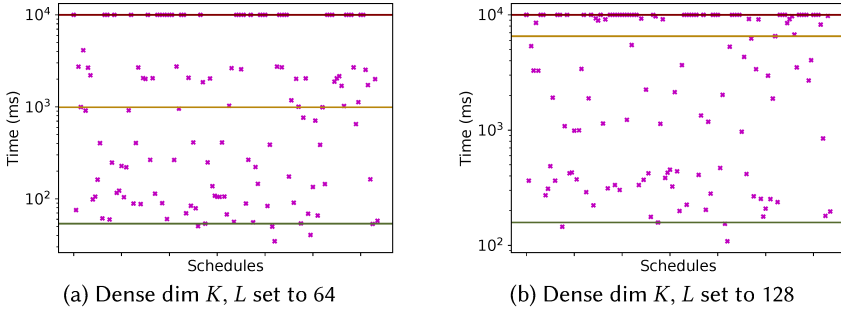


Fig. 12. Performance Comparison of SparseAuto with all of the other schedules for $\langle SpMM, GEMM \rangle$ using bcsstk17. The bottom, middle, and top lines correspond to the execution times of the SparseAuto, the default TACO schedule, and the timeout.

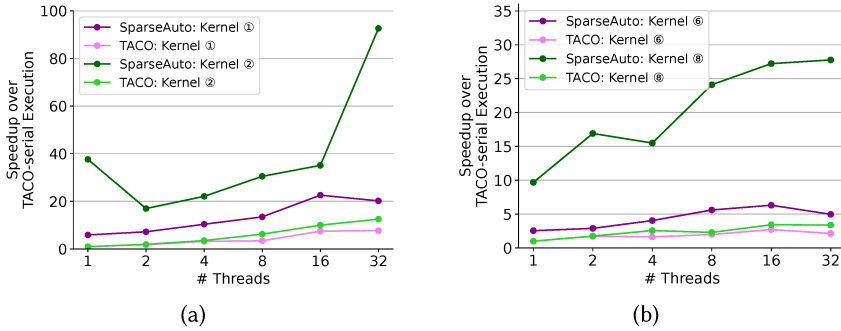


Fig. 13. Scaling of the SparseAuto w.r.t. TACO serial.

important to note that both schedules share the same iteration time complexity, with speedup differences arising from cache accesses. SpTTN-Cyclops maps computations to BLAS calls, a detail omitted in our evaluation.

6.3 Global Schedule Comparison, Scalability, and the Effect of Transposition

Comparison of performance against all schedules. We assess the performance of our chosen schedule in comparison to all other schedules illustrated in Figure 12 for a kernel with fewer schedule options, and for a smaller matrix. SparseAuto-selected schedule emerges as one of the top-performing schedules.

Scalability. We report the scalability results for completeness even though our auto-scheduler does not consider parallelization. The SparseAuto-selected schedules scale comparably to schedules generated by TACO, see Figure 13. Figure 13a and Figure 13b are generated using Webbase-1M and darpa1998, respectively. Scaling is weak in cases with small dense dimensions (e.g., 16) but improves with larger dense dimensions.

Effect of transpositions on performance. SparseLNR [Dias et al. 2022] selects the schedule $i \langle T_k, j'k : T_k + = \mathbf{B}_{ij} C_{jk}, lk : A_{il} + = T_k D_{lk} \rangle$ with an additional 1D auxiliary memory for the kernel $\langle SpMM, GEMM \rangle$. Notice that the transposed D_{kl} was used here as opposed to D_{lk} in our schedule. SparseAuto chosen schedule surpasses SparseLNR in terms of auxiliary memory efficiency, as our schedule in Table 2 utilizes only a single extra scalar memory. We transpose C_{jk} and D_{kl} and evaluate against SparseLNR. While SparseLNR schedule with 1D auxiliary memory outperforms ours in cases like $A_{il} = \sum_{jk} \mathbf{B}_{ij} C_{jk} D_{lk}$, and $A_{il} = \sum_{jk} \mathbf{B}_{ij} C_{jk} D_{kl}$, SparseAuto schedule with scalar

Table 6. Auxiliary memory requirements for different kernels. The right four columns show the number of elements required to store the intermediate results. The ‘—’ label shows that the given schedule is not available with the given framework.

Kernel	Description	Auxiliary Memory Requirements			
		TACO	SpAuto	Cyclops	Pigeon
① : $\langle SDDMM, SpMM \rangle$	$A_{il} = \sum_{jk} \mathbf{B}_{ij} C_{ik} D_{jk} E_{jl}$	0	1	—	—
② : $\langle SDDMM, SpMM, GEMM \rangle$	$A_{im} = \sum_{jkl} \mathbf{B}_{ij} C_{ik} D_{jk} E_{jl} F_{lm}$	0	1 to $1 + L$	—	—
③ : $\langle SpMMH, GEMM \rangle$	$A_{il} = \sum_{jk} \mathbf{B}_{ij} C_{jk} D_{jk} E_{kl}$	0	1	—	—
④ : $\langle SpMM, GEMM \rangle$	$A_{il} = \sum_{jk} \mathbf{B}_{ij} C_{jk} D_{kl}$	0	1	—	K
⑤ : $\langle 3D\ TTMC \rangle$	$A_{lmn} = \sum_{ijk} \mathbf{B}_{ijk} C_{il} D_{jm} E_{kn}$	0	1 to $1 + M$	$N + M * N$	—
⑥ : $\langle SpTTM, TTM \rangle$	$A_{ilm} = \sum_{jk} \mathbf{B}_{ijk} C_{jl} D_{km}$	0	1	—	—
⑦ : $\langle SpTTM, SpTTM \rangle$	$A_{ijm} = \sum_{jk} \mathbf{B}_{ijk} C_{kl} D_{lm}$	0	1	—	L
⑧ : $\langle MTTKRP, GEMM \rangle$	$A_{im} = \sum_{jk} \mathbf{B}_{ikl} C_{lj} D_{kj} E_{jm}$	0	1	—	—

Table 7. Performance with changing auxiliary memory sizes of TTMC kernel. We do not evaluate the instances marked with ‘—’ due to very long execution times (*i.e.*, timeout).

Dense Dims L, M, N	Aux. Mem. (B)		nell-2			flickr		
	SpAuto	Cyclops	SpAuto Time (s)	Cyclops Time (s)	Speedup	SpAuto Time (s)	Cyclops Time (s)	Speedup
16, 16, 16	68	1088	4.4	2.2	0.5x	12.3	67.4	5.5x
32, 16, 16	68	1088	4.3	3.0	0.7x	15.2	130.1	8.6x
64, 16, 16	68	1088	5.6	4.6	0.8x	20.9	254.8	12.2x
128, 16, 16	68	1088	5.2	8.2	1.6x	33.0	542.7	16.4x
16, 32, 32	132	4224	13.4	5.6	0.4x	40.6	208.8	5.2x
32, 32, 32	132	4224	13.8	8.3	0.6x	54.3	434.5	8.0x
64, 32, 32	132	4224	15.1	17.5	1.2x	88.9	1042.7	11.7x
128, 32, 32	132	4224	17.6	27.4	1.6x	152.6	2063.8	13.5x
16, 64, 64	260	16640	36.3	16.6	0.5x	170.7	996.9	5.8x
32, 64, 64	260	16640	38.9	31.8	0.8x	213.6	1990.0	9.3x
64, 64, 64	260	16640	43.4	52.8	1.2x	334.4	3952.8	11.8x
128, 64, 64	260	16640	52.6	103.3	2.0x	—	—	—
16, 128, 128	516	66048	97.5	55.9	0.6x	—	—	—
32, 128, 128	516	66048	108.6	102.9	1.0x	—	—	—
64, 128, 128	516	66048	136.6	200.8	1.5x	—	—	—
128, 128, 128	516	66048	221.1	426.9	1.9x	—	—	—

auxiliary memory excels in instances like $A_{il} = \sum_{jk} \mathbf{B}_{ij} C_{kj} D_{kl}$, and $A_{il} = \sum_{jk} \mathbf{B}_{ij} C_{kj} D_{lk}$. The discrepancy arises from cache access effects with transposed matrices. Addressing cache misses and access patterns would require the auto-scheduler to delve into intricate details, surpassing the scope of this paper. We identify this as potential future work.

6.4 Effect of Auxiliary Memory on Performance

This section analyses the auxiliary memory requirements of the selected schedules in each of the different frameworks. The auxiliary memory requirements are shown in Table 6. The default TACO schedule does not use any auxiliary memory because it generates perfectly nested loops (*i.e.*, linear). Schedules generated by SparseAuto require auxiliary memory no more than the other frameworks except the default TACO schedules.

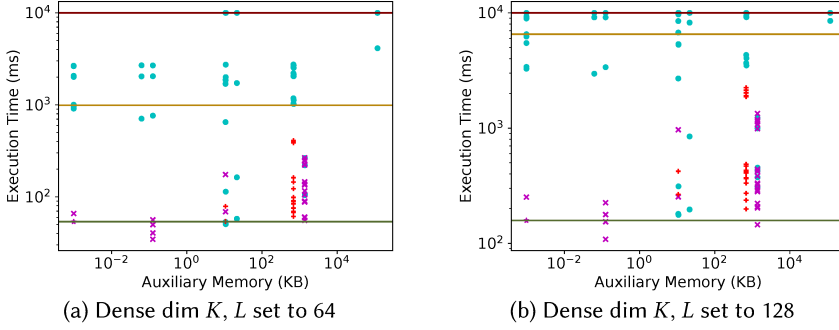


Fig. 14. Auxiliary Memory Usage vs. Execution Time for $\langle SpMM, GEMM \rangle$ kernel. The schedule chosen by SparseAuto is marked with a '*' in magenta. The schedules with the same time complexity as '*' are shown with 'x' markers in magenta. The schedules with the lowest time complexity are shown with '+' markers in red. The dot markers in cyan denote the other schedules. The bottom, middle and top horizontal lines mark the execution times of the schedule chosen by SparseAuto, default TACO, and the timeout limit, respectively.

Table 7 shows the performance of SparseAuto vs. SpTTN-Cyclops when the dense dimension sizes are varied in the kernels. Generally, the SparseAuto schedule outperforms the SpTTN-Cyclops schedule when the dense dimension bounds are higher. Notably, the dimension bound L dictates the number of times the auxiliary memory is passed between the producer and consumer. The performance varies between the two schedules more when the value of L is higher. Furthermore, doubling M and N quadruples the auxiliary memory in the SpTTN-Cyclops schedule, making it less efficient than the SparseAuto schedule for larger dense dimension bounds.

Figure 14 shows that the chosen schedule uses the lowest auxiliary memory compared to the other schedules while delivering top performance. Many schedules have the same time complexity units as the schedule chosen by SparseAuto, but they have different sizes of auxiliary memory. By considering both time and memory complexities together, we can see that the number of schedules evaluated at run-time is reduced significantly. The schedules having the lowest time complexity (shown in red '+' markers) use much more auxiliary memory than most other schedules.

Figure 15 shows the same set of schedules as Figure 14 but using concrete time complexity on the X-axis. Since there are many schedules with the lowest time complexity, if the system were to keep those schedules during the compile-time, a larger number of schedules would be evaluated at run-time, which would increase overhead. The schedules with the lowest time complexity perform worse than those chosen by SparseAuto. This experiment shows that auxiliary memory usage is important to consider in addition to time complexity to select the best schedule.

6.5 Discussion on the Effect of Transposition

Our framework assumes that transposed versions of sparse tensors are not available at run-time. Hence, we only consider loop orders that do not violate the original tensors' sparse access constraints. For example, considering the kernel $\langle SDDMM, SpMM \rangle$, $A_{il} = \sum_{jk} B_{ij} C_{ik} D_{jk} E_{jl}$, we only consider the loop orders that have i and j in that order when the inner computation contains the sparse matrix B_{ij} . However, if the transposed version of B_{ij} , which is B_{ji} , is available at run-time, the loop orders with j and i in that order can also be considered. This is a limitation of our framework.

A more advanced version of our auto-scheduler could consider the time and auxiliary memory it takes to transpose the sparse tensors and include it in the symbolic complexities of schedules. The transposition cost could depend on the sparse tensor format as well as the transposition algorithm. Taking a step further, the auto-scheduler could even consider transposing the dense

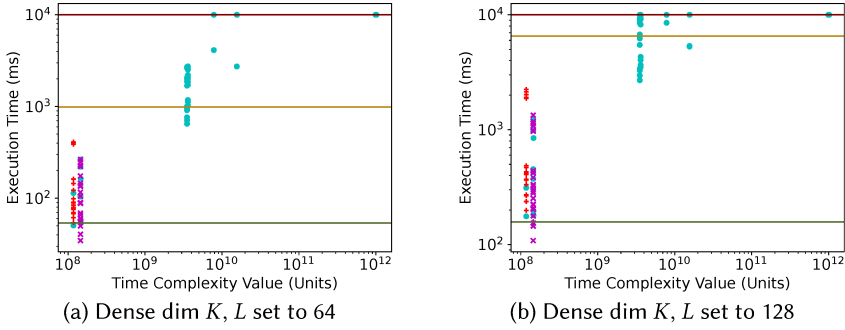


Fig. 15. Calculated Time Complexity vs. Execution Time for $\langle SpMM, GEMM \rangle$ kernel. Schedules marked by '+' has the lowest calculated time complexity. The schedules having the same memory complexity as the chosen schedule are shown as 'x' markers. The schedule chosen by SparseAuto is marked with a '*'.

tensors. However, this would require a more complex framework that can reason about the effects of transpositions on the performance of the schedules. This is a potential future work.

7 Related Work

Sparse tensor contractions and compilers Various works have delved into dense and sparse tensor contractions within the domains of tensor compilers, compiler optimizations, and targeted optimizations for specific kernels.

For dense tensor algebra, extensive research [Allam et al. 2006; Cociorva et al. 2003; Sahoo et al. 2005] has focused on CPU optimizations in memory-constrained environments. Dense transformations are comparatively straightforward due to the absence of structural or sparse access pattern constraints. GPU optimizations for dense tensor computations have been explored in works like [Abdelfattah et al. 2016; Kim et al. 2019; Nelson et al. 2015]. However, these approaches do not apply to sparse tensor computations, given the challenges posed by the intricacies of sparse data structures due to not having random access and non-affine loops.

The Tensor Contraction Engine (TCE)[Auer et al. 2006] addresses dense tensor computations by generating code to fit available memory, utilizing a feedback loop to minimize memory. Our approach, in contrast, relies on a poset-based mechanism. Other works[Hartono et al. 2009; Lam et al. 1997] adopt similar optimizations for dense tensors. Johnnie et al. [Gray and Kourtis 2021] approach the tensor contraction problem as a graph problem, emphasizing dense tensor contractions.

The Sparse Polyhedral Framework [LaMielle and Strout 2010; Strout et al. 2018, 2016] utilizes an inspector-executor strategy to transform the data layout and schedule sparse computations, aiming to enhance both locality and parallelism. Athena [Liu et al. 2021a] and Sparta [Liu et al. 2021b] are methodologies that offer highly optimized kernels for sparse tensor operations and contraction sequences. However, they lack support for recursive loop nest restructuring for arbitrary sparse tensor expressions.

General sparse tensor algebra compilers such as TACO [Kjolstad et al. 2017], COMET [Tian et al. 2021], and Sparsifier [Bik et al. 2022] in MLIR, focus on generating code for sparse tensor computations. However, they lack support for nested multiple levels of loop branches and mechanisms for exploring the search space. SparseTIR [Ye et al. 2023], SparseLNR [Dias et al. 2022], and ReACT [Zhou et al. 2023] can generate fused sparse loops but are limited in supporting arbitrary loop nests with multiple branches and exploring the search space.

Auto-schedulers for sparse tensor contractions Pigeon [Ahrens et al. 2022] introduce an auto-scheduler emphasizing loop depth and later utilize an asymptotic cost model for search space

pruning. Their system does not optimize for both time and auxiliary memory complexities, operates completely offline, executes multiple schedules at the last stage, in other words they design the system for complete offline schedule selection, their search space exploration algorithm does not explore the schedules with multi-level branch nests, and lacks the use of user-defined constraints at compile time for search space pruning. Although they introduce a good cost model, their system has the disadvantages described in Section 3. Their framework, evaluated on TACO, faces limitations in supporting intermediate temporaries with more than one dimension and includes schedules with data layout transformations in their auto-scheduler.

SpTTN-Cyclops [Kanakagari and Solomonik 2023] presents another auto-scheduler for sparse tensor contractions, offering a fully automated framework without user intervention in schedule selection. Unlike our approach, they do not emphasize poset-based pruning and opt for minimum loop depth schedules and then a maximum number of dense loops, which may not always be optimal, as discussed in Section 3. They lack support for user-defined constraints using an SMT solver to analyze schedule complexities for search space pruning. Their run-time loop generation algorithm affects evaluation time, while our method minimizes the number of schedules evaluated during run time.

8 Discussion and Conclusion

Auto-scheduling is a challenging problem due to the vast number of potential schedules — ranging from thousands to hundreds of thousands — for a given computation. Factors such as time complexity, memory usage, cache behavior, and parallelism must all be considered. Most systems rely on heuristic-based approaches or empirical evaluations to identify optimal schedules. We advocate for a systematic approach that dedicates considerable time to offline schedule generation and analysis; by investing hours in this process, most schedules can be eliminated, leaving only a few for evaluation at run-time. This viewpoint suggests that *scheduling as a service* (SchaaS) could benefit expensive computations, particularly scientific workloads, and lead to faster compute times and more efficient resource utilization.

We have introduced SparseAuto, a framework for recursive loop nest restructuring, including a scheduling language for sparse tensor contractions. An auto-scheduler for sparse tensor contractions is implemented, leveraging the said scheduling language to generate schedules. Among the many factors influencing schedule performance, we focus on two machine-independent criteria: time complexity and auxiliary memory usage, arising from variations in loop structures within sparse tensor contractions. SparseAuto employs a poset-based approach to prune the search space and utilizes an SMT solver for analyzing the symbolic cost of a schedule. Our findings demonstrate that SparseAuto delivers noteworthy performance enhancements.

Data Availability Statement

The paper is accompanied by the artifact [Dias et al. 2024] that contains the source code of SparseAuto, the benchmarks, and the scripts to reproduce the results presented in the paper.

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References

- A. Abdelfattah, M. Baboulin, V. Dobrev, J. Dongarra, C. Earl, J. Falcou, A. Haidar, I. Karlin, Tz. Kolev, I. Masliah, and S. Tomov. 2016. High-performance Tensor Contractions for GPUs. *Procedia Computer Science* 80 (2016), 108–118. <https://doi.org/10.1016/j.procs.2016.05.302> International Conference on Computational Science 2016, ICCS 2016, 6–8 June 2016, San Diego, California, USA.
- Willow Ahrens, Fredrik Kjolstad, and Saman Amarasinghe. 2022. Autoscheduling for Sparse Tensor Algebra with an Asymptotic Cost Model. In *Proceedings of the 43rd ACM SIGPLAN International Conference on Programming Language Design and Implementation* (San Diego, CA, USA) (*PLDI 2022*). Association for Computing Machinery, New York, NY, USA, 269–285. <https://doi.org/10.1145/3519939.3523442>
- A. Allam, J. Ramanujam, G. Baumgartner, and P. Sadayappan. 2006. Memory minimization for tensor contractions using integer linear programming. In *Proceedings 20th IEEE International Parallel Distributed Processing Symposium*. 8 pp.–. <https://doi.org/10.1109/IPDPS.2006.1639717>
- Alexander A. Auer, Gerald Baumgartner, David E. Bernholdt, Alina Bibireata, Daniel Cociorva Venkatesh Choppella, Xiaoyang Gao, Robert Harrison, Sandhya Krishnan Sriram Krishnamoorthy, Chi-Chung Lam, Qingda Lu, Marcel Nooijen, Russell Pitzer, J. Ramanujam, P. Sadayappan, and Alexander Sibiryakov. 2006. Automatic code generation for many-body electronic structure methods: the tensor contraction engine. *Molecular Physics* 104, 2 (2006), 211–228. <https://doi.org/10.1080/00268970500275780>
- Aart Bik, Penporn Koanantakool, Tatiana Shpeisman, Nicolas Vasilache, Bixia Zheng, and Fredrik Kjolstad. 2022. Compiler Support for Sparse Tensor Computations in MLIR. *ACM Trans. Archit. Code Optim.* 19, 4, Article 50 (sep 2022), 25 pages. <https://doi.org/10.1145/3544559>
- Aart J. C. Bik and Harry A. G. Wijshoff. 1993. Compilation Techniques for Sparse Matrix Computations. In *Proceedings of the 7th International Conference on Supercomputing* (Tokyo, Japan) (*ICS '93*). Association for Computing Machinery, New York, NY, USA, 416–424. <https://doi.org/10.1145/165939.166023>
- Jee Choi, Xing Liu, Shaden Smith, and Tyler Simon. 2018. Blocking Optimization Techniques for Sparse Tensor Computation. In *2018 IEEE International Parallel and Distributed Processing Symposium (IPDPS)*. 568–577. <https://doi.org/10.1109/IPDPS.2018.00066>
- Stephen Chou, Fredrik Kjolstad, and Saman Amarasinghe. 2018. Format Abstraction for Sparse Tensor Algebra Compilers. *Proc. ACM Program. Lang.* 2, OOPSLA, Article 123 (oct 2018), 30 pages. <https://doi.org/10.1145/3276493>
- D. Cociorva, Xiaoyang Gao, S. Krishnan, G. Baumgartner, Chi-Chung Lam, P. Sadayappan, and J. Ramanujam. 2003. Memory-Constrained Data Locality Optimization for Tensor Contractions. In *Proceedings International Parallel and Distributed Processing Symposium*. 8 pp.–. <https://doi.org/10.1109/IPDPS.2003.1213121>
- Timothy A. Davis and Yifan Hu. 2011. The University of Florida Sparse Matrix Collection. *ACM Trans. Math. Softw.* 38, 1, Article 1 (dec 2011), 25 pages. <https://doi.org/10.1145/2049662.2049663>
- Adhitha Dias, Logan Anderson, Kirshanthan Sundararajah, Artem Pelenitsyn, and Milind Kulkarni. 2024. SparseAuto: An Auto-Scheduler for Sparse Tensor Computations Using Recursive Loop Nest Restructuring. <https://doi.org/10.5281/zenodo.12764370>
- Adhitha Dias, Kirshanthan Sundararajah, Charitha Saumya, and Milind Kulkarni. 2022. SparseLNR: accelerating sparse tensor computations using loop nest restructuring. In *Proceedings of the 36th ACM International Conference on Supercomputing* (Virtual Event) (*ICS '22*). Association for Computing Machinery, New York, NY, USA, Article 15, 14 pages. <https://doi.org/10.1145/3524059.3532386>
- Johnnie Gray and Stefanos Kourtis. 2021. Hyper-optimized tensor network contraction. *Quantum* 5 (March 2021), 410. <https://doi.org/10.22331/q-2021-03-15-410>
- Will Hamilton, Rex Ying, and Jure Leskovec. 2017. Inductive representation learning on large graphs. *Advances in neural information processing systems* 30 (2017), 1024–1034.
- Albert Hartono, Qingda Lu, Thomas Henretty, Sriram Krishnamoorthy, Huaijian Zhang, Gerald Baumgartner, David E. Bernholdt, Marcel Nooijen, Russell Pitzer, J. Ramanujam, and P. Sadayappan. 2009. Performance Optimization of Tensor Contraction Expressions for Many-Body Methods in Quantum Chemistry. *The Journal of Physical Chemistry A* 113, 45 (2009), 12715–12723. <https://doi.org/10.1021/jp9051215> PMID: 19888780.
- So Hirato. 2003. Tensor Contraction Engine: Abstraction an Automated Parallel Implementation of Configuration-Interaction, Coupled-Cluster, and Many-Body Perturbation Theories. *The journal of physical chemistry. A* 107, 46 (2003), 9887–9897. <https://doi.org/10.1021/jp034596z>
- Yuwei Hu, Zihao Ye, Minjie Wang, Jiali Yu, Da Zheng, Mu Li, Zheng Zhang, Zhiru Zhang, and Yida Wang. 2020. FeatGraph: A Flexible and Efficient Backend for Graph Neural Network Systems. In *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis* (Atlanta, Georgia) (*SC '20*). IEEE Press, Article 71, 13 pages.
- Raghavendra Kanakagari and Edgar Solomonik. 2023. Minimum Cost Loop Nests for Contraction of a Sparse Tensor with a Tensor Network. <https://doi.org/10.48550/arXiv.2307.05740>

- Jinsung Kim, Aravind Sukumaran-Rajam, Vineeth Thumma, Sriram Krishnamoorthy, Ajay Panyala, Louis-Noël Pouchet, Atanas Rountev, and P. Sadayappan. 2019. A Code Generator for High-Performance Tensor Contractions on GPUs. In *2019 IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*. 85–95. <https://doi.org/10.1109/CGO.2019.8661182>
- Fredrik Kjolstad, Peter Ahrens, Shoaib Kamil, and Saman Amarasinghe. 2019. Tensor Algebra Compilation with Workspaces. In *Proceedings of the 2019 IEEE/ACM International Symposium on Code Generation and Optimization* (Washington, DC, USA) (CGO 2019). IEEE Press, Piscataway, NJ, USA, 180–192. <http://dl.acm.org/citation.cfm?id=3314872.3314894>
- Fredrik Kjolstad, Shoaib Kamil, Stephen Chou, David Lugato, and Saman Amarasinghe. 2017. The Tensor Algebra Compiler. *Proc. ACM Program. Lang.* 1, OOPSLA, Article 77 (Oct. 2017), 29 pages. <https://doi.org/10.1145/3133901>
- Jean Kossaifi, Aran Khanna, Zachary Lipton, Tommaso Furlanello, and Anima Anandkumar. 2017. Tensor Contraction Layers for Parsimonious Deep Nets. In *Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR) Workshops*.
- Vladimir Kotlyar, Keshav Pingali, and Paul Stodghill. 1997. A Relational Approach to the Compilation of Sparse Matrix Programs. In *Proceedings of the Third International Euro-Par Conference on Parallel Processing (Euro-Par '97)*. Springer-Verlag, Berlin, Heidelberg, 318–327.
- Chi-Chung Lam, P. Sadayappan, and Rephael Wenger. 1997. On Optimizing a Class of Multi-Dimensional Loops with Reductions for Parallel Execution. *Parallel Process. Lett.* 7 (1997), 157–168. <https://api.semanticscholar.org/CorpusID:9440379>
- Alan LaMielle and Michelle Mills Strout. 2010. Enabling Code Generation within the Sparse Polyhedral Framework.
- Richard Lippmann, David Fried, Isaac Graf, Joshua Haines, Kristopher Kendall, David McClung, Dan Weber, Seth Webster, Daniel Wyschogrod, Robert Cunningham, and Marc Zissman. 2000. Evaluating intrusion detection systems: the 1998 DARPA off-line intrusion detection evaluation. 2 (02 2000), 12 – 26 vol.2. <https://doi.org/10.1109/DISCEX.2000.821506>
- Jiawen Liu, Dong Li, Roberto Gioiosa, and Jiajia Li. 2021a. Athena: High-Performance Sparse Tensor Contraction Sequence on Heterogeneous Memory. In *Proceedings of the ACM International Conference on Supercomputing* (Virtual Event, USA) (ICS '21). Association for Computing Machinery, New York, NY, USA, 190–202. <https://doi.org/10.1145/3447818.3460355>
- Jiawen Liu, Jie Ren, Roberto Gioiosa, Dong Li, and Jiajia Li. 2021b. *Sparta: High-Performance, Element-Wise Sparse Tensor Contraction on Heterogeneous Memory*. Association for Computing Machinery, New York, NY, USA, 318–333. <https://doi.org/10.1145/3437801.3441581>
- Igor L. an Shi Yaoyun Markov. 2008. Simulating Quantum Computation by Contracting Tensor Networks. *SIAM J. Comput.* 38, 3 (2008), 963–981. <https://doi.org/10.1137/050644756>
- Thomas Nelson, Axel Rivera, Prasanna Balaprakash, Mary Hall, Paul D. Hovland, Elizabeth Jessup, and Boyana Norris. 2015. Generating Efficient Tensor Contractions for GPUs. In *2015 44th International Conference on Parallel Processing*. 969–978. <https://doi.org/10.1109/ICPP.2015.106>
- Md. Khaleedur Rahman, Majedul Haque Sujon, and Ariful Azad. 2021. FusedMM: A Unified SDDMM-SpMM Kernel for Graph Embedding and Graph Neural Networks. In *2021 IEEE International Parallel and Distributed Processing Symposium (IPDPS)*. 256–266. <https://doi.org/10.1109/IPDPS49936.2021.00034>
- Shi-Ju Ran, Emanuele Tirrito, Cheng Peng, Xi Chen, Gang Su, and Maciej Lewenstein. 2017. Review of tensor network contraction approaches. *arXiv preprint arXiv:1708.09213* (2017).
- Shi-Ju Ran, Emanuele Tirrito, Cheng Peng, Xi Chen, Luca Tagliacozzo, Gang Su, and Maciej Lewenstein. 2020. *Tensor Network Contractions: Methods and Applications to Quantum Many-Body Systems*. Springer Nature. <https://doi.org/10.1007/978-3-030-34489-4>
- Luca Rossi, Nesreen K. Ahmed, Jennifer Neville, and Keith Henderson. 2015. The Network Data Repository with Interactive Graph Analytics and Visualization. 42, 1 (2015). <https://doi.org/10.1145/2740908>
- S.K. Sahoo, S. Krishnamoorthy, R. Panuganti, and P. Sadayappan. 2005. Integrated Loop Optimizations for Data Locality Enhancement of Tensor Contraction Expressions. In *SC '05: Proceedings of the 2005 ACM/IEEE Conference on Supercomputing*. 13–13. <https://doi.org/10.1109/SC.2005.35>
- Ryan Senanayake, Changwan Hong, Ziheng Wang, Amalee Wilson, Stephen Chou, Shoaib Kamil, Saman Amarasinghe, and Fredrik Kjolstad. 2020. A Sparse Iteration Space Transformation Framework for Sparse Tensor Algebra. *Proc. ACM Program. Lang.* 4, OOPSLA, Article 158 (Nov. 2020), 30 pages. <https://doi.org/10.1145/3428226>
- Shaden Smith, Jee W. Choi, Jiajia Li, Richard Vuduc, Jongsoo Park, Xing Liu, and George Karypis. 2017. *FROSTT: The Formidable Repository of Open Sparse Tensors and Tools*. New York, NY, USA. <https://doi.org/10.1145/2049662.2049663>
- Michelle Mills Strout, Mary Hall, and Catherine Olschanowsky. 2018. The Sparse Polyhedral Framework: Composing Compiler-Generated Inspector-Executor Code. *Proc. IEEE* 106, 11 (2018), 1921–1934. <https://doi.org/10.1109/JPROC.2018.2857721>
- Michelle Mills Strout, Alan LaMielle, Larry Carter, Jeanne Ferrante, Barbara Kreaseck, and Catherine Olschanowsky. 2016. An Approach for Code Generation in the Sparse Polyhedral Framework. *Parallel Comput.* 53, C (apr 2016), 32–57. <https://doi.org/10.1016/j.parco.2016.02.004>

- Ruiqin Tian, Luanzheng Guo, Jiajia Li, Bin Ren, and Gokcen Kestor. 2021. A High Performance Sparse Tensor Algebra Compiler in MLIR. In *2021 IEEE/ACM 7th Workshop on the LLVM Compiler Infrastructure in HPC (LLVM-HPC)*. 27–38. <https://doi.org/10.1109/LLVMHPC54804.2021.00009>
- Ledyard R. Tucker. 1966. Some Mathematical Notes on Three-Mode Factor Analysis. *Psychometrika* 31, 3 (1966), 279–311. <https://doi.org/10.1007/BF02289464>
- Anand Venkat, Mary Hall, and Michelle Strout. 2015. Loop and Data Transformations for Sparse Matrix Code. In *Proceedings of the 36th ACM SIGPLAN Conference on Programming Language Design and Implementation* (Portland, OR, USA) (*PLDI '15*). Association for Computing Machinery, New York, NY, USA, 521–532. <https://doi.org/10.1145/2737924.2738003>
- Zihao Ye, Ruihang Lai, Junru Shao, Tianqi Chen, and Luis Ceze. 2023. SparseTIR: Composable Abstractions for Sparse Compilation in Deep Learning. In *Proceedings of the 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 3* (Vancouver, BC, Canada) (*ASPLOS 2023*). Association for Computing Machinery, New York, NY, USA, 660–678. <https://doi.org/10.1145/3582016.3582047>
- Tong Zhou, Ruiqin Tian, Rizwan A. Ashraf, Roberto Gioiosa, Gokcen Kestor, and Vivek Sarkar. 2023. ReACT: Redundancy-Aware Code Generation for Tensor Expressions. In *Proceedings of the International Conference on Parallel Architectures and Compilation Techniques* (Chicago, Illinois) (*PACT '22*). Association for Computing Machinery, New York, NY, USA, 1–13. <https://doi.org/10.1145/3559009.3569685>