Enhancing Continuous Beam Angle Resolution for Next Generation Wireless Systems: A Multi-Stage Phase-Shifting Polyphase Filters Approach

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***Abstract*— Increasing user density and capacity in next-generation systems presents a need for fine beam angle resolution especially in the emerging upper mid-band 7 – 24 GHz frequency regime. This paper presents a scalable area- and energy-efficient quadrature generator targeted for beamforming receivers with a multi-stage phase-shifting polyphase filter providing continuous beam angle resolution. When complemented with vector modulation for coarse tuning, a phase range of 360° is achieved realizing a phase-shifter-less implementation leveraging slice-based receiver architecture and polyphase filters. Fabricated in 65nm CMOS, the phase-shifting polyphase filter occupies 0.003 mm^2, consumes 0.25 mW, and achieves an Image Rejection Ratio >58 dB over the entire phase range. The quadrature generator is demonstrated with a proof-of-concept receiver array operating between 7.28-7.78 GHz consuming 37 mW per element occupying 1.26 mm^2.**

***Index Terms*— Multi-stage, polyphase filter, beam steering, continuous beam angle, local oscillator, vector modulator.**

I. Introduction

WIRELESS beamforming systems are becoming the prevailing front-end technology in modern radios and radar systems because of the need to overcome aperture loss at higher frequencies and provide spatial filtering [1]. Exponentially growing data rates presents the need for exploiting upper midband spectrum as shown in Fig. 1 for Wi-Fi and mobile applications [2]. Higher FR3 frequencies require advanced beamforming solutions with narrower beam widths, and finer beam angle resolution [3], [4]. Ideally, the beam angle resolution is continuous, such that the beam can be pointed to any location within the field of view [5]. While other continuous beam angle circuits have been proposed ([6], [7], [8]), they suffer from large size, high power, and sub-optimal complementary metal-oxide-semiconductor (CMOS) compatibility. This work presents a local oscillator (LO) signal processing design and methodology employing a multi-stage phase-shifting polyphase filter (PS-PPF) and demonstrating 360° continuous beam angle control with a multi-element 7.5 GHz array for the emerging upper mid-band FR3 spectrum focused on joint communication-sensing applications.

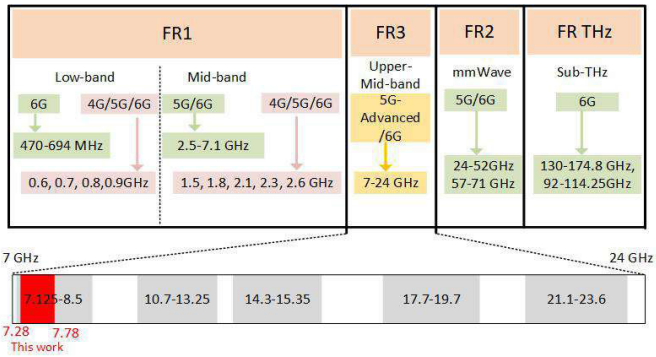

Fig. 1. Emerging FR3 spectrum.

Phase shifters play a vital role in beamforming receivers (RX) to provide an accurate beam steering angle, enhance signal reception, and therefore, improve the system performance. Amongst the several wideband beamforming architectures implementing stand-alone analog/digital phase shifters, different trade-offs exist in power, area, accuracy, and versatility [9] focused on phase-shifter resolution. In [1], a phase resolution of 5° is achieved summing separately controlled quadrature LO signals. In [3], a maximum phase resolution of 3.8° is realized, varying the current from the in-phase (I) and quadrature-phase (Q) paths. However, larger array sizes require a quadratic increase in the number of phase-shift elements limiting size, weight, and power (SWaP). Hybrid-coupler/polyphase filter (PPF) based input coupling is used in each element in [4] to realize a vector-modulator based continuous phase shifters in the RF path. However, it occupies a large area at low frequencies aside from being band limited. Varactor-based PPFs have been demonstrated in [10]

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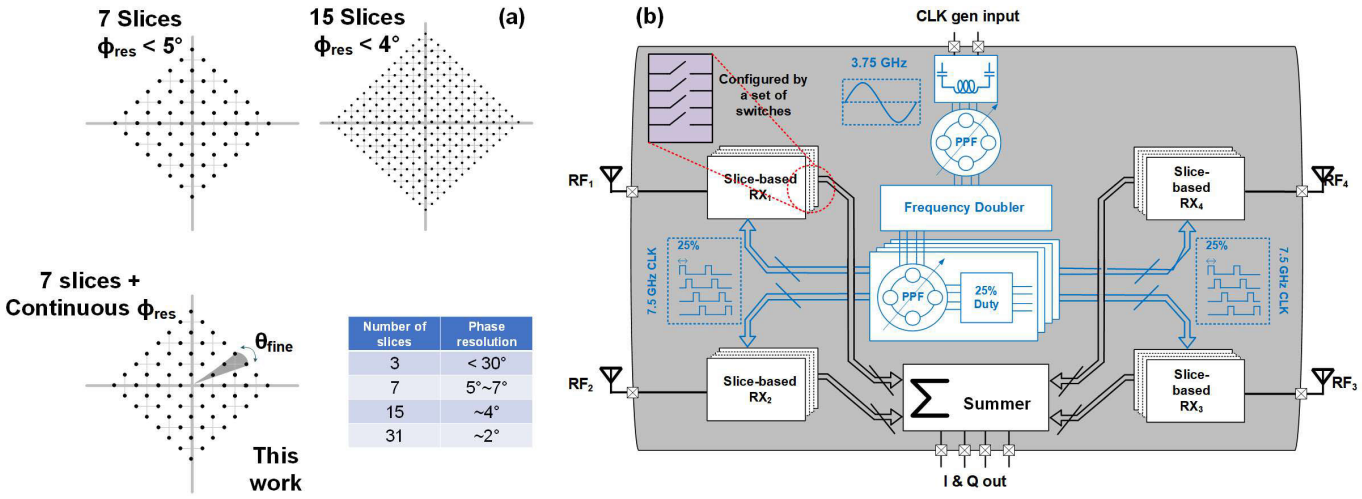

Fig. 2. (a) Phase constellation implementing 7 slices, 15 slices, and 7 slices with fine-tuning (this work), and table of achievable phase shift resolution using the slice-based architecture, (b) front-end RX architecture with slice-based vector modulation and phase-shifting LO.

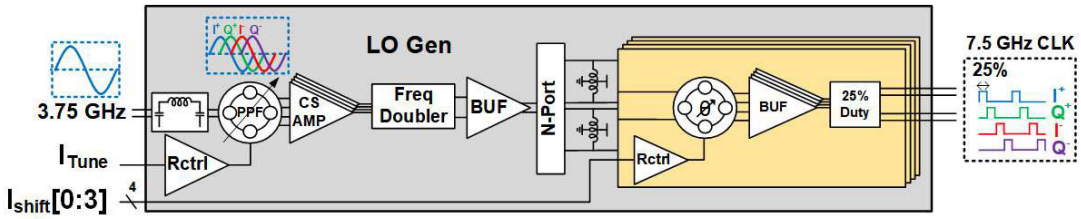

Fig. 3. Proposed 7.5 GHz LO architecture with process and temperature robust balanced frequency doubling, multiport distribution, and phase-shifting quadrature generation.

to mitigate phase error and achieve precision tuning over a 7.1 − 8.7 GHz range. However, the varactor noise and its sensitivity to process, voltage, and temperature increases the phase error and thus is not suited for fine resolution. Alternatively, slice-based vector modulators [11], [12] are emerging as a promising wide-band beamforming architecture due to their versatility, scalability, linearity, and low power with inherent vector phase control. The total phase constellation points for a slice-based architecture with an N binary scaled group are 2^{2N} [11]. Assuming the total slices quadrature output currents in one quadrant are $I = \alpha I_s$ and $Q = \beta I_s$, where $0 \leq \alpha, \beta \leq 2^N - 1$, while $\alpha + \beta = 2^N - 1$, and I_s is the unit slice output current, the achievable coarse phase shift can be expressed as $\phi_{\text{coarse}} = tan^{-1}(\beta/\alpha)$. The phase resolution using the slice-based architecture is captured in the table in Fig. 2(a). As the number of slices increases, the phase resolution gets better. For example, increasing the number of slices from 3 to 31 improves the resolution by several degrees from 30° to 2° as also shown in Fig. 2(a). Despite its advantages at lower RF frequencies [12], slice-based architectures are thus limited by significant power/area overhead due to the LO drivers in the clock distribution and the need to mitigate I/Q mismatches.

In contrast, this work demonstrates a low-range quadrature phase-shifting stage added to the coarse vector modulation in the slice-based RX array to generate a continuous beam angle resolution with a range of 360°. The fine phase shift is added to a 7-slice RX to yield a continuous phase-shifting RX as shown conceptually in Fig 2(a). This concept is presented in a 65nm complementary metal-oxide-semiconductor (CMOS) beamforming receiver using a phase-shifting quadrature generator and vector modulation as shown in Fig. 2(b). This work eliminates the need for a stand-alone high-resolution phase-shifter by adding it as a feature to the local oscillator's quadrature generator saving critical power and area. The proposed LO architecture, shown in Fig. 3, demonstrates that PS-PPF can generate quadrature signals with low quadrature mismatch and simultaneously provide continuous phase shifting with negligible area consuming < 0.25mW.

Section II compares quadrature generation topologies, provides an analysis of PPFs suited for high-frequency LO distribution, and outlines the concept of a multi-stage phase-shifting PS-PPF. Section III describes a complete LO signal processing and distribution design, including the implementation of a PS-PPF. Measurement results and conclusions are provided in Sections IV and V, respectively.

II. Analysis of Polyphase Filters

This section reviews quadrature LO generation techniques and then outlines the basic concepts of PS-PPFs and its evolution into the proposed highly area-/energy-efficient PS-PPFs enabling continuous beam-angle resolution.

A. Brief Survey of Quadrature Generators

Many RF front-ends use quadrature LO architectures to isolate the signal of interest or to implement a quadrature

modulation scheme. The primary techniques to implement quadrature generators include, but are not limited to, hybrid couplers [13], digital logic [14], oscillators [15], and polyphase filters (PPF) [16]. Transmission line-based hybrid couplers are passive in nature and provide high accuracy [13], [17] but are bulky at 7.5 GHz. In [18], an off-chip hybrid coupler is used in the signal path for generating quadrature signals. In [19], hybrid couplers with lumped elements achieve phase shift with inductive coupling and LC filters, but they suffer from increased in-phase (I) and quadrature-phase (Q) mismatches if the coupling coefficient drifts [16]. Conventional flip-flop-based frequency divider [20] and windmill divider presented in [21] require higher frequencies because they perform a frequency division by 2. Moreover, digital logic consumes high power when operating at high frequency [14]. The phase noise and the inductor quality factor requirements further limit the oscillator-based quadrature generators [22]. PPFs have been widely used for their simplicity and ability to scale with frequency [23], and their passive structure makes them one of the lowest power-consuming architectures amongst quadrature generators. The multitude of PPF configurations trade-off loss, bandwidth, size, and resilience over process, voltage, and temperature (PVT) variations with quadrature mismatch and scalability across frequency.

B. Quantifying I/Q Mismatch in Quadrature Generators

Ideal quadrature signals are equal in amplitude and have a phase difference of 90°. The mismatch between the *I*- and *Q*-phase is quantified by the RX Image-Rejection Ratio (IRR) as derived in [24]:

$$IRR = 20log_{10}\left(\frac{1 + 2A_{bal}cos(\phi_{err}) + A_{bal}^2}{1 - 2A_{bal}cos(\phi_{err}) + A_{bal}^2}\right) \quad (1)$$

$$A_{\text{bal}} = \frac{|v_{\text{I}}|}{|v_{\text{Q}}|} \quad (2)$$

$$\phi_{\text{err}} = \Delta\phi - 90^\circ \quad (3)$$

where v_{I} and v_{Q} are the amplitudes of the quadrature signals respectively. The relationship A_{bal} is the ratio between the *I* and *Q* amplitudes. When amplitude mismatch is presented alone, it will be represented in decibels as follows:

$$A_{\text{err}} = 20\log_{10}\left(\frac{1 + A_{bal0}}{1 - A_{bal0}}\right) \quad (4)$$

where A_{bal0} is the amplitude ratio centered around zero.

C. RC-Based PPF

PPFs use passive components such as resistors and capacitors to split signals into multiple phases, as shown in various forms in Fig. 4. Type-I and Type-II PPF configurations differ in the connection to the inputs *I* and $\overline{I}$. For achieving higher IRR over a wide bandwidth, multi-stage PPFs are used. Quadrature PPFs leverage the fact that first-order low-pass and high-pass filters have a phase shift at the cutoff frequency of −45° and +45°, respectively. If a low-pass and a high-pass filter are used to split a signal with a frequency equal to the cutoff frequency, the output will have a phase relationship of 90°. As system

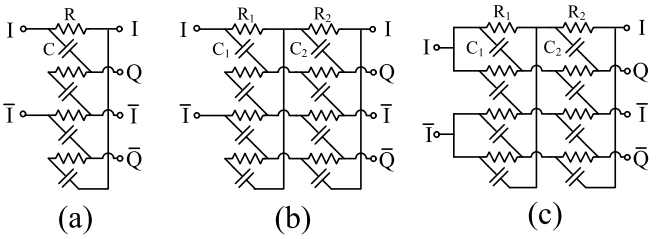

Fig. 4. (a) Type-I, (b) two-stage Type-I, and (c) two-stage Type-II RC PPF configurations. Input connections determine the type. Both types can be cascaded, as shown.

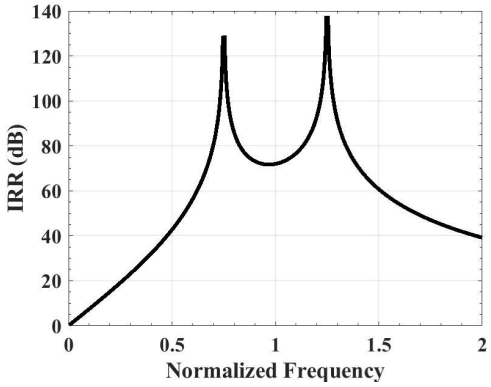

Fig. 5. Two-stage PPF wideband IRR design. The cutoff frequencies are chosen to be $0.75\,f_o$ and $1.25\,f_o$. As cutoff frequency varies with process and temperature, high IRR can still be achieved over large fractional bandwidths.

frequencies are increased, the passive R and C components get smaller, making PPFs highly scalable. Note that R and C are chosen for a desired cutoff frequency as $\omega = 1/RC$.

The quadrature amplitude and phase relationship is found as the ratio of the *I* and *Q* transfer functions as derived in [25] for Type-I as:

$$\frac{H_{\text{I}}^I}{H_{\text{Q}}^I} = \frac{1 + s^2C_1R_1C_2R_2}{s(C_1R_1 + C_2R_2)} \quad (5)$$

Note that the ratio is purely imaginary. This means that ideal Type-I PPFs inherently have 90° phase separation over a wide bandwidth. The ideal amplitude balance is achieved when the input signal frequency equals the cutoff frequency of either the first stage (ω_1) or second stage (ω_2).

The corresponding Type-II *I*/*Q* ratio is also derived in [25] as:

$$\frac{H_{\text{I}}^{II}}{H_{\text{Q}}^{II}} = \frac{1 - s(C_1R_1 + C_2R_2) - s^2C_1R_1C_2R_2}{1 + s(C_1R_1 + C_2R_2) - s^2C_1R_1C_2R_2} \quad (6)$$

From the ratio of transfer functions, we gather that the magnitude of the ratio is always one, indicating that Type-II PPFs are inherently amplitude-balanced. A wideband IRR for a two-stage Type-II PPF is shown in Fig. 5. An extremely wideband state-of-the-art rejection (> 50dB) can be achieved by spacing the cutoff frequency of each stage. An extremely wide IRR bandwidth provides robustness over process and temperature.

If we examine the gain of the wideband example system for both two-stage Type-I and two-stage Type-II we see that Type-II has less attenuation as shown in Fig. 6. The

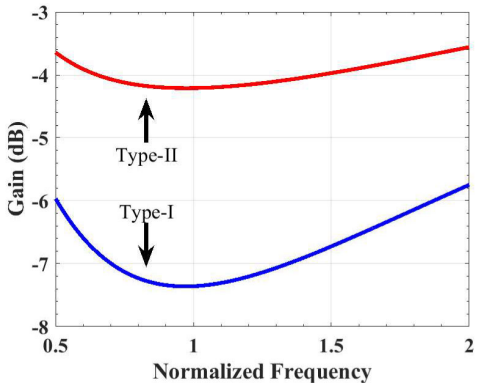

Fig. 6. Comparison of Type-I and Type-II voltage gain for two-stage PPF. Type II has less voltage attenuation than Type I.

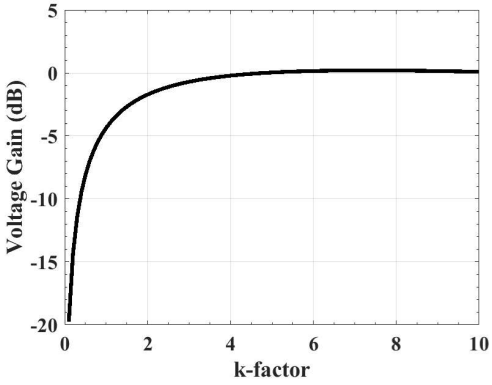

Fig. 7. Effect of k-factor on PPF Gain. As the k-factor increases, voltage attenuation decreases.

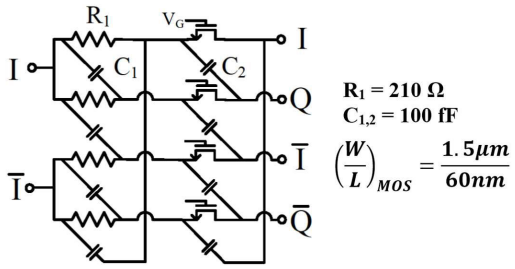

Fig. 8. The proposed phase-shifting PPF schematic. Second-stage resistors are replaced with transistors operated in the triode. By controlling the impedance of the transistor, the quadrature error or phase shift can be controlled depending on the cutoff frequency of the first stage and the input frequency.

impedance ratio from stage I to stage II should be minimized to reduce the loss further. If we define the ratio of C_1/C_2 as the 'k-factor,' we can observe the loss mitigation as shown in Fig. 7. This example minimizes the load impedance to highlight the relationship between each stage and maintains a constant cutoff frequency.

D. Proposed Phase-Shifting Polyphase Filters (PS-PPF)

If the passive components are replaced by transistors in triode, the PPF behavior can be precisely controlled as shown further. An example is shown in Fig. 8. Equation 6 can thus be rewritten in terms of the cutoff frequency of each stage.

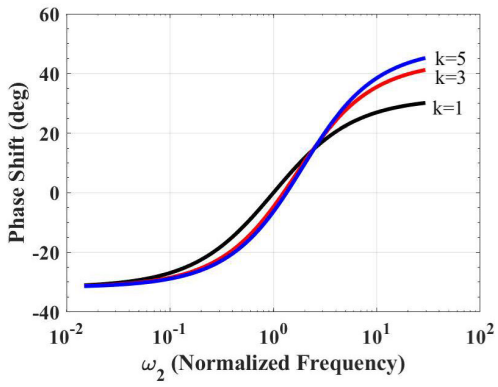

Fig. 9. Phase-shifting potential of PPFs as ω_2 varies. The value of ω_2 has been normalized to the first stage cutoff frequency, ω_1. Phase-shift range increases with the k-factor.

$$\frac{H_I^{II}}{H_Q^{II}} = \frac{1 - j\omega_{\text{in}}\left(\frac{1}{\omega_1} + \frac{1}{\omega_2}\right) - \frac{j^2\omega_{\text{in}}^2}{\omega_1\omega_2}}{1 + j\omega_{\text{in}}\left(\frac{1}{\omega_1} + \frac{1}{\omega_2}\right) - \frac{j^2\omega_{\text{in}}^2}{\omega_1\omega_2}} \tag{7}$$

If either stage has a cutoff frequency of ω_{in}, this ratio can be simplified to simply $-j$.

$$\begin{aligned}\left.\frac{H_I^{II}}{H_Q^{II}}\right|_{\omega_1=\omega_{\text{in}}} &= \frac{1-j-\frac{j\omega_{\text{in}}}{\omega_2}+\frac{\omega_{\text{in}}}{\omega_2}}{1+j+\frac{j\omega_{\text{in}}}{\omega_2}+\frac{\omega_{\text{in}}}{\omega_2}} \\ &= \frac{(1+\frac{\omega_{\text{in}}}{\omega_2})-j(1+\frac{\omega_{\text{in}}}{\omega_2})}{(1+\frac{\omega_{\text{in}}}{\omega_2})+j(1+\frac{\omega_{\text{in}}}{\omega_2})} \\ &= -j\end{aligned} \tag{8}$$

This ratio is purely imaginary and has a magnitude of one regardless of the second stage cutoff. This means that as long as ω_1 remains close to ω_{in}, this filter will have very good IRR, and it will be independent of ω_2. As we vary ω_2 and observe the phase response of H_{I}^{II} or H_{Q}^{II}, we see a significant phase shift opportunity, as shown in Fig. 9. The phase shift range can be increased further by increasing the k-factor. Section III presents the implementation details of this PS-PPF for a quadrature generator in a multi-element array.

III. Phase-Shifting LO Implementation

This section details an LO using frequency doubling and phase-shifting quadrature generation as shown in Fig. 3. This includes the design and implementation of the proposed PS-PPF. This LO is designed for a 2 × 2 beamformer with 2 elements having been characterized and demonstrated in Section IV. The beamformer has been adapted from [12] employing a 7-slice vector modulating RX array with passive mixers.

A. Output Duty Cycle

For quadrature systems using passive mixers, the LO output ideally has a 25% duty cycle to increase gain, lower noise figure, lower intermodulation distortion, and flicker noise [26]. The 25% duty cycle is achieved with transmission gates as shown in Fig. 10. Each I/Q-phase is similarly connected with

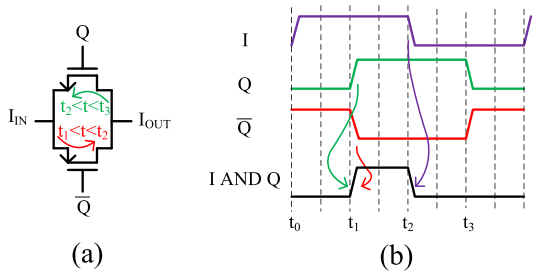

Fig. 10. Transmission gate (a) schematic including the flow of charge and (b) the corresponding AND operation which yields a duty cycle conversion from 50% to 25%.

the same phase relationships from the input to the control signals.

The layout of the four transmission gates requires matching parasitics to mitigate *I/Q* mismatch as shown in Fig. 15.

B. Output Drive Strength

A driverless LO is not feasible because a large output voltage swing is desired, yet the preceding stage uses series transistors in triode for which the voltage peak should not approach $V_{DD} - V_{th}$. The LO driver in this design converts a low-swing sinewave to a rail-to-rail square wave. This is achieved with a self-biased complementary common-source (CS) amplifier followed by two CMOS inverters.

The driver trade space balances receiver NF, linearity, power consumption, design complexity, and area. The target magnitude of the LO output is determined by simulation. By sweeping an ideal LO output voltage and measuring the NF and third-order intermodulation distortion (IIP3), we can isolate the effect of LO magnitude on receiver performance as shown in Fig. 11. To determine the tradeoff between NF/IIP3 and the LO output swing, the results are referenced to NF/IIP3 for an LO magnitude of 1V (the maximum core voltage for this technology). To limit the NF degradation to < 0.5dB an 800 mV output magnitude is chosen as the target. This trade-off relaxes the design constraints of the driver and reduces power consumption at the cost of a slight degradation to NF and linearity.

The implemented mixer is a current mode passive mixer. The LO swing is directly correlated to the mixer switch linearity, and thus the receiver linearity as shown in [27] and [28]. In [29], switched capacitor clock boosting is used to improve the clock swing, resulting in improved In-Band IIP3. The charge-pump based clock booster proposed in [30] provides $\approx 3\times$VDD clock swing and acheives superiour IB-IIP3 performance. In our simulations, we observe the similar trend: the IIP3 improves when LO swing increases, as shown in Fig. 11.

The driver is required to charge a 30 fF cap to 800 mV in 10 ps. The quadrature generator outputs a sinewave to the driver with a maximum slope of 3.5 mV/ps. The desired output edge rate is 80 mV/ps, thus the required gain is 27 dB. This is achieved with the three-stage driver shown in Fig. 12.

To reduce the area and complexity of the first stage, we use a self-biased configuration. Each three-stage driver consumes 2.32 mW, for a total of 9.28 mW per receiver element. The

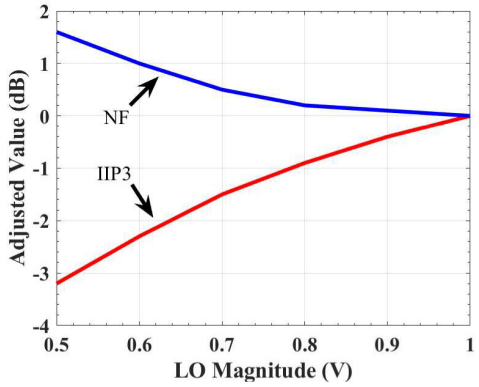

Fig. 11. Simulated effect of LO voltage swing on the proposed RX NF and linearity normalized to a technology-dependent maximum of $1V_{pp}$. This illustrates a trade-off between LO power consumption and RX performance.

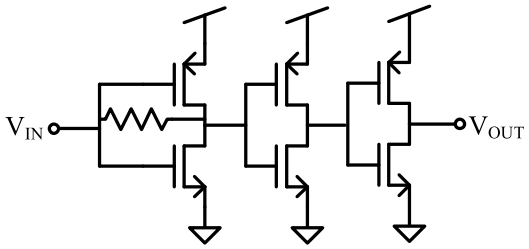

Fig. 12. The three-stage output driver is composed of a self-biased complimentary CS stage followed by two inverters.

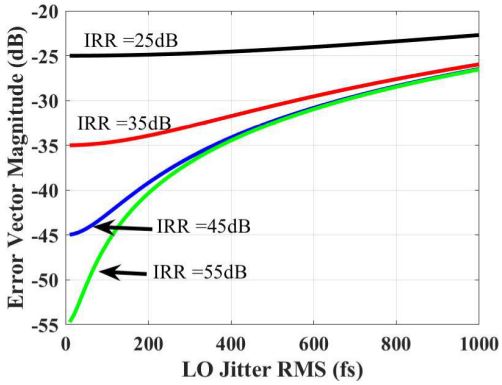

Fig. 13. EVM vs. LO jitter and IRR at 7.5GHz.

size of the three-stage driver is 0.011×0.015 mm^2 including power planes.

Additional IRR degradation will occur due to amplitude mismatch or phase mismatch between quadrature channels through the drivers and transmission gates. To minimize these mismatches, routing lengths are matched to within 0.5°, power routing is designed to limit IR loss mismatch to $<1\%$ V_{pp} (8mV), and additional metal is added to match parasitic capacitance as shown in Fig. 15. Using Equation 1, these constraints limit the maximum IRR of the system to $>$ 90dB. Post layout simulations estimate the IRR of the driver, transmission gates, and routing shown in Fig. 16 to be $>$ 86dB, dropping to 64dB when the PS-PPF is included.

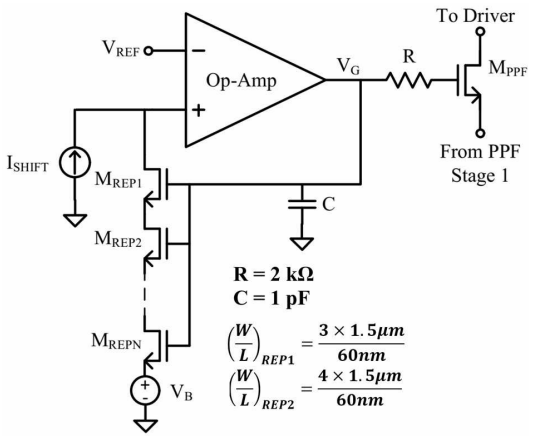

Fig. 14. PPF control circuit schematic. The voltage and current references are converted into PPF transistor resistance. Replica transistors are used in the feedback loop to achieve process and temperature variation tracking.

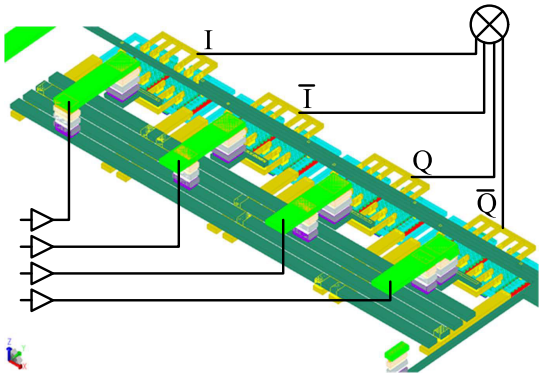

Fig. 15. 25% duty cycle is achieved with four transmission gates. Routing includes additional metal to improve parasitic capacitance matching between quadrature channels. This decreases amplitude and phase mismatch.

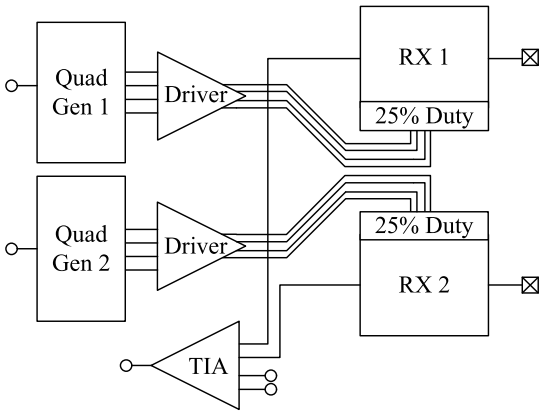

Fig. 16. The layout floor plan illustrates routing length mismatch challenges.

C. Multi-Stage Phase-Shifting PPF Implementation

Based on the analysis in Sec. II-D, quadrature generation is implemented using a two-stage Type-II PPF as shown in Fig. 8. At least two stages are required for a phase-shifting PPF, and Type-II is chosen to mitigate passive losses. For systems using quadrature encoding schemes, such as Quadrature Amplitude Modulation (QAM), the IRR of the LO signals affects the Error Vector Magnitude (EVM). The effect of LO IRR and jitter (J_{RMS}) on EVM is taken from [31] as follows and

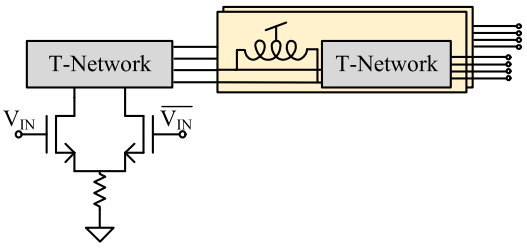

Fig. 17. Distribution circuit composed of an open-drain differential amplifier followed by a 1:4 T-network with inductive termination.

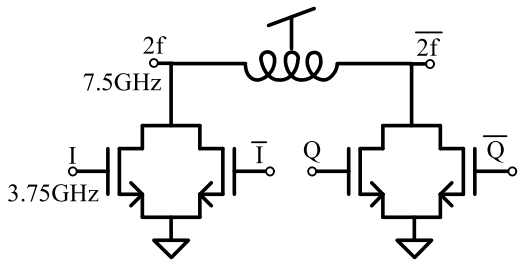

Fig. 18. Balanced push-push frequency doubling circuit. A balanced output requires quadrature input. A center-tapped inductor is used to improve differential coupling and increase gain with inductive peaking.

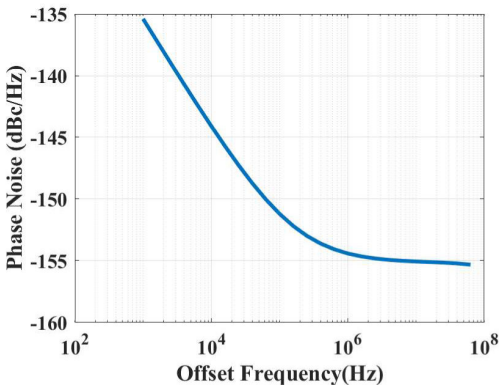

Fig. 19. Simulated frequency doubler phase noise.

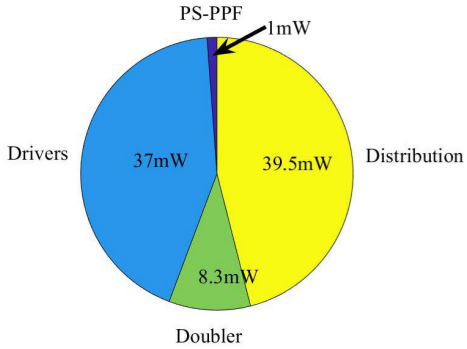

Fig. 20. Power consumption breakdown for LO circuit. The PS-PPF consumption includes all four instances.

determines the acceptable IRR of a quadrature generator given the system's EVM requirement and reference jitter.

$$\mathrm{EVM}_{\mathrm{LO\%}} = \sqrt{(J_{\mathrm{RMS}} \cdot 2\pi f)^2 \cdot 10^{-\frac{\mathrm{IRR}}{10}}} \tag{9}$$

According to IEEE 802.11, the EVM required for high code rate QAM-256 is -32dB [32]. Figure 13 illustrates the relation between EVM, jitter, and IRR at 7.5GHz. For a rough estimate, we assume a jitter of 400fs, and the IRR target becomes > 45dB.

Stage one has a cutoff frequency of 7.5GHz. This maintains the I/Q balance and allows the second stage to control the phase shift through the filter. All capacitors are 100fF MIM caps, and all resistors in stage one are 210Ω polysilicon resistors. The transistors are operated in the triode region, and the R_{DS} is controlled through V_G. The nominal control point for the MOS resistors is 450Ω. It is designed for a phase-shift range equal to the phase-shift resolution of the vector modulator, 8°. The vector modulator is composed of seven identical slices granting four binary weights, each with four phase options. This yields an average angle resolution of 8°. The remaining phase positions are granted by the phase-shifting PPF. Controlling the PPF is achieved with a technique inspired by [23] and shown in Fig. 14.

A reference voltage and a control current are fed from off-chip. A large resistance is placed between the op-amp and the PPF to limit the LO leakage through this path and to help couple the AC source voltage onto the gate. The replica transistor (M_{REP}) in feedback has the same dimensions as the PPF transistor so that it can track the operating parameters over PVT. The R_{DS} of the PPF transistor is controlled by both V_{REF} and I_{SHIFT}. For this design, V_{REF} is held constant. As the current through the replica transistor changes, the op-amp forces the voltage across the replica to track V_{REF}. In this way the op-amp converts the external signals V_{REF} and I_{SHIFT} into an R_{DS} in both transistors. Therefore, it is important to keep the replica transistor in triode as well. This can be done by keeping V_{REF} very low, but this causes challenges in op-amp operation and stability. Another option is to add multiple replica transistors in series, which divides the V_{DS} equally between each series transistor. Lastly, we can add a voltage source (V_B) to the source of the last replica transistor to ensure triode operation. The closed-loop formula for R_{DS} is as follows.

$$R_{DS} = \frac{V_{REF} - V_B}{N \cdot I_{SHIFT}} \tag{10}$$

As the control current is varied from 200μA to 500μA, the phase shift and IRR changes as shown with measurements in Section IV. The phase shift range is ±4° as designed to bridge the gap of a seven-slice quadrature vector modulator. The modest phase shift presented here is just a fraction of what is possible. The practical limit to phase shift range is dependent on the control circuit design. High open-loop gain keeps the replica transistor in triode extending the variable resistance range, but presents a stability trade-off. By increasing the k-factor and increasing the variable resistance range, PS-PPFs have the potential to shift over 45°.

The IRR and phase shift range will shift slightly over process and temperature. With RC component process variation the cutoff frequency of each stage will vary. This results in the IRR peaks from Fig. 5 shifting left or right, degrading IRR. Given 1-sigma process variation at 25° C, the IRR of this

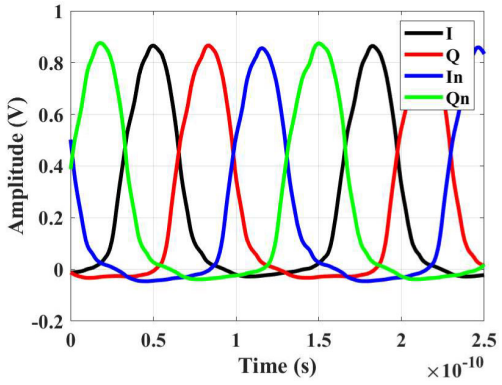

Fig. 21. Simualted quadrature LO output waveforms.

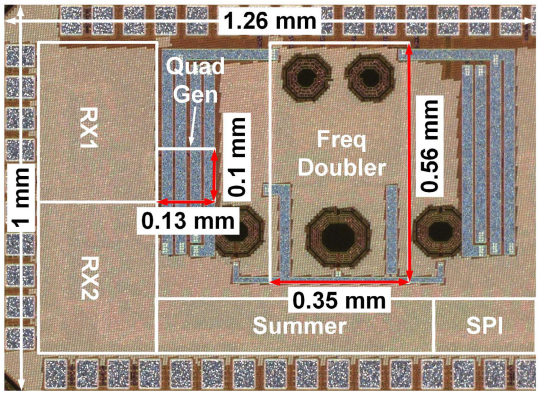

Fig. 22. Chip micrograph with 0.35 × 0.56mm^2 frequency doubler, as well as the 0.13 × 0.1mm^2 quadrature generator for each RX.

circuit is simulated to remain > 64dB as shown in Fig 26. For additional process and temperature robustness, the first stage can be controlled with switchable banks of passive devices or variable MOS devices to ensure the IRR peak remains acceptable for the desired application.

The power consumed by the PPF and control circuit includes that of the op-amp and the replica transistors. The op-amp is biased with 16μA and operates on 1V. The control current has a range of 200μA to 500μA, and the voltage drop across multiple series replica FETs (M_{REF1},..., M_{REFN}) is 450mV. This quadrature generator consumes at most 0.24mW for a total of < 1mW for all four receivers in the chip. Power consumption can further be reduced by lowering the control current. The layout of an PS-PPF adds parasitics that affect the cutoff frequency of each stage. The optimal layout minimizes the number of routing cross-overs and makes routing parasitics symmetrical as shown in [33].

D. LO Distribution

Distributing the frequency multiplied signal to each of the four on-chip receivers is achieved with a current-mode n-port with one differential input and four differential outputs. The n-port is terminated with inductors for inductive peaking, reducing the gain requirements of the frequency doubler. The amplifier is an open-drain degenerated common-source stage followed by a one-to-four differential T-network. Achieving a low phase and amplitude mismatch between elements requires

a highly symmetrical distribution network. The amplitude mismatch peak between distribution outputs is < -80 dB for this design. The phase mismatch peak between outputs is $< 0.02°$. The amplifier feeds a current-mode signal into the differential T-network. Inductive loads are placed at the end of the network for inductive peaking. Center-tapped inductors are used as differential loads with the center tap tied to V_{DD}. The circuit is shown in Fig. 17.

E. Frequency Doubling

Instead of a phase-locked loop (PLL), a doubler is used to save power. A state-of-the-art PLL for a similar frequency range consumes over 30 mW [34]. The doubler in this design consumes 8.3 mW while maintaining low additive phase noise using a push-push topology with inductive peaking. The push-push doubler is composed of quadrature CS stages with the in-phase drains tied together and the quadrature-phase drains tied together, as demonstrated in [19]. The load is a center-tapped inductor with the center tap tied to V_{DD}. By using quadrature inputs, a balanced output is achieved. An inductive load is used for peaking and improving differential coupling. The circuit is shown in Fig. 18.

To achieve balanced frequency doubling, a quadrature generator is placed before the frequency doubler. This quadrature generator is a two-stage Type-II PPF. Two stages are used for tunability over process and temperature, and Type-II is preferred for lower losses. This quadrature generator also demonstrates a PPF with near-zero voltage attenuation by maximizing the k-factor as defined above. Losses are limited to just 0.2 dB. A copy of the control circuit for the phase shifter is used here as well.

The frequency doubler uses large-signal operation. The input signals are biased at V_{TH}, so the transistors only conduct for half of the period for each phase. Tying the drains together for two signals that are separated by 180° results in a symmetrical current draw that alternates from side to side.

To maintain high symmetry while minimizing routing length and cross-over parasitics, the distribution amplifier is placed between the push-push transistors and the load inductor. A post-layout model is generated using parasitic extraction and EMX for an EM model with parasitics. Post-layout simulation yields a cycle-to-cycle jitter of 102 fs RMS when integrated from an offset of 10 Hz to 3.75 GHz for 100 cycles. The phase noise is -144 dBc/Hz at an offset of 10 kHz, as shown in Fig.19. The power consumption is 8.3mW.

F. Top-Level Summary

The power consumption breakdown for the LO circuit is shown in Fig. 20. The PS-PPF consumes only 1.2% of the overall LO budget. The simulated quadrature output waveforms are shown in Fig. 21. The 7.5 GHz quadrature generator is equipped with a phase-shifting feature, and it maintains state-of-the-art IRR performance. A performance comparison with other PPFs is presented in Table I.

IV. Measured Results

The RX was designed and fabricated using the standard 65-nm CMOS process, and the QFN-packaged part was tested over the frequency range of 7.28-7.78 GHz. The input RF signals are generated using a Keysight Arbitrary Waveform Generator (AWG), i.e., M8195A. Fig. 22 shows the die micrograph occupying 1.26 mm^2 where the LO portion for each RX occupies 0.013 mm^2 and consumes $\sim$ 25 mW/element. An S11 of <-10 dB is measured as shown in Fig. 23(a). Setting the configuration switches in each RX for the maximum gain achieves a gain of 22 dB across the -3 dB input BW, as illustrated in Fig. 23(b). This performance is further amplified by an additional $+6$ dB when a second in-phase input is engaged because, in this case, the current going to the TIA is doubled. The single-channel minimum NF_{DSB} of 8.93 dB is depicted in Fig. 23(b). Note that the NF slightly degrades when the RX configuration switches are set for an angle of arrival different from zero for an input signal since the RX gain drops. However, the chip's overall SNR improves by enabling the second element by a factor of two, i.e., $+3$ dB. The power consumption of a single RX block is 14 mW. Fig. 24(a) and (b) highlight a 1-dB compression point (P1dB) of -9 dBm and an in-band OIP3 of 20.6 dBm, respectively. Fig. 25 shows the variation in gain for two sets of coarse phase shift configuration. Setting I is set to 0° while setting II is where the coarse phase tuning is set to 36°. In this case, an amplitude RMS error of 0.4 dB is achieved at the midband frequency of 7.5 GHz. Fig. 26 indicates the fine phase shift achieved through PPF control current tuning ($\pm 4°$), with the phase shifter exhibiting an RMS phase error of 0.74°. 1-sigma process deviation is gathered from Monte-Carlo

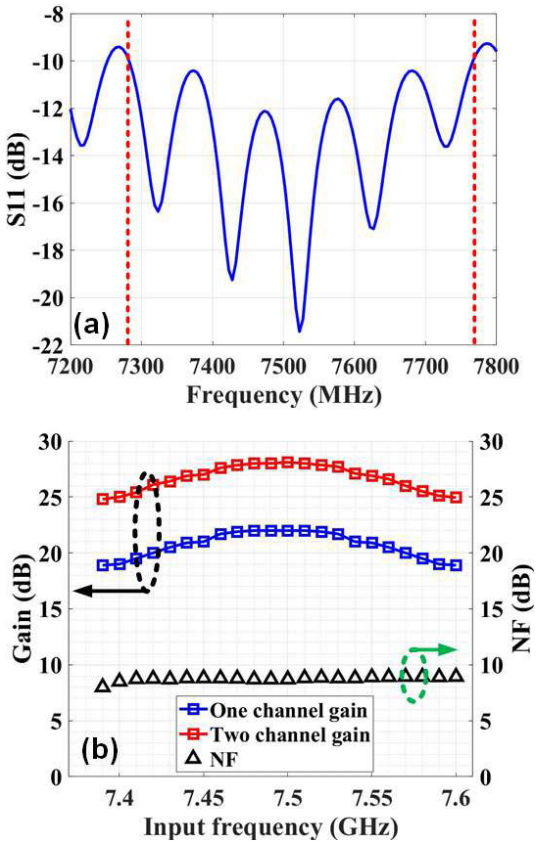

Fig. 23. Measured (a) 1-channel S11, (b) 1- and 2-channel gain, and 1-channel NF.

TABLE I
QUADRATURE GENERATOR PERFORMANCE COMPARISON

Work	Technology	Architecture	Phase Shifting	Frequency (GHz)	Phase Noise	Power (mW)	IRR (dB)	Area (mm^2)
RFIC 2016 [35]	45nm SOI CMOS	PPF	No	20-30	NR	NR	> 41	< 0.75
CSICS 2017 [14]	55nm SiGe BiCMOS	Divider	No	62	NR	172	NR	0.03
TMTT 2017 [23]	28nm CMOS	PPF	No	55 – 70	<-165dBc/Hz @ 10kHz PPF Only	< 0.192	> 65	0.0008
RFIC 2018 [19]	65nm CMOS	Hybrid Coupler	No	12	NR	NR	> 50	0.048
ISSCC 2018 [16]	55nm CMOS	PPF	No	28 – 44	NR	3	> 40	0.19
IMC-5G 2019 [36]	45nm SOI CMOS	Divider	No	5 – 31	NR	86-220	> 54	0.15
TCSII 2019 [33]	40nm CMOS	PPF	No	60	NR	NR	> 35	0.0033
This Work	65nm CMOS	PPF	Yes	7.5	<-130dBc/Hz @ 10kHz LO Output	0.25	> 58	0.0032

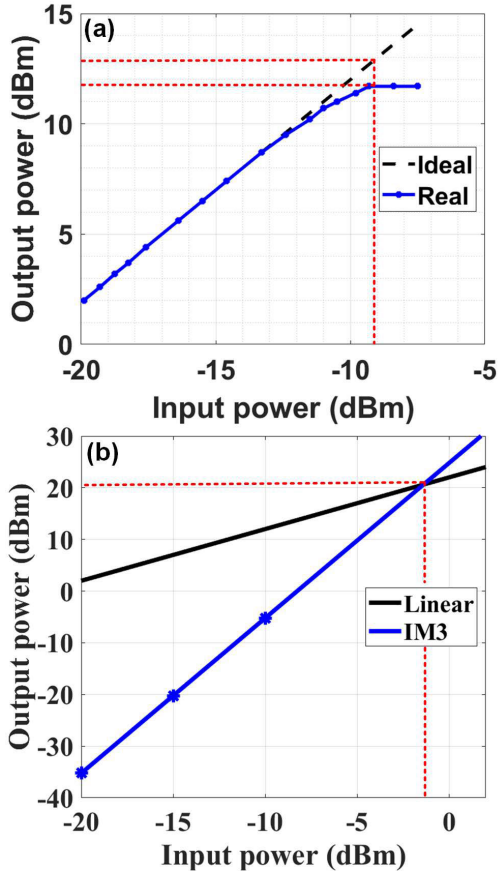

Fig. 24. Measured 1-channel (a) P1dB and (b) OIP3.

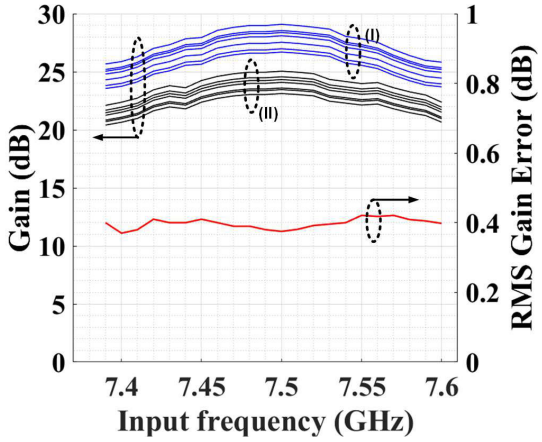

Fig. 25. (Pri. axis) 2-element gain with coarse phase-tuning step set to (I) 0° and (II) 36° respectively varied over the fine phase-tuning range. (Sec. Axis) RMS gain error.

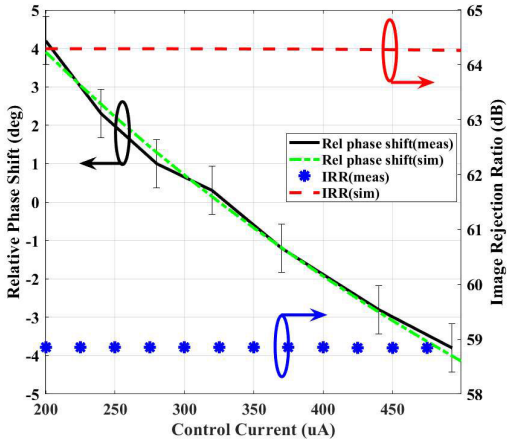

Fig. 26. Measured and simulated phase shift and IRR from proposed PPF as control current is varied. The desired phase shift range is achieved without compromising the quadrature balanced, as measured by IRR.

simulation, and the deviation is denoted in Fig. 26. Depicted in Fig. 26, an IRR of $>$ 58dB is achieved within the PPF current tuning span at 7.5 GHz. The IRR results for simulation and measurement differ because the simulation is probing the signals before the mixer, whereas the measurement was made post-mixer. Fig. 27(a) demonstrates the phase constellation points in one quadrant, showing that the fine phase shift works when the coarse stage is set for zero and 36°. Therefore, by implementing both fine and coarse phase-tuning stages, we can cover 360°. Measured IRR over 200MHz RF BW, centered at 7.5GHz, is shown in Fig. 27(b). A uniform IRR is achieved by setting the PPF control currents as 200uA. A summary of quadrature generator performance and comparison is provided in Table I.

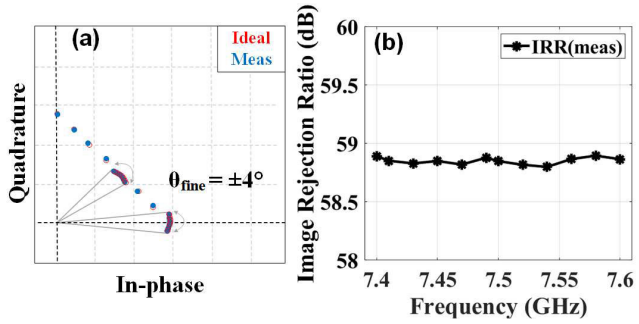

Fig. 27. (a) Measured phase constellation showing the (±4°) phase shift feasibility over 360°, and (b) Measured IRR over 200MHz RF BW.

V. Conclusion and Future Works

Quadrature generators are an essential building block for modern radios. This work shows that polyphase filters are a versatile quadrature generator topology. The multitude of PPF configurations allows for low loss, high bandwidth, PVT resilience, small size, low I/Q mismatch, and scalability. A phase-shifting quadrature generator for beamforming transceivers is presented. This circuit maintains state-of-the-art performance against other quadrature generators with an image rejection ratio $>$ 58dB, a power consumption of $<$ 0.24mW, and an area of 0.0032mm^2. Due to this versatile topology, the proposed quadrature generator can easily be modified for a wide range of applications, including those that require PVT robustness, high bandwidth, and millimeter-wave (mmW) frequencies. This quadrature generator is demonstrated in a local oscillator designed for a four-element beamforming receiver. The primary quadrature generator is a PS-PPF used for continuous beam-angle control. An additional quadrature generator is included as a tunable PPF for a process and temperature robust frequency doubler. Future works will aim to demonstrate wideband operation of this phase-shifting quadrature generator across a larger array.

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