Superconductor Logic Implementation With All-JJ Inductor-Free Cell Library

Haolin Cong, Sasan Razmkhah, Mustafa Altay Karamuftuoglu, and Massoud Pedram, *Fellow, IEEE*

***Abstract*—Single flux quantum (SFQ) technology has garnered significant attention due to its low switching power and high operational speed. Researchers have been actively pursuing more advanced devices and technologies to further reduce the reliance on inductors, bias, and dynamic power. Recently, innovative magnetic Josephson junction devices have emerged, enhancing the field of superconductor electronics logic. This article introduces a novel cell library design that relies entirely on Josephson junctions, showing promising potential for eliminating the need for inductors in conventional SFQ cells. This results in a 55% reduction in cell size and an 80% decrease in both static and dynamic power consumption. The proposed library implements a half flux quantum logic, where each pulse duration is half that of a SFQ pulse. This article presents the schematics of the basic cells, emphasizing critical circuit parameters and their margins. In addition, it examines layout blueprints, showcasing the advantageous area-saving characteristics of the proposed design.**

***Index Terms*—All-Josephson junction (JJ), half flux quantum (HFQ), single flux quantum (SFQ), superconductor electronics.**

I. Introduction

SINGLE flux quantum (SFQ) technology [1] holds great potential for advancing the next generation of very large-scale integration (VLSI) circuits. Among SFQ logic circuits, the rapid SFQ (RSFQ) logic family stands out, offering extremely high operational speeds. RSFQ utilizes Josephson junctions (JJs), which are known for their ultra-fast picosecond (ps) switching times. RSFQ logic cells exhibit swift responses with a clock-to-output delay of 10 ps, enabling RSFQ systems to excel in the 40–60 GHz range [2], [3], [4]. JJs require significantly less energy to switch than CMOS technology, potentially as low as $10^{-19}\mathrm{J/bit}$. This efficiency sets RSFQ systems apart as more power-efficient alternatives. The RSFQ domain has garnered substantial attention, with studies covering circuit and system designs [5], [6], [7], innovative layout designs [8], [9], and notable progress in electronic design automation tools and algorithms [10], [11].

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Despite the numerous advantages offered by RSFQ circuits, they are confronted with significant challenges. RSFQ circuit integration density remains relatively low, accommodating only around 10 000 logic gates within a 1 cm^2 chip area. This limitation is the key limiting factor in meeting the logic circuit requirements of various applications. In addition, RSFQ circuits lack dense on-chip memory and require substantial bias currents for their operation. Given these obstacles, it becomes imperative to explore alternative logic circuit families capable of overcoming these challenges and driving the advancement of SFQ technology.

At the core of superconductor circuits lies the JJ. Serving as the active component in an SFQ circuit, the JJ adopts the standardized superconductor–insulator–superconductor (SIS) configuration. The dynamic behavior of a JJ is encapsulated by the current-phase relation (CPR), which relies on parameters, such as the current density (J_s), the critical current density (J_C) at which the JJ exits the superconducting state, and the phase difference (ϕ) spanning two superconducting layers. This simplified CPR equation assumes a consistent supercurrent tunneling through the JJ's barrier while maintaining temperatures well below the critical threshold. Importantly, this equation accurately approximates the behavior of the SIS JJs and serves as the cornerstone for most SPICE-based simulation engines.

The MITLL SFQ5ee process [12], [13] is an exemplary technology that employs an $\mathrm{Nb/Al-AlO}_x\mathrm{/Nb}$-type junctions, with the superconducting layers composed of Nb and the insulator being AlO_x. By replacing the insulator layer with a magnetic material featuring a built-in magnetic field, the SIS JJ transforms into a magnetic junction (MJJ) [14], [15]. The MJJ has been extensively studied for its unique properties, giving rise to innovative devices, such as the π-junction (π-JJ), φ-junction (φ-JJ), and 2φ-junction (2φ-JJ), which have piqued the interest of researchers.

Researchers are actively pursuing the development of faster, more efficient, and compact technology. However, reducing the size of inductors in SFQ circuits poses an important challenge due to increasing mutual inductance and crosstalk in SFQ circuit layouts, limiting further reductions in the width and spacing of metal lines. While the kinetic inductor offers a potential solution, it has its challenges. Addressing this issue, the work outlined in [16] attempts to eliminate the need for inductors and enhance SFQ circuit scalability by utilizing logic cells [such as AND and OR gates, NOT and XOR gates, non-destructive readout (DRO) Data flip-flops (DFFs)] with 2φ-junctions. Maksimovskaya et al. [17] replaced the 2φ-JJ with a stack of 0 and

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π-JJ, which is easier to fabricate. In addition, a similar study covers logic implementations with bistable JJs [18].

In all these studies, the 2φ-JJ is used to create a phase difference in the loop, and this phase difference will cause a phase shift, hence creating a circulating current in the loop. For three JJs, three basic loops with different JJ combinations are created. Each has a different phase relation and can be used as readout, driver, and storing loops. In this work, the 2φ-JJs are acting as the switching elements. Therefore, we can incorporate circuits similar to the RSFQ structures but with much smaller bias values. Due to the bistability of the 2φ-JJs, we create HFQ pulses in each π phase, and therefore, the circuits are twice the speed of RSFQ by nature. This will result in $\tilde{1}00$ GHz clock frequencies in the fabrication technologies similar to the current MIT LL SFQ5ee process.

Simultaneously, efforts are underway to leverage the 2φ-junction to minimize dynamic power consumption in SFQ systems, as explored in [19]. This study introduced three novel cells incorporating the 2φ-junction: a Josephson transmission line (JTL), an inverter, and an OR gate. Compared to conventional RSFQ cells, these cells utilize half flux quantum (HFQ) pulses, resulting in reduced latency and switching power. However, it is important to note that this study lacks detailed circuit parameters, and the three cells do not constitute a complete standard cell library to meet fundamental functional requirements.

Moreover, there are various papers exploring the possible implementations of HFQ circuits [20], [21], [22], [23]. In these works, the Fujimaki laboratory team from Nagoya University explores the design of the HFQ circuits using the π-JJs. The π-JJ layer is deposited on the already established Nb process with Nb/Al-AlO$_x$/Nb JJs.

This article introduces a comprehensive standard cell library based on 2φ-JJ technology, encompassing four essential logic cells (inverter, AND gate, OR gate, and XOR gate), five transmission blocks (JTL, splitter (SPL), merger, passive transmission line (PTL) transmitter and receiver), one storage cell (DFF), and two I/O interface blocks (dc/SFQ and SFQ/dc converters.) This library caters to the fundamental requirements of a general-use system.

We validate the functionality of each cell using the JoSIM simulator [24]. Furthermore, we optimize the circuits using qCS [25], achieving commendable margins. qCS performs a binary search in order to determine lower and upper bound margins. The optimization is achieved by a hybrid swarm optimization method (automatic niching particle swarm optimization) with a novel centering-favored objective function [26], [27]. Critical circuit parameters and their total margins (the summation of lower and upper bounds) are meticulously presented, along with projected layout areas for the cells using the MITLL SFQ5ee process. The rest of this article is organized as follows. Notably, a simulated 2φ-junction device is included in Section II. In Section III, we delve into the design intricacies of each cell within the library, concluding with a summary. In addition, Section IV outlines the methodology employed for estimating layouts and offers a comparative analysis with a conventional RSFQ cell library. Finally, Section V concludes this article.

II. 2φ-Junction

Recent research has revealed intriguing phenomena at the $0-\pi$ transition, where the fundamental sinusoidal term of the CPR vanishes, rendering high-order harmonic terms significant [28]. In a study by Stoutimore et al. [29], a single superconductor–ferromagnet–superconductor junction employing a $Cu_{47}Ni_{53}$ alloy barrier is realized with two parallel superconducting inductors: a readout inductor and a small shunt inductor. The readout inductor couples with a commercial dc superconducting quantum interference device sensor, detecting flux Φ within the readout loop.

Through measurements of the CPR across various barrier thicknesses and temperatures, Stoutimore et al. [29] established a π-periodic behavior, putting to rest alternative explanations except for a second-order CPR. Consequently, the CPR is redefined as follows:

$$J_s(\phi) = J_{c1}\sin(\phi) + J_{c2}\sin(2\phi). \tag{1}$$

This gives rise to a new device known as the 2φ-JJ, characterized by the CPR

$$J_s(\phi) = J_{c2}\sin(2\phi). \tag{2}$$

The 2φ-JJ possesses intriguing properties: it features a CPR with a period of π rather than 2π, undergoes switching with a π phase jump, and produces a HFQ ($\frac{1}{2}\Phi_0 \approx 1.03 \times 10^{-15}$ Wb) accompanied by a π phase shift for each switching event [19]. These characteristics have fueled additional research into the utilization of 2φ junctions.

III. Logic Cell Implementation With 2φ-JJs

In the 2φ-JJ based design, most cells adhere to the conventional RSFQ cell structures, except inductors, which are replaced by normal JJs (0-JJs.) The 2φ-JJ serves as the switching component. Consequently, a logic "1" for this logic family is represented by an HFQ pulse, with the voltage $\cdot$ time product being half that of a full flux quantum ($\frac{1}{2}\Phi_0 = 1.03 \times 10^{-15}$ Wb.) This modification eliminates the need for inductors in the cell design, thereby avoiding the disadvantages and inconveniences associated with large inductances in RSFQ logic circuits.

Although the designed inductors are eliminated, parasitic inductors unavoidably exist in every connection. Therefore, an intrinsic 0.5 pH inductance is assumed for each connection during the design process. According to simulations, the tolerance to parasitic inductance exceeds 100% (0 to >1 pH.) Note that all parasitic inductances are omitted in the following schematics to improve the clarity of the figures.

To confirm the behavior of the JJ models, we simulate the I–V characteristic of the 0, π, and 2φ JJs [30] and compare them in Fig. 1. The difference between 0-JJ and 2φ-JJ is in the switching behavior. Each junction switches when the voltage–time integration exceeds the flux quantum requirement. The 2φ-JJ switches twice when the 0-JJ switches once while receiving an equivalent amount of flux quantum. The area under the voltage–time graph of a 0-JJ pulse is always ϕ_0 whereas 2φ-JJs create a pulse with half that value.

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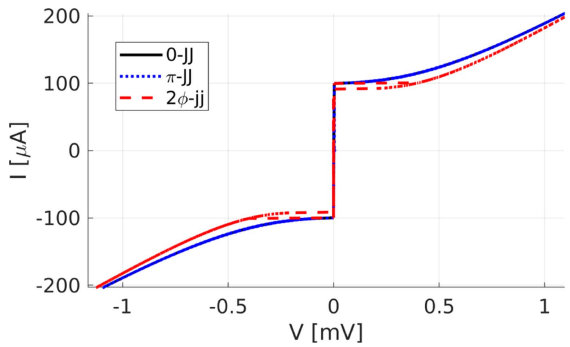

Fig. 1. Simulation I–V of 0, π, and 2φ JJs.

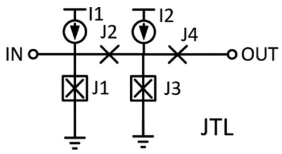

Fig. 2. Schematic of the JTL.

In the following sections, we will explore the specifics of each cell, presenting schematic diagrams accompanied by a table listing parameter values and associated cell margins. In addition, we will provide simulation waveforms to demonstrate the correct functionality of each cell. Preliminary layouts have been generated for these cells to assess potential area savings. However, it is essential to note that, at present, no existing technology offers the 2φ-JJ in a fabrication stack-up. Consequently, these layouts cannot be fabricated in any facility known to the authors. For our layout design, we employed the MITLL SFQ5ee process parameters with a simulated 2φ-JJ device. To maintain clarity and minimize redundancy, we will only present an example layout of the OR gate in the summary section, providing readers with a preliminary physical view of the cell layouts.

A. Wiring Cells

1) JTL (2φ-JTL): Fig. 2 illustrates the schematic of a JTL block. Within this schematic, devices denoted by square boxes (J1 and J3) represent the 2φ-JJs, while those without boxes are 0-JJs (J2 and J4.) Notably, the structure is duplicated, meaning that J1/J3, J2/J4, and I1/I2 are identical. This design ensures the JTL cell's repeatability, allowing for the creation of a JTL chain by connecting the OUT port to a subsequent JTL IN port without introducing unnecessary components.

As depicted, J1 replaces the inductor that is present in the previous RSFQ JTL, forming a J1–J2–J3 loop that establishes a phase equation. This equation ensures that the integration of the phase difference, starting from the positive terminal of J1 through J2, FJ3, and back to J1, amounts to an integer multiple of 2π. When an HFQ pulse arrives from the IN port, J1 switches and generates another HFQ pulse, which then propagates to the next device. This mechanism facilitates the transmission of the HFQ pulse along the JTL. The simulation waveform is depicted in Fig. 3, and the component values can be found in Table I. Notably, the critical margin for JTL is 71% dictated by J1/J3.

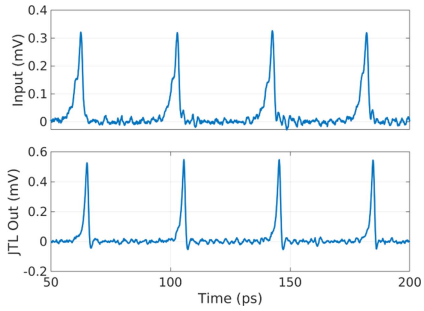

Fig. 3. Simulation of the JTL with added noise.

TABLE I
PARAMETER VALUES AND MARGINS OF JTL

Component	Value	Margin
J1,J3	$70\,\mu A$	71%
J2,J4	$80\,\mu A$	97%
I1,I2	$45\,\mu A$	88%
Bias	$1\,mV$	88%

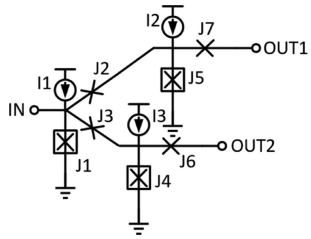

Fig. 4. Schematic of the splitter cell.

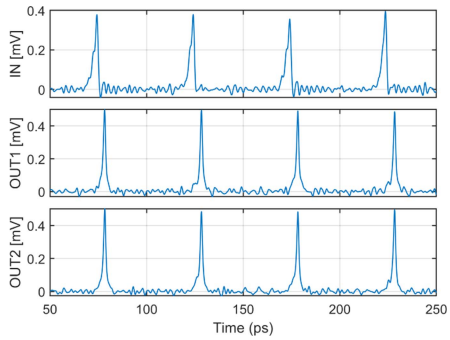

Fig. 5. Simulation of the splitter cell with added noise.

2) Splitter: Similar to SFQ cells, HFQ logic cells have a fan-out of one. Therefore, a splitter is employed to duplicate the pulse. Fig. 4 presents the schematic of the splitter cell. In this arrangement, J1 receives the pulse from the IN port, and the looping current is divided into two branches. This division triggers J5 and J4 separately, generating an HFQ pulse at each output port. The simulation waveform is displayed in Fig. 5, and the component values can be found in Table II. Notably, the critical margin for the splitter is 70% dictated by the current bias I2/I3.

3) Merger: Fig. 6 illustrates the schematic of the merger cell, often referred to as a confluence buffer. When it receives an HFQ

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TABLE II
PARAMETER VALUES AND MARGINS OF SPLITTER CELL

Component	Value	Margin	Component	Value	Margin
J1	65 μA	98%	I1	70 μA	100%
J2,J3	73 μA	99%	I2,I3	45 μA	70%
J4,J5	80 μA	88%	Bias	1 mV	88%
J6,J7	80 μA	90%			

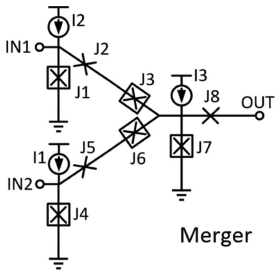

Fig. 6. Schematic of the merger cell.

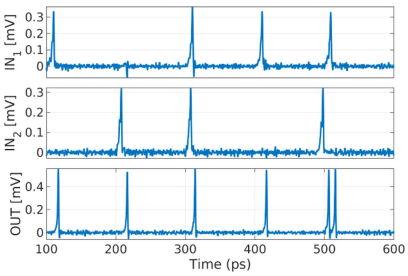

Fig. 7. Simulation of the merger cell with added noise.

TABLE III
PARAMETER VALUES AND MARGINS OF MERGER CELL

Parameter values and margins of merger cell

Component	Value	Margin	Component	Value	Margin
J1,J4	83 μA	75%	J8	93 μA	82%
J2,J5	151 μA	100%	I1,I2	27 μA	100%
J3,J6	62 μA	91%	I3	120 μA	81%
J7	40 μA	100%	Bias	1 mV	72%

pulse from either input port (e.g., IN1), the pulse triggers the corresponding junction (J1). This action increases the current in the respective branch (J1–J2–J3–J7), leading to the switching of J7, resulting in an output pulse. Concurrently, a buffering junction on the other branch (in this case, J6 for input from IN1) is triggered to counteract the backward flux flow toward the other input port (IN2). Specifically, J3 and J6 serve as barriers to prevent the reverse propagation of pulses. In the event that two input pulses arrive simultaneously or within a small time window (smaller than ∼9.5 ps), only one output pulse is generated at the OUT port. The simulation waveform is depicted in Fig. 7, illustrating both the input and output waveforms and the phases of J3 and J6 to demonstrate how they inhibit backpropagation. Detailed component values can be found in Table III. It is worth noting that the critical margin for the merger is 72%, determined by the overall bias voltage.

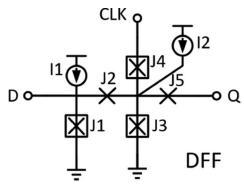

Fig. 8. Schematic of the DFF.

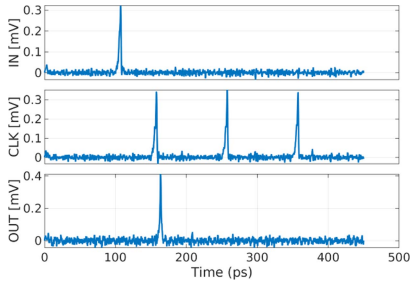

Fig. 9. Simulation of the DFF with added noise.

TABLE IV
PARAMETER VALUES AND MARGINS OF DFF

Component	Value	Margin	Component	Value	Margin
J1	63 μA	68%	J5	117 μA	97%
J2	65 μA	90%	I1	31 μA	100%
J3	86 μA	75%	I2	32 μA	100%
J4	74 μA	85%	Bias	1 mV	88%

B. Memory Cells

1) D Flip-Flop: Fig. 8 illustrates the schematic of the DFF. When an HFQ pulse arrives from the input port D, it is stored within the J1–J2–J3 loop as a clockwise looping current. This action increases the bias current of J3. Consequently, when an HFQ pulse arrives from the CLK port, it triggers J3, generating an HFQ pulse at the output port Q. In cases, where no HFQ is stored, the incoming pulse from CLK triggers the J4 junction, resulting in no output at Q. The simulation waveform is displayed in Fig. 9, and the component values are detailed in Table IV. Notably, the critical margin for the DFF is 68% dictated by J1.

Memory cells, such as DFF and logic gates, in this technology, similar to SFQ, are clocked. Hence, it is crucial to consider setup and hold times in these designs during functional verification. Therefore, while optimizing the cells with qCS, we provided all possible patterns within the input, clock, and output waveforms of the circuit under test. Moreover, a dedicated timeframe is allocated to account for potential scenarios caused by jitter, considering the test frequency of the circuits in the testbench. Here, the simulation results only include simplified waveforms to demonstrate the functionality for better visualization and understanding.

2) NDRO: Nondestructive read out memory cells are widely used as a memory unit in SFQ circuits. The DFF cell is a traditional DRO unit that stores a single bit of information. Its core architecture is a simple storage loop that stores flux from input and releases it to output by a clock signal. In contrast to the DRO,

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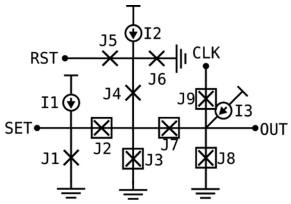

Fig. 10. Schematic of the 2φ-based NDRO memory cell.

TABLE V
PARAMETER VALUES AND MARGINS OF NDRO CELL

Component	Value	Margin	Component	Value	Margin
J1	$75\,\mu A$	100%	J7	$58\,\mu A$	100%
J2,	$63\,\mu A$	58%	J8	$48\,\mu A$	70%
J3,	$44\,\mu A$	94%	J9	$107\,\mu A$	76%
J4	$139\,\mu A$	94%	I1	$236\,\mu A$	100%
J5	$88\,\mu A$	57%	I2	$123\,\mu A$	70%
J6	$56\,\mu A$	97%	I3	$128\,\mu A$	75%

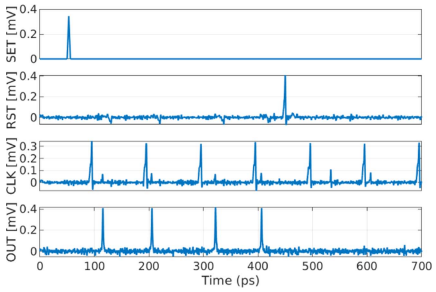

Fig. 11. Simulation of the NDRO cell with added noise.

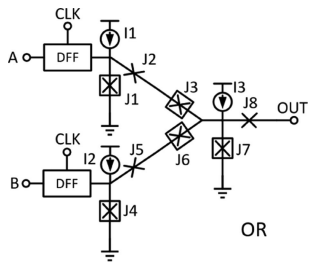

Fig. 12. Schematic of the OR gate.

NDRO does not release the pulse by the clock signal and requires a reset pin to clear the stored value within its storage loop. Fig. 10 shows the structure of the NDRO cell. The NDRO design values are given in Table V. The simulation waveform can be observed in Fig. 11.

C. Logic Cells

1) 2φ-OR: To grasp the concept of the OR gate's operation, consider it as two DFFs driven by the same clock and followed by a merger, as depicted in Fig. 12. The DFF cell has already been discussed, rendering it unnecessary to reiterate its details. The subsequent merging section possesses the same structure as the previously introduced merger. However, there are slight differences in component values as the tool automatically optimizes them. These optimized values are displayed in Table VI, with the critical margin being 40% dictated by J1/J4. The simulation waveform can be observed in Fig. 13.

TABLE VI
PARAMETER VALUES AND MARGINS OF OR GATE

Component	Value	Margin	Component	Value	Margin
J1,J4	$95\,\mu A$	40%	J8	$74\,\mu A$	69%
J2,J5	$100\,\mu A$	67%	I1,I2	$25\,\mu A$	93%
J3,J6	$83\,\mu A$	37%	I3	$83\,\mu A$	99%
J7	$68\,\mu A$	73%	Bias	$1\,mV$	44%

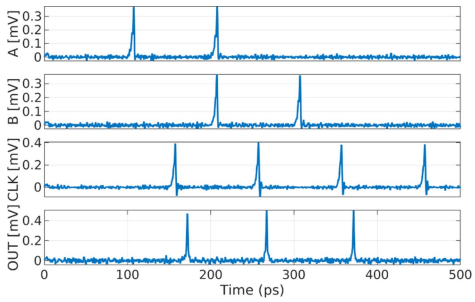

Fig. 13. Simulation of the OR gate with added noise.

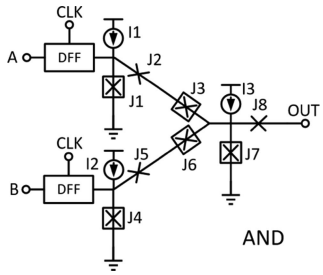

Fig. 14. Schematic of the AND gate.

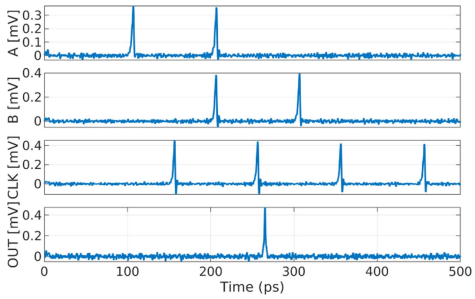

Fig. 15. Simulation of the AND gate with added noise.

2) 2φ-AND: As depicted in Fig. 14, the AND gate adopts an identical structure to the OR gate. However, it manipulates the key components, specifically the merging part, to ensure that the output junction J7 necessitates at least two HFQ pulses to generate an output pulse. The simulation waveform is illustrated in Fig. 15, and the component values are provided in Table VII. Notably, the critical margin for the merger is 85%, dictated by J8.

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TABLE VII
PARAMETER VALUES AND MARGINS OF AND GATE

Component	Value	Margin	Component	Value	Margin
J1,J4	70 μA	97%	J8	74 μA	85%
J2,J5	140 μA	99%	I1,I2	31 μA	100%
J3,J6	72 μA	94%	I3	32 μA	100%
J7	99 μA	98%	Bias	1 mV	92%

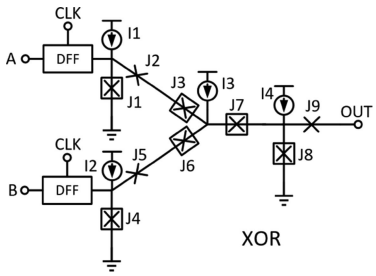

Fig. 16. Schematic of the XOR gate.

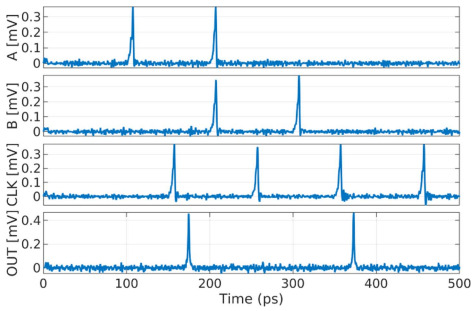

Fig. 17. Simulation of the XOR gate with added noise.

TABLE VIII
PARAMETER VALUES AND MARGINS OF XOR GATE

Component	Value	Margin	Component	Value	Margin
J1,J4	87 μA	46%	J9	80 μA	89%
J2,J5	95 μA	75%	I1,I2	31 μA	79%
J3,J6	72 μA	40%	I3	63 μA	88%
J7	70 μA	20%	I4	39 μA	39%
J8	72 μA	22%	Bias	1 mV	26%

3) 2φ-XOR: The schematic of the XOR gate is illustrated in Fig. 16. In contrast to the AND or OR gate, there is an additional junction (J7) after the merging point of the two input branches. With J7 in place, when pulses arrive from both branches (corresponding to the case: A = 1 and B = 1), J7 switches, while J8 remains inactive, resulting in no output pulse. Conversely, in situations where only one pulse is received from either of the branches (corresponding to the cases: A = 1, B = 0, or A = 0, B = 1), J8 is triggered, producing the output pulse. The simulation waveform is visualized in Fig. 17, and the component values can be found in Table VIII. Notably, the critical margin for the merger is 20%, dictated by J7.

4) 2φ-INV: Fig. 18 displays the schematic of an inverter. The upper section of the cell has a splitter-like structure, but one branch is merged with the clock branch of a DFF-like structure at the bottom. Consequently, when the clock signal arrives, the first part of the inverter generates "11" or "10" based on whether an input pulse was stored. Subsequently, the following XOR-like structure completes the inversion operation. The simulation waveform is depicted in Fig. 19, and the component values are provided in Table IX. Notably, the critical margin for the merger is 16%, dictated by J14 and J15.

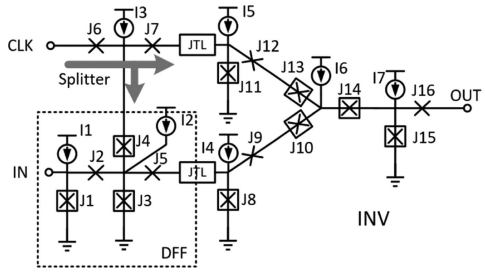

Fig. 18. Schematic of the inverter.

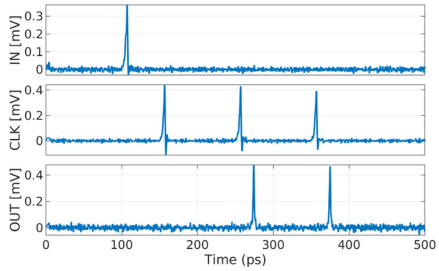

Fig. 19. Simulation of the inverter with added noise.

TABLE IX
PARAMETER VALUES AND MARGINS OF THE INVERTER

Component	Value	Margin	Component	Value	Margin
J1	85 μA	43%	J2	77 μA	69%
J3	95 μA	52%	J4	70 μA	48%
J5	82 μA	62%	J6	80 μA	81%
J7	80 μA	61%	J8,J11	96 μA	76%
J9,J12	101 μA	85%	J10,J13	78 μA	64%
J14	80 μA	16%	J15	82 μA	16%
J16	90 μA	67%	I1	43 μA	63%
I2	40 μA	79%	I3	57 μA	65%
I4,I5	37 μA	79%	I6	70 μA	73%
I7	40 μA	36%	Bias	1 mV	22%

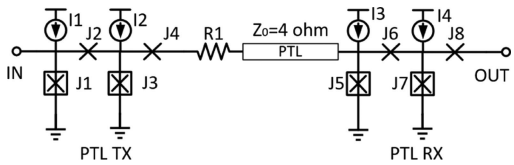

Fig. 20. Schematic of the PTL driver and receiver.

D. Interface Cells

1) PTL Driver and Receiver: Fig. 20 presents the schematic for both the PTL transmitter/driver (TX) and receiver (RX). These structures have JTL-like designs, with the PTL driver

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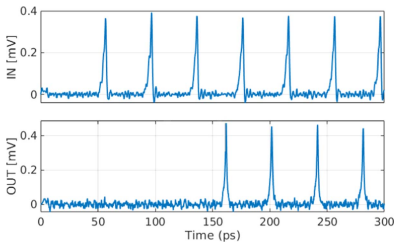

Fig. 21. Simulation of the PTL driver and receiver with added noise.

TABLE X
PARAMETER VALUES AND MARGINS OF PTL TX AND RX

Component	Value	Margin	Component	Value	Margin
J1	$80\,\mu A$	81%	J5	$75\,\mu A$	88%
J2	$80\,\mu A$	84%	J6	$61\,\mu A$	87%
J3	$70\,\mu A$	100%	J7	$80\,\mu A$	81%
J4	$83\,\mu A$	100%	J8	$80\,\mu A$	84%
R1	$0.5\,ohms$	100%	I3	$62\,\mu A$	81%
I1	$45\,\mu A$	88%	I4	$45\,\mu A$	88%
I1	$49\,\mu A$	94%	RX bias	$1\,mV$	88%
TX bias	$1\,mV$	100%			

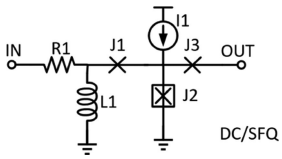

Fig. 22. Schematic of the dc/SFQ converter.

featuring a serial resistor at the output port for impedance matching. In this configuration, the characteristic impedance is set to 4 Ω, although designers can select practical values for their technology and adjust circuit parameters accordingly. The simulation waveform is displayed in Fig. 21, and the component values can be found in Table X. It is worth noting that the critical margin for the PTL driver is 81%, dictated by J1, and the critical margin for the PTL receiver is 81%, dictated by J7.

2) DC/SFQ Converter: Fig. 22 shows the dc/SFQ converter schematic. R1 is a serial input resistor that converts the input voltage to current. The resistor can be implemented ON-chip (this design) or OFF-chip. A large inductor L1 follows the input resistor. At the rising edge of the input, L1 reveals high impedance, and most of the current will flow through J2, which triggers an HFQ pulse at the output port. When the input voltage becomes steady, L1 is equivalent to a short connection, and the input current will flow through L1 to the ground, leaving J2 untouched. The simulation waveform is shown in Fig. 23, and the component values are listed in Table XI. The critical margin of the PTL driver is 98% on J1.

3) SFQ/DC Converter: Fig. 24 shows the SFQ/dc converter schematic. When an input pulse comes, it breaks the quiescent state of the cell and leads the output junction J5 to start oscillating. Another input pulse will then pull the cell back to its initial state. While in active mode, the SFQ/dc converter will keep

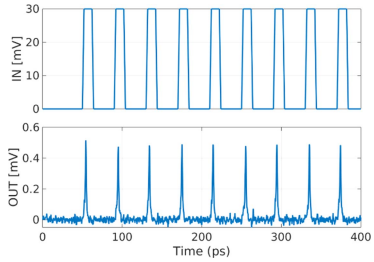

Fig. 23. Simulation of the dc/SFQ converter with noise.

TABLE XI
PARAMETER VALUES/MARGINS OF DC/SFQ CONVERTER

Component	Value	Margin	Component	Value	Margin
R1	$50\,ohms$	100%	I1	$48\,\mu A$	100%
J1	$83\,\mu A$	98%	L1	$6.7\,pH$	100%
J2	$71\,\mu A$	100%	Bias	$1\,mV$	100%
J3	$100\,\mu A$	100%			

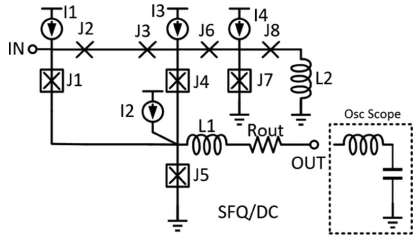

Fig. 24. Schematic of the SFQ/dc converter.

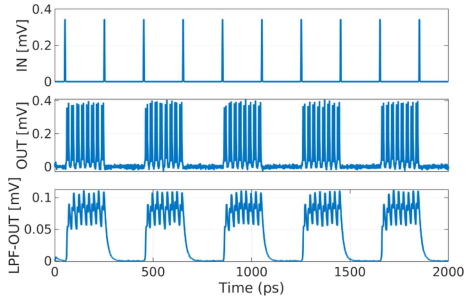

Fig. 25. Simulation of the SFQ/dc converter with added noise. After passing through a low-pass filter, the dc signal level shows around 100 μV amplitude.

pumping out current through the L1. The serial resistor R_{out} forms a low-pass filter with the OFF-chip wire inductance and the equivalent load of the oscilloscope, which is usually used to monitor the output of a chip. Fig. 25 shows the simulation waveform. The input signal is at the top. The middle plot is the observed voltage after L1, and the bottom is the signal at the oscilloscope. As we can see, the output state changes every time an input pulse comes. The component values are listed in Table XII. The critical margin of the PTL driver is 87% on the overall bias voltage.

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TABLE XII
PARAMETER VALUES/MARGINS OF SFQ/DC CONVERTER

Component	Value	Margin	Component	Value	Margin
J1	$112\,\mu A$	91%	J2	$104\,\mu A$	100%
J3	$70\,\mu A$	100%	J4	$78\,\mu A$	100%
J5	$70\,\mu A$	97%	J6	$80\,\mu A$	100%
J7	$80\,\mu A$	100%	J8	$80\,\mu A$	100%
L1	$0.5\,pH$	100%	L2	$3\,pH$	93%
I1	$45\,\mu A$	100%	I2	$26\,\mu A$	100%
I3	$48\,\mu A$	100%	I4	$22\,\mu A$	100%
Rout	$50\,ohm$	100%	Bias	$1\,mV$	87%

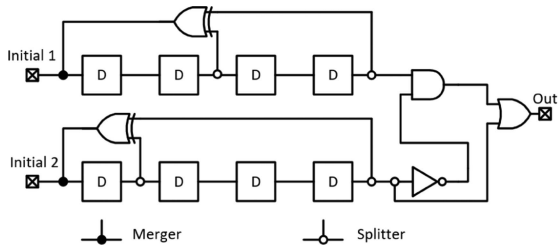

Fig. 26. Schematic of the pseudorandom pattern generator.

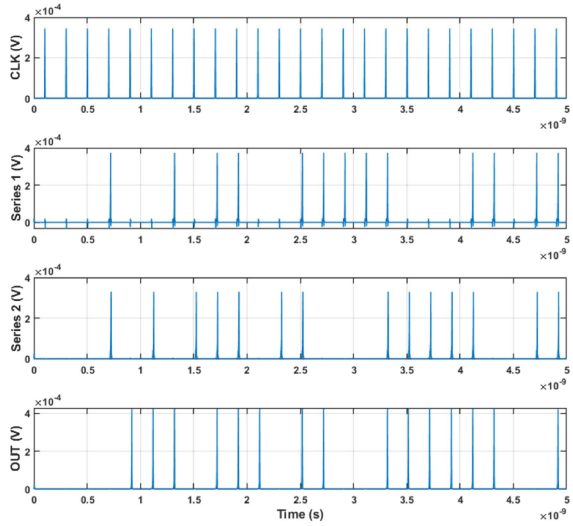

Fig. 27. Simulation of the pseudorandom pattern generator.

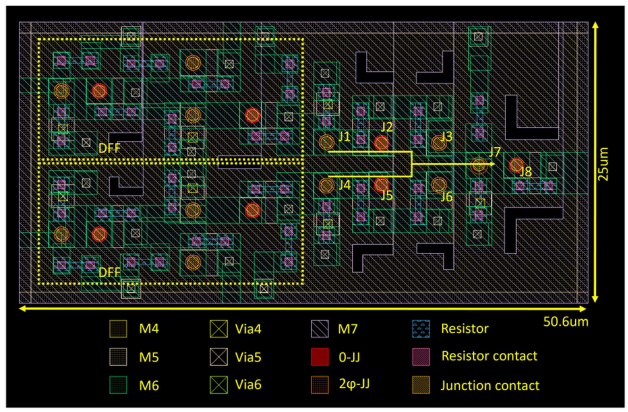

Fig. 28. Example layout of the OR gate.

IV. RESULTS AND IMPLEMENTATION

A. Pseudorandom Pattern Generator

A pseudorandom pattern generator has been implemented to evaluate the library cells, as depicted in the schematic shown in Fig. 26. Two DFF chains are formed, with signals tapped from various points in these chains using splitters. These signals are then directed to XOR gates. Subsequently, the outputs of the two XOR gates are combined with the initial signals, creating a feedback data loop and the overall function of an external linear feedback shift register. This configuration generates two random data series inputs to the subsequent stages: the AND gate, inverter, and OR gate. All cells in Fig. 26 are synchronized with a clock signal, although the clock signal is not displayed to maintain diagram clarity and readability.

Fig. 27 presents the simulation waveform of this microsystem. The top waveform represents the clock signal distributed to all the cells. "Series 1" and "Series 2" denote the bit series at the outputs of the two DFF chains, while "OUT" signifies the output of the final OR gate. This microsystem effectively demonstrates the correct functionality of the employed cells and showcases the system integration capability of the HFQ standard cells.

The above explanation described the HFQ standard cell library design utilizing the 2φ-junction. In addition, prototype layouts were created for each cell using a simulated technology based on the published MITLL SFQ5ee process. An extra layer, the 2φ-junction layer, was assumed to enable the implementation of the 2φ-junction. Fig. 28 illustrates the OR gate layout. The layout predominantly comprises four metal layers (M4–M7), three metal vias, one resistor layer, two junction layers for 0-JJ and 2φ-JJ, respectively, one resistor contact layer, and one junction contact layer. In Fig. 28, it is evident that eliminating the inductor results in a more compact layout. Furthermore, as technology advances, the area could potentially be further reduced. Table XIII provides a comprehensive list of all the cells implemented in this library, including the number of junctions (0-JJ and 2φ-JJ) and critical margins. It also compares estimated layout areas and bias current with a conventional RSFQ library we implemented [31]. On average, the HFQ cells exhibit a 50.8% reduction in area and a 61% decrease in bias current compared with the conventional RSFQ library.

B. Advantages, Limitations, and Feasibility

As demonstrated in Table XIII, the bistable junctions can provide a big advantage in reducing the size of circuits by eliminating inductors, reducing the required bias due to phase-shifted loops with constant currents, and increasing operating speed due to half-flux operation. The limiting factor in the wiring cell speed is the output switching junction's recovery time. For wiring cells, such as JTL, SPL, and merger, we could reach 100 GHz frequency in simulations. For the logic, such as AND, OR, and XOR, 70 GHz frequencies were achieved. The limiting factors in the clock speed in these circuits are setup and hold time between input data and clock pulses. While 2ϕ junctions are a promising

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TABLE XIII
SUMMARY OF THE 2φ-JJ BASED LIBRARY CELLS AND RSFQ COUNTERPARTS

Cell name	Number of JJs	Critical margin	Area reduction (%)	Bias current reduction (%)	Area (RSFQ)	Bias current (RSFQ)
JTL	4	71%	64	50	$625\ um^2$	$180\ \mu A$
DFF	5	68%	40	70	$625\ um^2$	$212\ \mu A$
NDRO	9	55%	75	44	$2500\ um^2$	$863\ \mu A$
Merger	8	72%	12	54	$625\ um^2$	$375\ \mu A$
Splitter	7	70%	21	48	$625\ um^2$	$309\ \mu A$
OR	18	37%	50	46	$2500\ um^2$	$475\ \mu A$
AND	18	85%	50	59	$2500\ um^2$	$530\ \mu A$
XOR	19	20%	43	33	$2500\ um^2$	$435\ \mu A$
PTL driver	4	81%	32	65	$625\ um^2$	$265\ \mu A$
PTL receiver	4	81%	41	58	$625\ um^2$	$252\ \mu A$
DC/SFQ converter	3	98%	75	89	$1875\ um^2$	$450\ \mu A$
SFQ/DC converter	8	87%	72	86	$3125\ um^2$	$1025\ \mu A$

technology, the fabrication process for these junctions is not mature yet. The current fabrication methods cannot produce a reliable 2ϕ-JJ and, hence, cannot be translated to large-scale circuit integration. To fabricate these circuits, two levels of JJs, 2ϕ and normal, are needed with several interconnection layers. Therefore, in the Expedition: DISCoVER project, one of our main tasks is investigating a scalable fabrication method for such circuits.

V. CONCLUSION

An HFQ standard cell library employing the 2φ-junction is demonstrated. The detailed design methodology encompasses schematic representations, component values, and their respective margins for each available block within the standard cell library. The library includes essential components, such as inverters, AND, OR, XOR gates, JTLs, splitters, mergers, PTL drivers, PTL receivers, DFFs, dc/HFQ converters, and HFQ/dc converters. Compared to conventional RSFQ cells, this new design necessitates less bias current, reduces reliance on inductors, enhances stability and scalability, and occupies about 55% smaller area. These advancements position the HFQ logic family as a compelling contender for the next generation of VLSI circuits.

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