One Ferroelectric Field-Effect Transistor and one Capacitor Ternary Content-Addressable Memory Based on Charge Domain Sensing Mechanism

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***Abstract*—In this work, one ferroelectric Field-Effect transistor one capacitor (1FeFET-1C) and two ferroelectric Field-Effect transistor two capacitor (2FeFET-2C) ternary content-addressable memory (TCAM) based on charge domain sensing mechanism are proposed and experimentally verified. These charge domain based sensing TCAM have good device variation immunity, high energy efficiency, and potentially high density integration ability due to similar structure with DRAM.**

***Index Terms*—Ternary Content-Addressable Memory (TCAM), Charge Domain Sensing, Ferroelectric Field-Effect Transistor (FeFET), Compute in Memory**

I. Introduction

Ternary Content Addressable Memory (TCAM) has found widespread applications in various domains such as IP address lookup [1], pattern matching, cache controllers in processors [2], and network intrusion detection systems [3]. Its ability to perform parallel research efficiently, with nanosecond scale latency, has recently drawn significant interest in the realm of artificial intelligence (AI). Traditional TCAM is SRAM-based so that the scaling down ability and standby power are some of the challenges [4]. Compare with the SRAM-based TCAM, the FeFET based TCAM as a kind of nonvolatile TCAM have the smaller cell area and reduced standby power consumption. Especially after the discovery of the ferroelectricity of Hf-based materials [5], the CMOS compatibility of ferroelectric devices are significantly improved. For commonly current sensing based TCAM design, sensing current are strongly various with search voltage, which means highly sensitive with devices variations. To address this challenge, we propose charge domain based sensing TCAM with 1FeFET-1C and 2FeFET-2C design. By using charge domain sensing mechanism, in which FeFET acts as a switch and its ON current does influence the sense current as long as it can pass the signal so that this design become more robust compared with current sensing based TCAM.

In this paper, we propose a charge domain based sensing TCAM based on 1FeFET-1C and 2FeFET-2C. Also their functionality are experimentally verified. These TCAM designs have the nonvolatile ability and also have a similar structure as DRAM, which yields a better compatibility with 3D DRAM-like integration.

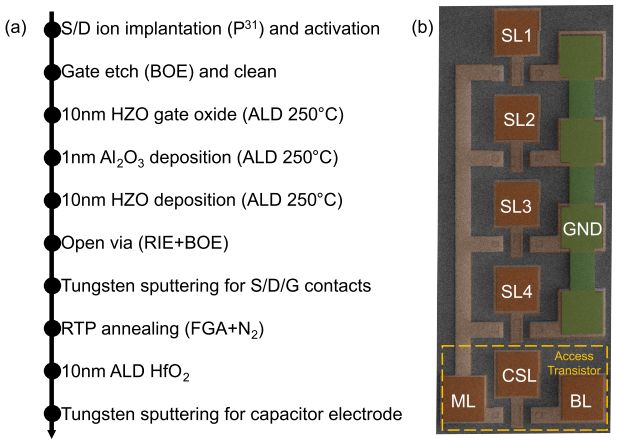

Fig. 1. (a) Process flow and (b) SEM image of 4×1 1FeFET-1C array with one access transistor.

II. Fabrication

The fabrication process for our TCAM cell and array is shown in Fig. 1(a). After the Source and Drain (S/D) ion implantation and activation are performed, gate trench are formed by reaction ion etch (RIE) combined with buffered oxidant etchant (BOE) wet etch. After that, a HZO(10 nm)/AL_2O_3(1 nm)/HZO(10 nm) gate stack is deposited by atomic layer deposition (ALD). Then the S/D via is opened and followed by tungsten (W) sputtering as the bottom electrode of capacitor. Subsequently, a 10 nm HfO_2 layer is deposited by ALD as the dielectric layer for capacitor and 100 nm W is sputtered as the top electrode. Finally, 1 min 500 °C in forming gas and N_2 atmosphere annealing is performed in N_2 to crystallize the ferroelectric layer. The scanning electron microscopy (SEM) image of the a 4×1 array with one access transistor is shown in Fig. 1(b).

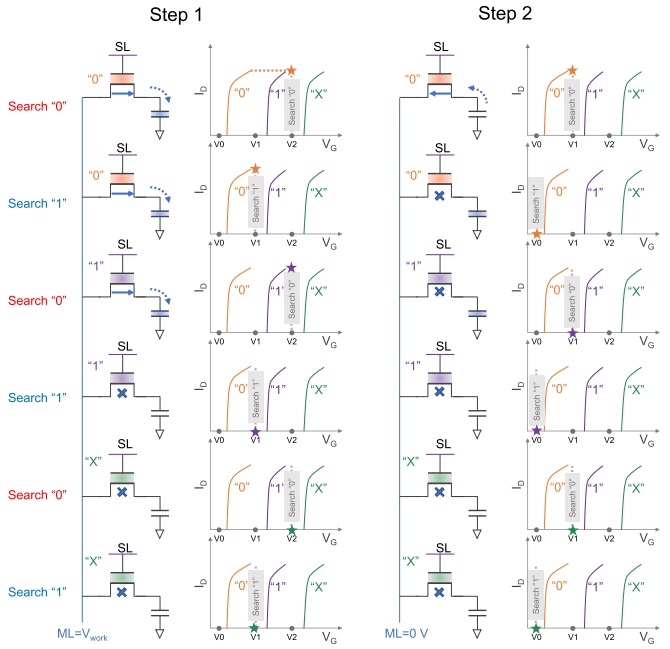

Fig. 2. Operation principle of charge domain sensing based 1FeFET-1C TCAM.

III. 1FeFET-1C TCAM Design

In our 1FeFET-1C TCAM design, we utilize three states of FeFET. Here, we define the low-V_{th} state, middle-V_{th} state, and high-V_{th} state as the "0", "1", and "X" TCAM state, respectively. The gates of FeFET in one array are connected to independent search lines (SL), and the source of FeFET are connected to one match line (ML) together. The entire operation waveform for 1FeFET-1C TCAM includes initial, charge and charge sharing sequences. Initial or write sequence set FeFET in one cell or in array to specific polarization states or TCAM state. Following is a two step charge sequence whose detail is shown in Fig. 2. The voltage of match line (V_{ML}) are set V_{work} and 0 V in step 1 and step 2, respectively. For search "0" operation, we applied V_2 and V_1 in step 1 and step 2 at all search lines. V_2 is between the V_{th}s for "0" and "1" states. V_1 is between the V_{th}s for "1" and "X". Thus, for search "0" operation, capacitors in cells for "0" and "1" state will be charged in first step 1, and capacitors in cells for "0" will be discharged in step 2. So, after search "0" operation, only cells in state "1" will be charged. For search "1" operation, we applied V_1 and V_0 at search line in step 1 and step 2. V_0 is below the V_{th}s for "0" . Thus, for search "1" operation, only capacitors in cells for "1" state will be charged in first step 1, and no capacitors will be discharged in step 2. So, after search "1" operation, only cells in state "0" will be charged. And we can easily see that cells in state "X" will never be charged for both search "0" and "1" operation because the transistors have high V_{th}. After performing charge sequence, the ML is floated, the charges in capacitors inside each cell will be shared, which will be amplified by sense amplifier. In our experiment, ML floating operation is realized by turning off the Access transistor through biasing cell select line (CSL).

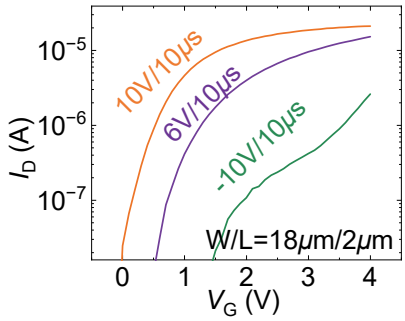

Fig. 3. Transfer curves of FeFET during three different pulse amplitudes.

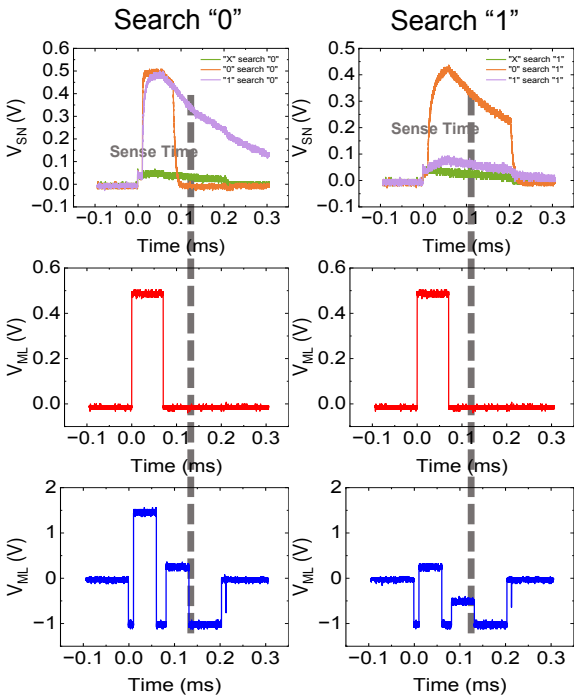

Fig. 4. Waveform and output of sense node during search "0" and "1" operation for states "0", "1", "X" for 1FeFET-1C design.

Firstly, The FeFET characteristics was experimentally demonstrated. Channel length and width of the FeFET is 2 and 18 μm, respectively. Fig. 3(a) illustrates the transfer curves of FeFET after applying pulses with different amplitudes. Low-V_{th}, middle-V_{th} and high-V_{th} states are obtained by applied pulses with 10 V, 6 V and -10 V. All pulse widths are 10 μs. According to the transfer curves for three states, operation parameters V_0, V_1, V_2 and V_{work} are chosen as -0.5, 0.6, 1.1 and 0.5 V, respectively. And V_{th} shift between each state are larger than 0.5 V, which makes it easy to recognize.

Secondly, we verified the functionality of TCAM in one cell, the area of capacitor inside each cell is 50×50 μm^2. During this test, we exchange the role of access transistor and cell transistor, in which case we could detect the voltage of capacitor by keeping access transistor on all the time and monitoring the voltage of sense node (V_{SN}) or V_{ML} using oscilloscope. The waveform and output result (Fig. 4 (a)) shows correct functionality of this 1FeFET-1C TCAM cell.

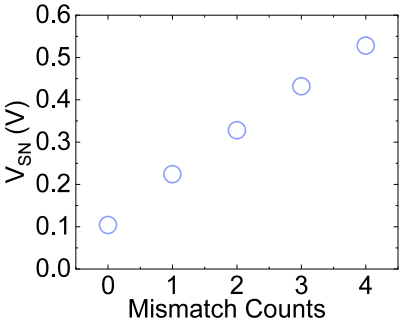

Fig. 5. Sense node voltage for different mismatch counts.

At sense time, only when TCAM state mismatch the search state, V_{SN} is at high level (∼0.3 V). Otherwise, $V_{SN}$is low level (∼50 mV). So the sense margin is ∼6.

Finally, the Hamming distance calculate ability is verified in a 4×1 array with one access transistor. During this test, the initial state of this array is set as ”0000” and then search ”0001” ”0011” ”0111” and ”1111”, respectively. After performing charge operation and floating match line, the charges in capacitors inside each cell will be shared. After charge sharing, the output of V_{ML} is sensed, which is shown in Fig. 5. The sense voltage shows obviously linear trend with mismatch bits. Thus, this result demonstrates that 1FeFET-1C TCAM can successfully sense the number of mismatch bits, which is Hamming distance between search data and stored data.

IV. 2FeFET-2C TCAM Design

Another available Charge domain sensing based TCAM design is 2FeFET-2C. And which is different from 1FeFET-1C design is that only two ferroelectric polarization state are used. This design can be adopted when multi-state can not be achieved in FeFET with gate-stack scaling. The basic operation principle is shown in Fig. 6. In this design, only one charge sequence are required.

In this design, LVT-HVT, HVT-LVT, and HVT-HVT states combinations are defined as state ”0”, ”1”, and ”X”, respectively. For search ”0” operation, V_0 and V_1 and V_{ML} are applied on SL_1 and SL_2 and V_{work}, respectively. Thus, only the second capacitor are charged in state ”1” cell. For search ”1” operation, V_1 and V_0 and V_{ML} are applied on SL_1 and SL_2 and V_{ML}, respectively. Thus, only the first capacitor are charged in state ”0” cell. To verify this 2FeFET-2C TCAM, same sample are used. V_{work} are set 1 V. The search results are shown in Fig. 7. For mismatch case, V_{SN} is low voltage (∼50 mV). And for mismatch case, that is ∼150 mV.

Conclusion

In this work, we proposed two kinds of charge domain based sensing TCAM using 1FeFET-1C or 2FeFET-2C structure and its functionality is verified experimental. By adopting this charge domain sensing, the effect of device variations can be weakened. And because FeFET are used as the memory unit, nonvolatile performance and low standby power can be realized compare with SRAM-based TCAM. Also, 1FeFET-1C cell is similar with DRAM so that it could be high density integrated like 3D DRAM.

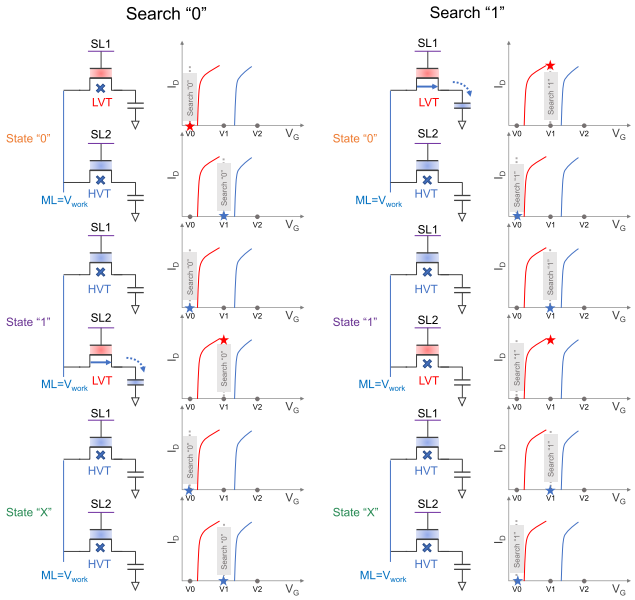

Fig. 6. Operation principle of charge domain sensing based 2FeFET-2C TCAM.

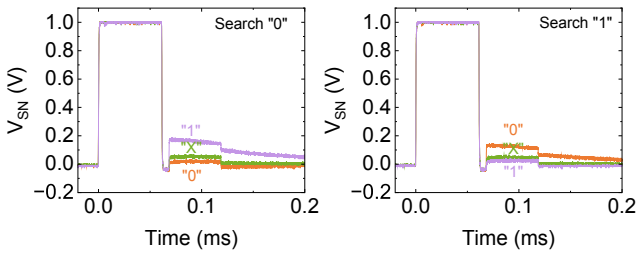

Fig. 7. Output of sense node during search ”0” and ”1” operation for states ”0”, ”1”, ”X” for 2FeFET-2C design.

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