An Offset Calibration Scheme for On-Chip Thermal Profiling with Differential Temperature Sensors

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Abstract

This paper introduces an on-chip analog calibration method tailored for differential temperature sensors in thermal monitoring applications. A three-step calibration process is proposed within a two-stage high-gain instrumentation amplifier (IA) to compensate for the output voltage offset due to device mismatches and on-chip temperature gradients. The calibration circuits were designed in a standard 65 nm CMOS process for simulation. Results indicate that an input-referred offset with a mean of $\mathbf{0.2\ \mu V}$ can be achieved after calibration, through which the standard deviation is greatly reduced from $\boldsymbol{\sigma = 880.3\ \mu V}$ to $\boldsymbol{\sigma = 5.86\ \mu V}$. Furthermore, the proposed analog offset calibration scheme has negligible impact on the sensitivity of the complete temperature sensor circuit, as shown by Monte Carlo and process-temperature corner simulation results.

Keywords: Differential temperature sensor, offset reduction, analog calibration, hardware security, built-in testing.

1 Introduction

On-chip calibration has been a handy tool in various applications ranging from analog [5, 10, 13, 14] and mixed-signal [8, 9, 16, 19] systems to radio frequency (RF) [1, 7, 11] system-on-a-chips (SoCs). The methods include but are not limited to chopper stabilization ([5, 6, 14, 16]) as well as digital offset detection and cancellation ([9, 19]). Over the past years, the effectiveness of on-chip calibrations in different applications has been assessed and demonstrated through both measurement [5, 10, 13, 14] and simulations [1, 7–9, 11, 16, 19]. On the other hand, on-chip temperature sensors have been employed for RF power/-linearity built-in-testing [3, 4, 12], temperature-based hardware Trojan detection [15, 17, 18], and monitoring of device aging [2], where the non-intrusive nature of the BJT-based temperature sensing scheme allows to avoid electrical loading effects during on-chip thermal profiling. In particular, the effectiveness of on-chip monitoring with a differential temperature sensor has recently been demonstrated in [2] with a microcontroller-based approach at the printed circuit board level to automatically tune a power amplifier for compensation of performance degradation over time.

A conceptual diagram of a differential temperature sensor with a BJT-based sensing front-end and an instrumentation amplifier (IA) is displayed in Fig. 1, where the temperature sensing front-end includes a pair of vertical bipolar-junction transistors (BJTs) [12] and a transimpedance amplifier (TIA) with chopper and low-pass filter (LPF). The TIA with an integrated chopper and an LPF has been proven effective in suppressing low-frequency flicker noise while maintaining high transimpedance gain [15]. A two-stage IA contributes to additional gain-boosting (e.g., gain $\approx$ 400 as in [17]). The 65 nm CMOS example sensor design utilized in the presented assessment of the calibration method has a temperature sensitivity

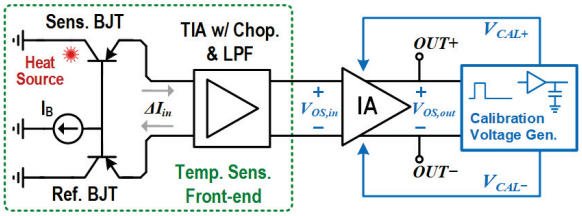


Fig. 1 Differential temperature sensing system with a BJT-based sensing front-end [15, 17, 18], and a high-gain IA with analog foreground calibration.

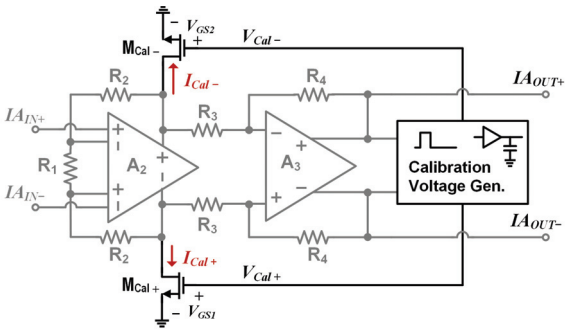


Fig. 2 Two-stage instrumentation amplifier (IA) with analog foreground calibration using current subtraction transistors.

of $675.5\,\mathrm{V/^{\circ}C}$, which is similar to the $840\,\mathrm{V/^{\circ}C}$ sensitivity of the 130 nm CMOS design in [17].

DC offsets that appear at the IA input (i.e., from residue offset of the chopping TIA, the inherent input-referred offset of the IA, BJT mismatch, low-frequency thermal gradients on the chip, etc.) will be amplified by the IA and can saturate the final output. Therefore, the use of an offset reduction method is essential, such that a calibration step can be executed to drive the differential output voltage to zero prior to measurement. To the best of the authors' knowledge, this paper presents an integrated automatic analog offset calibration scheme for an on-chip differential temperature sensor for the first time.

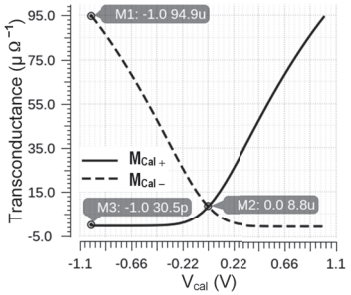
The remainder of this paper is organized as follows: Section 2 introduces the proposed analog calibration scheme for a two-stage IA, Section 3 presents the circuit-level design details. Simulation results of the complete differential temperature sensor with proposed offset calibration are covered in Section 4. Section 5 draws the conclusion.

2 Proposed Offset Calibration Scheme for a Two-stage Fully-differential IA

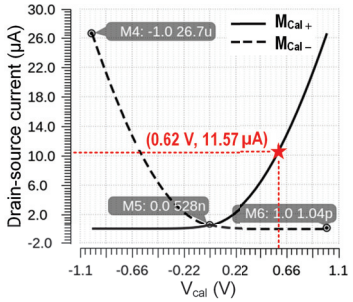
A simplified block diagram of the proposed calibration loop for a two-stage IA is displayed in Fig. 2. The calibration voltage generation block senses the output DC offset of the IA and generates the calibration voltages ($V_{Cal\pm}$). Two current subtraction NMOS transistors ($\mathrm{M_{Cal\pm}}$) are connected to the first-stage feedback loop of the IA and remain turned off when $V_{Cal\pm} = 0$. Depending on the sensed IA output voltage, either $\mathrm{M_{Cal+}}$ or $\mathrm{M_{Cal-}}$ will be turned on such that the current flow depends on the gate-source voltages, where $V_{GS1} = V_{Cal+}$, $V_{GS2} = V_{Cal-}$ (Fig. 2). Note that this analog calibration is designed to operate in the foreground prior to a temperature measurement, which implies that the calibration voltage generation block is deactivated before the input signal is processed, such that only the IA's DC offset is suppressed and not the differential input signal. On the other hand, the obtained gate-source voltages of $\mathrm{M_{Cal\pm}}$ (i.e., $V_{Cal\pm}$) have to be held to generate the proper calibration currents (i.e., $I_{Cal\pm}$) until the measurement is completed. Hence, the $V_{Cal\pm}$ generation is designed in a "sample-and-hold" manner, where an amplifier senses the output offset and generates the gate control voltages $V_{Cal\pm}$, while two metal-insulator-metal (MIM) capacitors hold the generated voltages during and after the calibration. The details of the calibration process will be discussed in Section 3.

As is labeled in Fig. 2, the calibration current is subtracted from the first-stage feedback loop of the IA. Based on the sensed output DC offset, either $\mathrm{M_{Cal+}}$ or $\mathrm{M_{Cal-}}$ is activated and pulling current from the feedback network to drive the output offset voltage towards zero. Note that if no DC offset is present at the IA output ($\mathrm{IA_{OUT+}} = \mathrm{IA_{OUT-}}$), then both transistors remain in the cutoff or subthreshold region such that negligible DC current is consumed. To minimize power consumption, the main calibration circuitry is deactivated after the calibration as discussed in Section 3, whereas the gate control voltages of $\mathrm{M_{Cal\pm}}$ are held by capacitors.

To properly select the dimensions of the $\mathrm{M_{Cal\pm}}$ transistors, Monte Carlo (MC) simulations were completed with 100 runs to ensure that the transistors are able to subtract the required calibration currents ($I_{Cal\pm}$) in all MC cases. Considering the potential gate leakage, an NMOS transistor type with a thick gate oxide and a deep N-well (DNW) was selected for current subtraction. The dimensions of the DNW NMOS transistors are $1\,\mu\mathrm{m}/1.1\,\mu\mathrm{m}$, and their simulated DC characteristics are displayed in



(a) Transconductance (g_m).



(b) Drain-source current (I_{ds}).

Fig. 3 Simulated DC characteristics of the current-subtracting transistors within the analog calibration loop.

Fig. 3. When the differential gate-control voltage (i.e., $V_{Cal} = V_{Cal+} - V_{Cal-}$) is swept from -1 V to $+1$ V, we can observe that the transconductance (g_m) of the DNW NMOS varies from 30.5 $\mathrm{p\Omega^{-1}}$ to 94.9 $\mu\Omega^{-1}$, and the corresponding calibration current ranges from 1.04 pA to 26.7 μA. Without DC offset, both $\mathrm{M_{Cal+}}$ and $\mathrm{M_{Cal-}}$ are biased in the subthreshold region and subtracting an equal drain-source current of I_{ds}= 528 nA [Fig. 3(b)] from the IA feedback loop. The labeled example values (V_{Cal}= 0.62 V, I_{ds}= 11.57 μA) in Fig. 3(b) were obtained from one voltage calibration instance in the presence of devices mismatches, which will be discussed in Section 4. Note that the gate-control voltages ($V_{Cal\pm}$) can also be designed to bias $\mathrm{M_{Cal\pm}}$ in the cutoff region by shifting the output common-mode level of the calibration amplifier if desired. The design of the calibration amplifier is discussed in Section 3.

3 Circuit Design Considerations

3.1 Calibration Voltage Generation and Control Logic

The calibration voltage generation technique in Fig. 4 consists of three major parts: (1) a calibration amplifier that senses the output voltage difference at the IA output ($\mathrm{IA_{OUT\pm}}$) and generates gate-control voltages ($V_{Cal\pm}$) for the current subtraction transistors ($\mathrm{M_{Cal\pm}}$ in Fig. 2); (2) a pair of low-leakage charge-storing capacitors ($\mathrm{C_{S/H}}$) that sample and hold the generated $V_{Cal\pm}$ voltages, and which provide a constant bias for $\mathrm{M_{Cal\pm}}$ until each temperature measurement is finished; (3) an on-chip control clock (CLK) generation block that provides signals to time the set, sample-and-hold, and calibration phases for the on-chip switches. Transmission gates were selected as switches in the signal paths under consideration that the input/output signal varies within a wide range (due to the amplified initial DC offset).

Two 51 pF metal-insulator-metal (MIM) capacitors were employed as the charge-storing capacitors ($\mathrm{C_{S/H}}$), with each capacitor having dimensions that correspond to a layout area of 80×80 $\mu\mathrm{m}^2$. The leakage of the charge-storing MIM capacitors ($\mathrm{C_{S/H}}$) was evaluated using foundry-supplied device models from the process design kit (PDK). Process-voltage-temperature (PVT) simulations revealed that the stored calibration voltages (e.g., V_{Cal} =600 mV) reduce by 30 mV over 2.64 seconds (ΔT_{leak}) in the nominal corner (i.e., TT, 27°C), with variations between 2.25 and 3 seconds over the other corner cases. Hence, the maximum leakage current across PVT corners can be estimated to be $I_{leak} = \mathrm{C_{S/H}} \cdot \Delta V_{Cal}/\Delta T_{leak} \approx$ 0.7 pA. The designated measurement time in this work is 64 ms (discussed in Section 3); therefore, the voltage error due to MIM capacitor leakage according to simulations is negligible ($< 0.2\%$) within such a short time.

As shown in Fig. 4, the series transmission gates in the input/output signal paths are controlled by ϕ_1, while the shunt transmission gates of the charge-storing capacitors are controlled by ϕ_2. The offset voltage calibration consists of three major steps (Table 1):

1. ϕ_1 is `Low`, ϕ_2 is `High`: both $\mathrm{SW_1}$ and $\mathrm{SW_A}$ are open, whereas the shunt transmission gates ($\mathrm{SW_2}$) are closed. The calibration amplifier is gated while the charge-storing capacitors are short to ground ($V_{Cal\pm} = 0$). Hence, the current subtraction NMOS transistors in Fig. 2 are turned off, and no calibration current is subtracted from the IA feedback network ($I_{Cal\pm} \approx 0$).
2. ϕ_1 is `High`, ϕ_2 is `Low`: both $\mathrm{SW_1}$ and $\mathrm{SW_A}$ are closed while the shunt transmission gates ($\mathrm{SW_2}$) are open. The calibration amplifier is activated and generates the gate-control voltages ($V_{Cal\pm}$) based

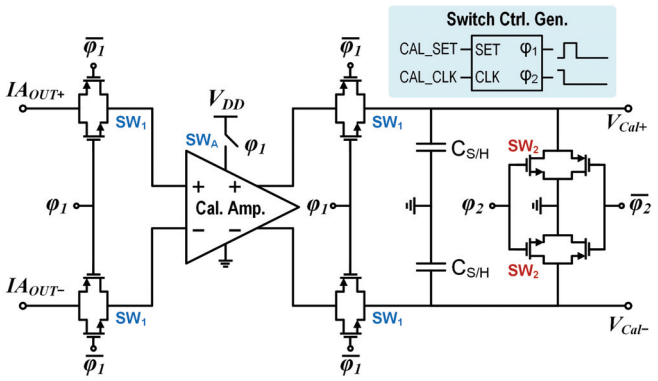


Fig. 4 Block diagram of the analog calibration circuitry with transmission gates, charge-storing capacitors, open-loop amplifier, and switch control generator.

on its input voltage difference (i.e., the sensed IA output offset). The calibration amplifier output is stored on $\mathrm{C_{S/H}}$, and controls the gates of the current subtraction transistors in the IA feedback loop.

3. ϕ_1 is `Low`, ϕ_2 is `Low`: all transmission gates ($\mathrm{SW_1}$, $\mathrm{SW_A}$ and $\mathrm{SW_2}$) are open. The calibration amplifier is gated to isolate its output from the current subtraction transistors. Meanwhile, the charge-storing capacitors ($\mathrm{C_{S/H}}$) continue to hold the generated gate-control voltages ($V_{Cal\pm}$) until the RST signal is triggered, and all transmission gates will be reset [Step (1)].

Fig. 5 displays the block diagram of the calibration CLK generation logic, which includes (i.) a synchronous 10-to-1 frequency divider that can be directly clocked using a 10-kHz system CLK signal; (ii.) an asynchronous counter that generates multiple clock signal outputs; and (iii.) a combinational logic block that converts the counter outputs to two control phases (ϕ_1 and ϕ_2). Both, the 10-to-1 frequency divider and the asynchronous divider, consist of DFFs with SET and RST controls. SET is directly controlled by a digital trigger signal, which activates the foreground calibration on demand and remains `High` until the end of each monitoring phase. On the other hand, RST is generated automatically and resets all DFFs once the measurement phase is complete. In this case, RST is triggered by the `High` output (Q5) of DFF5, which signals the end of each temperature monitoring period and resets all DFFs at the same time. Both the frequency divider and the counter are gated when RST is triggered, and all DFFs will remain gated until the next time SET is switched `High` through the designated input, such that a new sequence of "calibration-and-monitoring" operation is initiated.

The corresponding timing diagram of the calibration timing signal generation is shown in Fig. 6, where CLK, SET, ϕ_1 and ϕ_2 are displayed. To allow enough time for the charge-storing capacitors ($\mathrm{C_{S/H}}$) to sample the amplifier output (Fig. 4), 40 CLK cycles are assigned to the offset calibration phase, where the calibration amplifier is sensing the IA output offset and generating the gate-control voltages to be stored on $\mathrm{C_{S/H}}$. Another 40 CLK cycles are reserved ahead of the calibration (phase (1) in Fig. 6), such that the charge-storing capacitors ($\mathrm{C_{S/H}}$) are fully reset (i.e., $V_{Cal\pm} = 0$). Meanwhile, 560 CLK cycles are assigned to (3) (not fully shown in Fig. 6), where the charge-storing capacitors ($\mathrm{C_{S/H}}$) continue to hold the gate-control voltages ($V_{Cal\pm}$) until the on-chip temperature measurement is finished. Given a clock frequency of f_{CLK}= 10 kHz, the total amount of time for each measurement is 64 ms [4 ms for Step (1), 4 ms for (2), and 56 ms for (3)]. Adjustable calibration and measurement time can be obtained by changing the CLK frequency accordingly.

3.2 Offset-Sensing Amplifier with Deactivation Switches

As illustrated in Fig. 4, the calibration amplifier has to be gated before the calibration is activated and after the calibration has been completed. Instead of using a single power switch to disconnect the supply (V_{DD}) from the amplifier, multiple smaller NMOS transistors were added as enable/disable switches such that the calibration amplifier can be efficiently activated and deactivated without placing switches directly into the supply current path. Fig. 7 displays the schematic

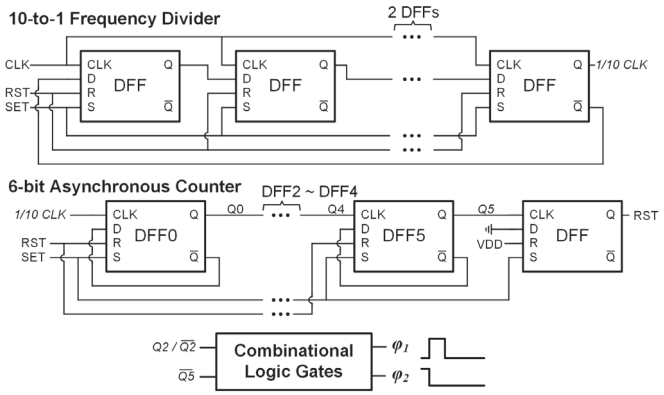


Fig. 5 Block diagram of the 3-step switch control generation in Fig. 4.

Table 1 Overview of the 3-step calibration process (Fig. 4)

	(1)	(2)	(3)
ϕ_1	Low	High	Low
ϕ_2	High	Low	Low
$\mathrm{SW_{1,A}}$	Open	Closed	Open
$\mathrm{SW_2}$	Closed	Open	Open
Cal. Amp.	Gated	Activated	Gated
$\mathrm{C_{S/H}}$	Short to ground	Hold $\mathrm{V_{Cal\pm}}$	Hold $\mathrm{V_{Cal\pm}}$
Operation	$\mathrm{C_{S/H}}$ reset	Offset calibration	Done

of the proposed calibration amplifier with deactivation switches:

1. When ϕ_1 transitions to `High` (Step (2) in Table 1), the enable NMOS ($\mathrm{M_{n1}}$) switch is closed and connects the gate-bias voltage for the current generation transistors ($\mathrm{M_3}$ and $\mathrm{M_4}$). The disable switches $\mathrm{M_{n2}}$ and $\mathrm{M_{n3}}$ remain open, such that their high off-resistance results in a negligible impact on the biasing and signal paths. Therefore, the calibration amplifier is activated during Step (2) in Fig. 6.
2. When ϕ_1 transitions to `Low`, the enable switch transistor ($\mathrm{M_{n1}}$) opens and isolates the bias current (I_{bias}) from the current-generation transistors of stage 1 ($\mathrm{M_3}$) and stage 2 ($\mathrm{M_4}$). Meanwhile, switches $\mathrm{M_{n2}}$ and $\mathrm{M_{n3}}$ are closed and create short circuits from node X to V_{DD}, and from node Y to ground, respectively. Since node X and node Y are pulled up/down accordingly, the output stage of the calibration amplifier is completely deactivated. When $\mathrm{M_4}$ and $\mathrm{M_5}$ are turned off during $\phi_1 = \mathtt{Low}$, the high off-resistance in series with $\mathrm{SW_1}$ (Fig. 4) minimizes the leakage current from $\mathrm{C_{S/H}}$, such that the calibration voltage ($V_{Cal\pm}$) stored on $\mathrm{C_{S/H}}$ can be held with negligible change until the end of each measurement.

Note that the node labeled V_{bias} in Fig. 7(b) shares same gate bias voltage as transistors $\mathrm{M_3} \sim \mathrm{M_4}$ of the calibration amplifier in Fig. 7(a).

4 Simulation Results

Fig. 8 displays an example case of the offset calibration obtained through Monte Carlo simulation with device mismatches, where the generated control voltage ($V_{Cal\pm}$) and sensed IA output voltages ($\mathrm{IA_{OUT\pm}}$) are plotted alongside the timing signals of the 3-step operation. It can be observed that the initial IA output offset is around 400 mV in this case. Before the calibration is activated, the calibration voltages ($V_{Cal\pm}$) are pulled down to the ground by the shunt transmission gates ($\mathrm{SW_2}$) of the charge-storing capacitors (Fig. 4), and the IA output offset is uncompensated. When ϕ_1 transitions to `High` and ϕ_2 to `Low`, the calibration amplifier is activated and generates the gate control voltages (i.e., $V_{Cal\pm}$) for the current-subtraction transistors ($\mathrm{M_{Cal\pm}}$). When a certain amount of current is drawn from the IA feedback network (Fig. 4), the IA output offset is brought down from 401 mV to 1.4 mV. In this example, given $V_{Cal+} = 1.06\,\mathrm{V}$ and $V_{Cal-} = 0.44\,\mathrm{V}$, the current-subtraction NMOS on the positive side ($\mathrm{M_{Cal+}}$) is

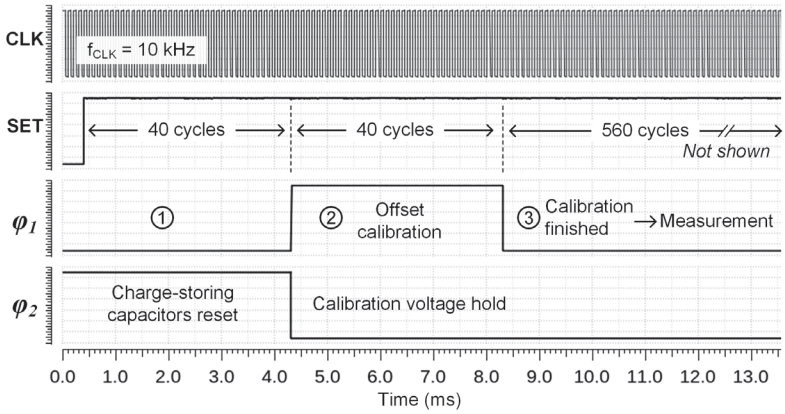
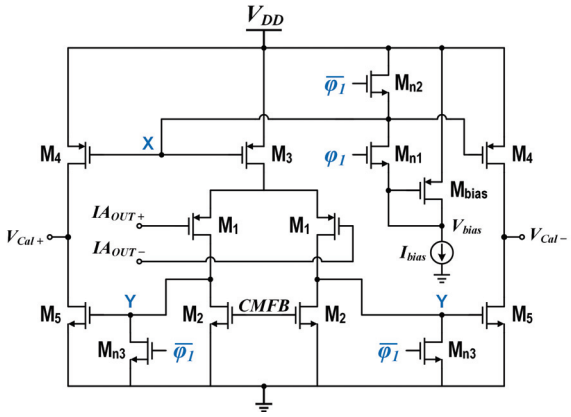
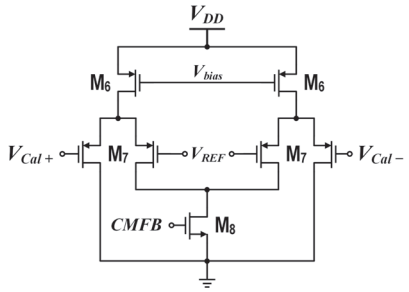


Fig. 6 Timing diagram of the 3-step switch control (Fig. 5) for the offset voltage calibration.



(a) Calibration amplifier with enable/disable switches.



(b) Common-mode feedback (CMFB) circuit.

Fig. 7 Schematic of the calibration amplifier with enable/disable switches and common-mode feedback.

turned on and biased in the saturation region, whereas $\mathrm{M_{Cal-}}$ is turned off (i.e., $I_{Cal-} \approx 0$). Hence, the total subtracted current through $\mathrm{M_{Cal+}}$ can be estimated to be 11.57 µA according to the i_{ds}-V_{Cal} plot shown in Fig. 3(b). The charge-storing capacitors ($\mathrm{C_{S/H}}$) continue to hold the calibration voltages until the end of the temperature measurement phase. Since $f_{CLK} = 10$ kHz is used as the calibration clock here, the assigned lengths of the phases for each measurement are: 4 ms of $\mathrm{C_{S/H}}$ reset (40 CLK cycles), 4 ms of voltage calibration (40 CLK cycles), and 56 ms of $V_{Cal\pm}$ hold for measurement (560 CLK cycles).

Fig. 9 displays the simulated transient IA outputs from 200 Monte Carlo runs, which illustrates the three typical phases of the proposed analog calibration loop: (1) before, (2) during, and (3) after calibration. The results show that the designed 3-step foreground calibration is capable of compensating for a wide range of IA offsets. Please note that although 4 ms is assigned to Step (2) in this proof-of-concept design, the actual settling time of the calibration loop is around 300 µs, as can be seen in Fig. 8. Therefore, the calibration logic control shown in Fig. 5 (and Fig. 6) can be reconfigured to minimize the total amount of calibration time, if necessary in a particular application. In other words, only 300 µs are required to calibrate the IA offset before each temperature measurement. The simulated transient gain of the IA was also evaluated to be 384 V/V, where a 50-Hz differential sinusoidal signal with an amplitude of 1 mV was applied to the IA input ($\mathrm{IA_{IN}}\pm$). Note that the test signal was activated after the completion of the calibration [Step (3)] to confirm that the signal is not suppressed. Table 2 summarizes the simulated closed-loop specifications of the designed analog calibration loop, which includes the

Table 2 Simulated specifications of the calibration amplifier operating in the closed-loop configuration

Closed-Loop Voltage Gain (A_v)	25.24 dB
-3 dB Frequency ($f_{-3\mathrm{dB}}$)	2.13 kHz
Unity-Gain Frequency (f_u)	151.5 kHz
Phase Margin (PM)	52.44°
Power Consumption	0.14 mW

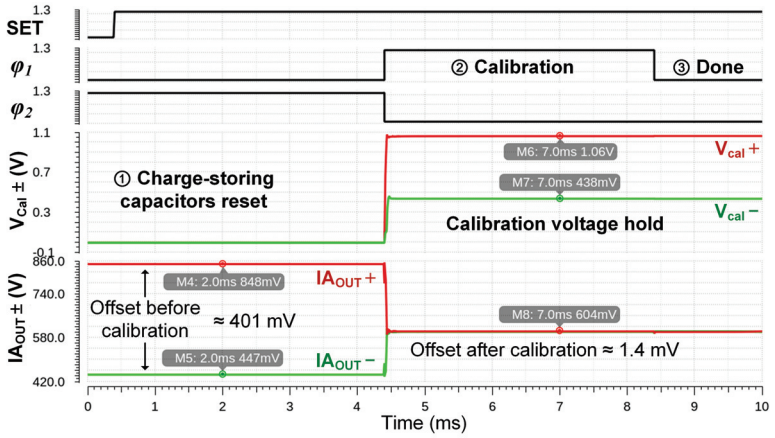


Fig. 8 Example transient offset calibration signals from one Monte Carlo simulation case.

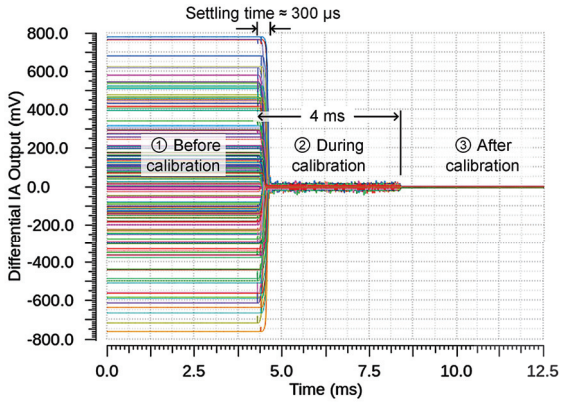


Fig. 9 Simulated transient IA outputs before, during, and after calibration (Monte Carlo simulation).

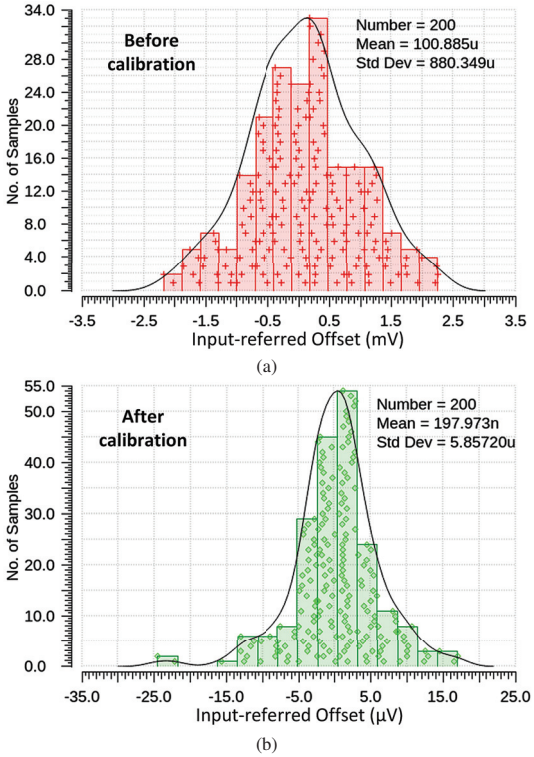


Fig. 10 Simulated input-referred offsets: (a) before calibration, (b) after calibration.

calibration amplifier, current-subtraction transistors ($M_{Cal\pm}$), and the two-stage IA with feedback resistors. Note that the calibration amplifier only consumes power during the calibration phase of approximately 4 ms).

The input-referred offset before and after the calibration can be obtained by dividing the IA output offset by the IA gain from transient simulation, which is illustrated by the histograms from Monte Carlo simulations ($N = 200$) in Fig. 10. The IA offset before calibration was captured by taking the $IA_{OUT\pm}$ difference at $t = 1$ ms [Step (1)], while the offset after calibration is taken at $t = 9$ ms [Step (3)]. As shown in Fig. 10(a), the initial input-referred IA offset is evenly distributed around $100.9\ \mu V$, with a standard deviation of $\sigma = 880.3\ \mu V$. On the other hand, the input-referred IA offset after the 3-step calibration is greatly suppressed, where the standard deviation of the Monte Carlo histogram is reduced to $5.86\ \mu V$ as annotated in Fig. 10(b).

The overall temperature sensitivity of the complete sensor was also assessed through simulations. Fig. 11(a) and Fig. 11(b) display the simulated temperature sensitivity and dynamic range of the cascaded stages shown in Fig. 1, where the impact of device mismatches and process-temperature variations are

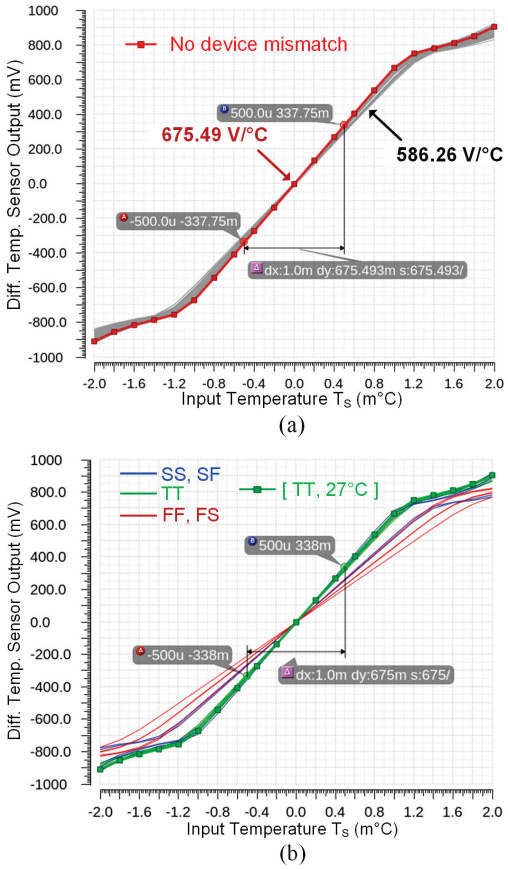


Fig. 11 Simulated differential temperature sensor input/output characteristics in the presence of (a) device mismatches (N = 50 Monte Carlo simulations), and (b) process and ambient chip temperature variations.

evaluated. Fig. 11(a) displays the simulated temperature sensitivity from 50 MC runs. The temperature sensor output without device mismatches (hence without electrical offsets in the system) is also plotted on top of the MC results, where a temperature sensitivity of $675.5\ \mathrm{V/^{\circ}C}$ can be observed over the dynamic range of $\pm 1\ \mathrm{m^{\circ}C}$. As device mismatches are introduced to the system, the overall temperature sensitivity varies between $586.3\ \mathrm{V/^{\circ}C}$ and $675.5\ \mathrm{V/^{\circ}C}$ (across 50 MC runs) with the activated chopping (shown in Fig. 1) and analog calibration. The dynamic range also varies slightly between $\pm 1.1\ \mathrm{m^{\circ}C}$ and $\pm 1\ \mathrm{m^{\circ}C}$.

The sensitivity and dynamic range of the complete temperature sensor were also evaluated under process and temperature variations. Five process corners [SS, SF, TT, FS, FF] and three typical temperature corners [$-40^{\circ}\mathrm{C}$, $27^{\circ}\mathrm{C}$, $85^{\circ}\mathrm{C}$] were tested, and the same sensitivity/dynamic range simulations were repeated over the 15 process-temperature combinations. Please note that the abovementioned temperature is the ambient chip temperature for the entire system instead of the differential temperature change due to local circuit-under-test activities monitored by the sensor circuit. Compared to the simulated sensor output under device mismatches [Fig. 11(a)], it was observed that process and ambient chip temperature variations have a more significant impact on the temperature-sensing system. The temperature sensitivity in the presence of process and temperature variations varies from $413\ \mathrm{V/^{\circ}C}$ to $688\ \mathrm{V/^{\circ}C}$, while the dynamic range varies from $\pm 1.6\ \mathrm{m^{\circ}C}$ to $\pm 1.0\ \mathrm{m^{\circ}C}$, accordingly.

5 Conclusion

An on-chip analog calibration method for differential temperature sensor offset reduction has been created. As discussed in this paper, the three-step foreground analog calibration was proposed to compensate for differential offsets within a high-gain two-stage instrumentation amplifier. The corresponding design strategy and circuit-level considerations were described together with simulation-based evaluations. An input-referred offset of $< 0.2\ \mu\mathrm{V}$ was obtained after a $300\ \mu\mathrm{s}$ settling time. Monte Carlo and process-temperature corner simulations were conducted to demonstrate the robustness of the proposed calibration technique. Only small impacts were observed for the sensitivity and dynamic range of the differential temperature sensor for on-chip thermal monitoring applications.

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