A Reconfigurable Bandpass Filter with Ferroelectric Devices for Intracardiac Electrograms Monitoring

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***Abstract*—This paper introduces a novel three-stage bandpass filter for intracardiac electrograms monitoring (IEGM), employing ferroelectric field-effect-transistor (FeFET) technology to allow bandwidth adaptation for personalized medicine. By utilizing FeFET's channel and gate stack as programmable resistor and capacitor respectively, the filter achieves precise cardiac signal isolation tailored to individual's physiological needs. Based on Globalfoundries (GF) 28 nm SLPe process that features FeFET, the design offers a broad continuous gain tuning range (22 dB to 82 dB) and bandwidth tuning range (0.1 to 25 Hz for low cut-off frequency and 10 to 120 Hz for high cut-off frequency), with an average power consumption of 393 nW, showcasing a significant stride in low-power cardiac monitoring. Moreover, input sensitivity to FeFET threshold voltage mismatch and noise characteristics are also evaluated.**

***Keywords*—Ferroelectric device, bandpass filter, adjustable gain and bandwidth, low power, biomedical circuit**

I. Introduction

The advent of personalized healthcare has brought with it the need for precise, patient-specific treatment for arrhythmias. One of these cardiac monitors is Implantable Cardioverter Defibrillators (ICDs), which offer in-time treatment (i.e., high-voltage defibrillation) for critical medical conditions (i.e., experiencing life-threatening ventricular arrhythmia) [1]. However, the utility of IEGMs sensed by ICDs is often compromised by extrinsic noise and physiological variability among individuals. Traditionally, as shown by Fig.1, addressing these challenges has involved the use of customizable signal bandpass filters, leveraging multiple capacitors and resistors to adjust gain and bandpass frequency for high-quality IEGM signals. However, this approach offers limited tunability and is constrained by the available choices for fine-tuning. An alternative method employs conventional MOSFET technology, utilizing gate voltage adjustments to fine-tune resistance values. While this allows for more precise control, it introduces additional complexity and the need for extra auxiliary analog circuits, complicating the design process. In response to these limitations, our research introduces a novel solution: a 3-stage bandpass filter that utilizes the FeFET technology. This innovation leverages the unique adjustability of FeFET to achieve ultra fine-tuning of gain and bandwidth settings, allowing for personalized tailoring of the filtering process to individual patients' cardiac signals by just adding small digital circuits for programming the FeFET. Unlike traditional MOSFET, which is characterized by a fixed threshold voltage, FeFET employs doped Hafnia (HfO_2) as the gate dielectric [2]. This enables an extensive range of threshold voltage (V_{th}) tuning due to the partial polarization feature of the material, thus providing a mechanism to tune the channel resistance (as programmable resistor with small drain voltage).

The research community has primarily focused on using FeFET as the next generation embedded non-volatile memory (NVM) for eFlash replacement (i.e., in microcontroller). Differentiated from these efforts, we will explore a new aspect of adopting FeFET in analog circuit design as tunable components. Besides the programmable channel resistance, recently, there is a work reporting that the gate capacitance of FeFET is also adjustable without static bias voltage [3].

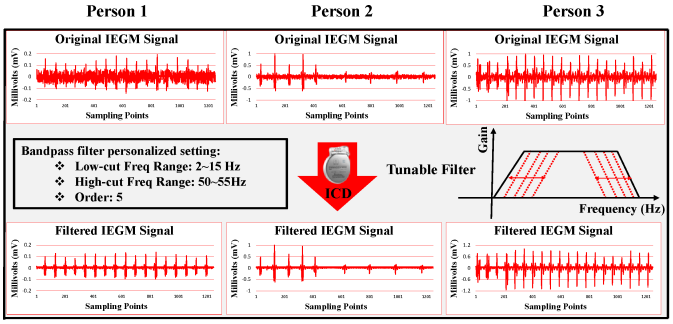

Fig. 1. The utility of IEGMs sensed by ICDs and bandpass filter requirements for tunability among individuals.

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Therefore, FeFET offers versatile reconfigurability for analog circuit design (with tunable R and C). In section II, we introduce FeFET technology, exploring its electrical properties and the methodologies employed to harness these properties for high-precision tuning, as demonstrated through experimental data and Verilog-A modeling from foundry courtesy wafers. In section III, we discuss the details of our 3-stage filter design for IEGM, including amplifier design and the capabilities for tuning gain and bandwidth at each stage. Simulation results in GF 28 nm SLPe process-design-kit (PDK) validate the proposed design.

II. Fefrroelectric Technology

A. Principle of FeFET

FeFET, which incorporates ferroelectric materials in its gate stack, has drawn significant attention in the realm of memory design due to its non-volatility, fast programming speed, and capability for multilevel operation by partial polarization [4]. These attributes suggest FeFET a potential candidate for reconfigurable analog circuit design. The core operational principle of FeFET involves modulating the dipoles within the ferroelectric layer by programming voltage pulse (e.g., +/-3 V with 100 ns). Consequently, this process alters the transistor's threshold voltage. An illustration of a Si-doped HfO_2 FeFET based on GF's 28nm SLPe process [5] is provided in Fig. 2. Through the application of varying numbers of voltage pulses as shown in Fig. 3, it attains partial polarization. This technique enables the precise adjustment of the FeFET's V_{th} values through the iterative programming-verify pulsing scheme.

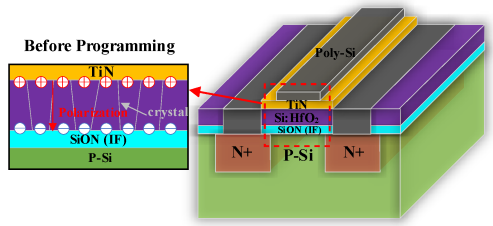


Fig. 2. Si-doped HfO_2 FeFET device structure based on GF's 28 nm SLPe process.

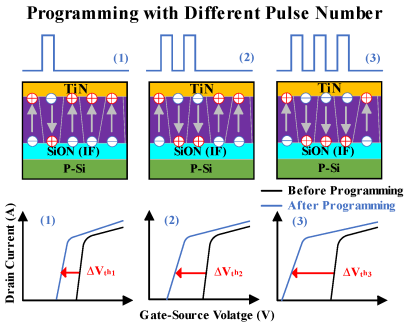


Fig. 3. Partial polarization and I-V curve adjustability by applying a different number of the fixed voltage pulse.

B. FeFET Tunning Capabilities for R and C

We have access to GF's 28 nm FeFET courtesy wafer for extensive electrical measurement. The current-voltage (I-V) curve of the FeFET, modeled by the Verilog-A model based on experimental data, is illustrated in Fig. 4. For FeFET devices with a 200 nm length, the current density can be adjusted within a wide range (5 pA/μm to 2.6 μA/μm) by altering the V_{th} value from 0.74 V to 0.23 V (at Vgs = 0.5 V). The gate capacitance-voltage (C-V) curve of the FeFET (when source/drain are connected), based on both experimental data and Verilog-A modeling, is shown in Fig. 5. This demonstrates that the FeFET capacitance density can be tuned from 0.215 fF/μm² to 10 fF/μm² (at Vgs = 0 V).

III. Three-Stage Bandpass Filter

The multi-stage filter architecture significantly enhances the adjustable range for both gain and bandwidth, a feature indispensable for monitoring the signals characteristic of intracardiac electrograms. Our design integrates a 3-stage filter employing FeFET as resistor and capacitor components within the GF's 28 nm SLPe process, as depicted in Fig. 6. The initial stage is devised as a low-pass filter, offering a fixed gain while enabling the tuning of the high cut-off frequency through bias current adjustments, thereby facilitating overall bandpass frequency modulation. Additionally, the inclusion of a FeFET resistor in this stage allows for the tuning of the low cut-off frequency, circumventing bandwidth constraints.

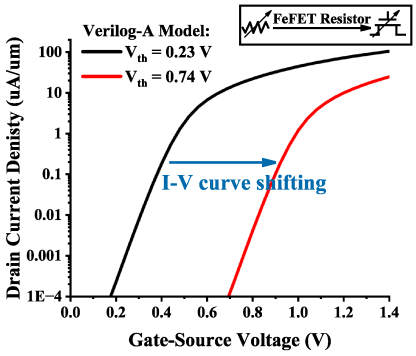


Fig. 4. I_D vs. V_{GS} curve of FeFET device based on GF's 28 nm SLPe process simulated by the Verilog-A model that is calibrated with experiments.

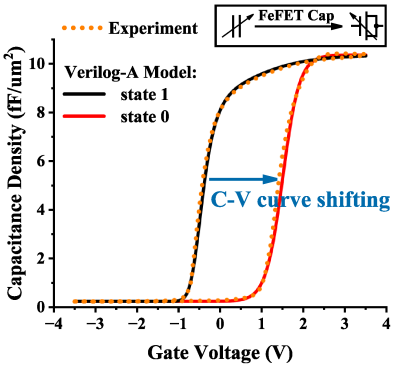


Fig. 5. C_G vs. V_{GS} curve of FeFET device based on GF's 28 nm SLPe process simulated by the Verilog-A model that is calibrated with experiments.

The subsequent stages are fashioned as high-pass filters, each offering variable gain and a tunable low cut-off frequency. Furthermore, digital pulse programming logic is employed to adjust the FeFET's V_{th} by supplying voltage pulses in alignment with digital code number settings, thus enhancing precision in gain and bandwidth control and reducing the overall area at the same time. An internal signal test selector is incorporated to facilitate the testing of outputs from the first and second filter stages, streamlining the evaluation process.

A. *Two-stage OTA Design with CMFB*

In the design of the amplifier employed at each stage, a consistent architecture consisting of a 2-stage Operational Transconductance Amplifier (OTA) devoid of non-resistor Common-Mode Feedback (CMFB) [6] is utilized. The transistor-level structure is shown in Fig. 7. We choose the PMOS of amplification work in weak inversion [7], which is instrumental in achieving ultra-low power consumption while concurrently ensuring a high gain output, thereby contributing to a significant reduction in the overall power consumption of the system. Additionally, the incorporation of the stacked MOSFET technique serves to enhance the open loop gain and diminish gain error, further refining the performance of the amplifier.

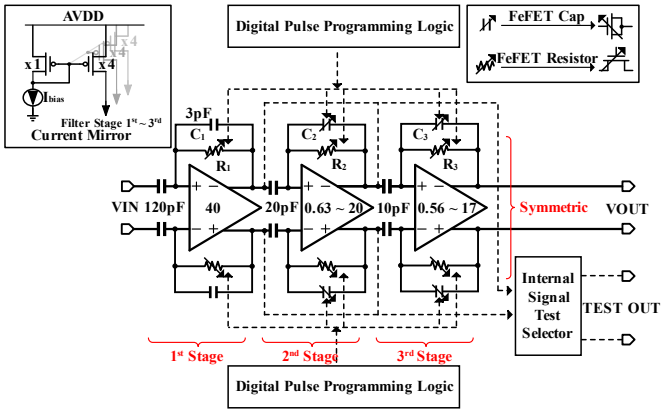


Fig. 6. 3-stage gain and bandwidth adjustable filter scheme for IEGMs.

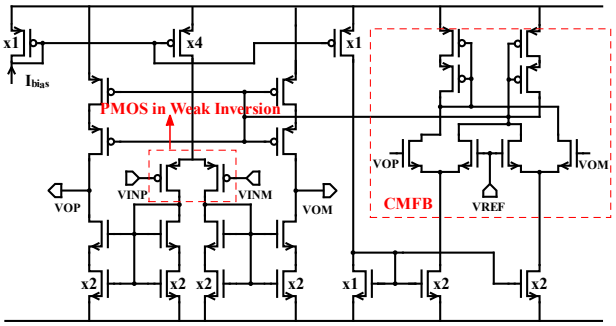


Fig. 7. 2-stage OTA with CMFB for ultra-low power.

B. *First-stage Bandpass Filter*

The first stage filter constructed by OTA and feedback RC network functions is shown in Fig. 8 (a) as a bandpass filter and configured into low-pass filter mode as shown in Fig. 8 (b). The fixed capacitors C_1 and C_{IN} provide a fixed × 40 gain for the first stage according to (1) to amplify the input signal initially, which ensures the signal intensity for the process of later stages.

$$A_V = \frac{C_{IN}}{C_1} \tag{1}$$

$$f_{-3dB\_high} = \frac{\beta \cdot Gm}{2\pi \cdot C_L} \tag{2}$$

$$f_{-3dB\_low} = \frac{1}{2\pi \cdot R_1 \cdot C_1} \tag{3}$$

The modulation of the low-pass bandwidth is achieved by varying the bias current within the range of 1nA to 15nA, thereby facilitating an adjustability range for the bandwidth from 10 Hz to 120 Hz. This adjustability is attained through the alteration of the transconductance (G_m) value, as delineated in (2). A configuration of FeFET resistors, designated as R_1, is also employed as feedback resistors in the circuit, which is to maintain a minimal low cut-off frequency, thereby ensuring that the bandwidth limitations do not impede the processing capabilities of subsequent stages, in accordance with the calculations presented in (3). Furthermore, these FeFET resistors also offer the flexibility to fine-tune the low cut-off frequency, thus optimizing the performance of the ensuing two stages for enhanced signal processing efficacy.

C. *Second and Third-Stage Filter*

The second and third stages have the same bandpass structure as shown in Fig. 9 (a), and both are configured into high-pass mode as demonstrated in Fig. 9 (b) with distinct RC parameter settings. By adjusting the V_{th} of the FeFET capacitors C_2 and C_3, the capacitance value is altered, thereby adjusting the gain in the range × 0.63 ~ 20 for the second stage and × 0.56 ~ 17 for the third stage according to (4). To resolve the limitation of the biggest capacitance values for single FeFET, multiple FeFET capacitors in parallel are introduced to increase the total capacitance value. Similarly, modifications to the V_{th} of FeFET resistor R_2 and R_3 allow for tuning resistance value, thus regulating the high-pass bandwidth for each stage from 0.1 Hz to 25 Hz based on (5).

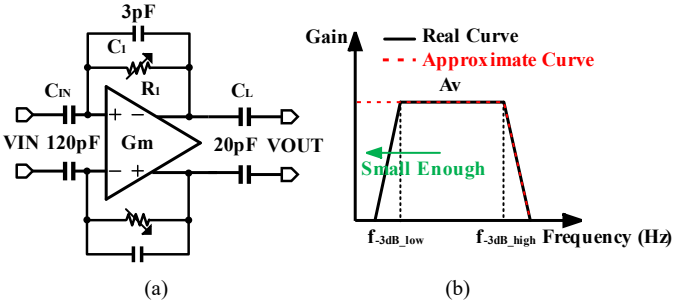
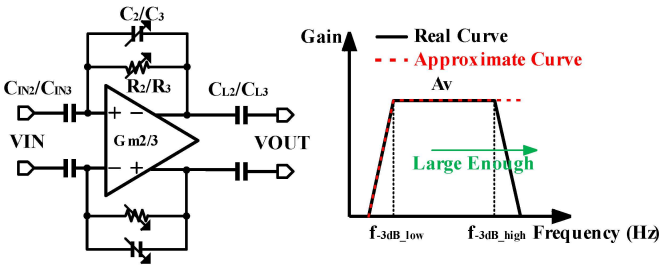


Fig. 8. (a) The first stage band-pass filter structure and (b) the gain vs. frequency curve for low-pass filter approximation.



(a) (b)

Fig. 9. (a) The second and third-stage band-pass filter structure and (b) the gain vs. frequency curve for high-pass filter approximation.

$$A_{V2} = \frac{C_{IN2}}{C_2} \quad and \quad A_{V3} = \frac{C_{IN3}}{C_3} \tag{4}$$

$$f_{-3dB\_low} = \frac{1}{2\pi \cdot R_2 \cdot C_2} \quad or \quad f_{-3dB\_low} = \frac{1}{2\pi \cdot R_3 \cdot C_3} \tag{5}$$

D. Circuit Simulation Result

The AC simulation results are shown in Fig. 10 based on Cadence Spectre simulation using GF's 28nm SLPe PDK with the calibrated FeFET Verilog-A model. In two boundary gain cases, 22dB and 82dB, by adjusting the FeFET capacitances, we pick three boundary types of configurations for each to test the adjustability. By varying the I_{bias} (1 nA ~ 15 nA), the low cut-off frequency can be tunned between around 10 Hz and 120 Hz, and by varying the Vth (0.23 V ~ 0.74 V) for FeFET R_2 in 2nd stage, the high cut-off frequency can be adjusted in around 0.1~25Hz. Overall, the circuit matrix is shown in Table I, which realizes extremely small input voltage resolution (0.07 mV), ultra-low power, good power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) performance. Finally, the sensitivity of the bandwidth vs. V_{th} is also investigated; the sensitivity value is between 0.05 Hz/mV and 0.55 Hz/mV, which means that a 4 mV average mismatch of the V_{th} value programming will cause a 1Hz variation in the tuning range.

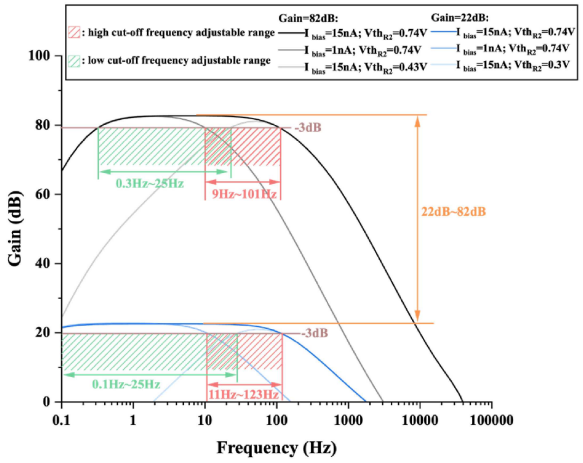


Fig. 10. Simulated gain vs. frequency in adjustable range for the 3-stage filter.

TABLE I. MAIN MATRIX FOR THE THREE-STAGE FILTER

Parameters	Simulation Results
Supply Voltage	1 V
Power Consumption (I_{bias} = 10 nA)	393 nW
Minimum Input Resolution	0.07 mV
FeFET R Tunning Range	R1/R2/R3: 87 MΩ ~998 GΩ
FeFET C Tunning Range	C2: 44.8 pF ~ 1.4 pF C3: 18 pF ~ 0.56 pF
Gain Tunning Range	22 dB ~ 82 dB
Low Cut-off Frequency Tunning Range	0.1 Hz ~ 25 Hz
High Cut-off Frequency Tunning Range	10 Hz ~ 120 Hz
CMRR (@60Hz)	237 dB (Gain = 22 dB) 246 dB (Gain = 82 dB)
PSRR (@60Hz)	-219 dB (Gain = 22 dB) -150 dB (Gain = 82 dB)
Sensitivity for Bandwidth vs. V_{th}	0.05 Hz/mV ~ 0.55 Hz/mV

IV. CONCLUSION

Our work introduced a pioneering reconfigurable 3-stage bandpass filter utilizing GF's 28nm FeFET technology for enhanced IEGM monitoring. We demonstrated the potential of FeFET for precise physiological signal filtering, with our design offering customizable gain and bandwidth adjustments. This represents a significant stride towards reconfigurable analog circuit design with ferroelectric devices.

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