Theory and Design of Pseudo-Doherty Load-Modulated Double Balanced Amplifier With Intrinsic Insensitivity to Antenna VSWR

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***Abstract*— This paper presents a novel Double-Balanced power amplifier (PA) architecture with an intrinsic load isolation. Derived from the generic load modulated balanced amplifier (LMBA), by designing the single-ended control amplifier (CA) as another balanced PA, the Pseudo-Doherty load-modulated double-balanced amplifier (PD-LMDBA) can inherit the intrinsic load-mismatch tolerance of balanced amplifier without any reconfiguration and load-impedance sensing. Theoretical analysis reveals that both the control amplifier (CA, as carrier) and primary balanced amplifier (BA, as peaking) exhibit complementary load modulation trajectories for their sub-amplifiers (CA1 and CA2, BA1 and BA2) under mismatch. This allows the PA to inherit the intrinsic load insensitivity from the generic quadrature-balanced amplifier and sustain nearly constant performance against arbitrary load variations. A prototype is implemented at 2.1 GHz, achieving 76.2% efficiency at peak power and 69.5% at 10-dB OBO with matched load. Under a 2 : 1 voltage standing wave ratio (VSWR) of load mismatch, an efficiency up to 72.5% at peak power and 64.1% at 10-dB OBO are measured. In modulated evaluation with a 20-MHz OFDM signal, the PA maintains linearity against 2 : 1 VSWR, with 2.1% of error vector magnitude (EVM) and down to −39.5 dB adjacent channel power ratio (ACPR), closely approximating the matched condition.**

***Index Terms*— Balanced amplifier, Doherty power amplifier, linearity, load mismatch, reconfigurable.**

I. Introduction

EVOLVING standards of wireless communication necessitate the adoption of modulations that support high data rates to cater to the increasing demand for faster wireless data transmission. This progression towards spectrally efficient modulations, while beneficial for data rate enhancement, introduces a challenge by significantly raising the peak-to-average power ratio (PAPR) of the transmitted signals. This increase is attributed to the combination of numerous sub-carriers and the use of complex digital modulation techniques, such as 4096QAM. To efficiently amplify these high-PAPR signals, there is a pressing need for power amplifiers (PAs) that not only operate efficiently across a wide output back-off (OBO) range but also accommodate the broader bandwidth requirements and support for multimode or multiband operations introduced by the expansion of wireless communications into higher frequencies (e.g., the 3-5 GHz range allocated for 5G). This requires PAs that can maintain efficiency over a broad OBO range and support the required bandwidth, thereby managing complexity and cost-effectiveness of the system. In response to these demands, recent developments have seen the emergence of novel PA technologies and architectures, including but not limited to, advancements in envelope tracking [1], outphasing PAs [2], [3], [4] and Doherty PA techniques [5], [6], [7], [8], as well as innovative solutions like load-modulated balanced amplifiers (LMBA) [9], [10], [11], [12], [13], [14], [15]. These advancements aim at achieving unparalleled efficiency, OBO range, and bandwidth capabilities, marking a significant stride towards meeting the high efficiency and performance targets of modern PAs.

On the other hand, massive MIMO, a cornerstone of 5G technology for increasing user capacity through spatial diversity [16], faces challenges due to the dense packing of antenna arrays, leading to a pronounced mutual coupling among the antennas. This coupling effect [17] results in a well-known complication associated with antenna scan impedance, which sees considerable variation during beam steering [18]. Studies have pointed out that this impedance mismatch in active antennas can reach a voltage standing wave ratio (VSWR) as high as 6 : 1 during the process of beam scanning [19], [20]. Such variations in the antenna's impedance directly affect the performance of power amplifiers (PAs), which serve as the immediate preceding stage to the antenna, in terms of linearity, stability, output power, and efficiency.

Various solutions have been proposed to solve load mismatch issues in PA array systems. Traditionally, placing a circulator or isolator between the PA and antenna has been a method to prevent interaction [18], [21], yet these ferrite-based devices are costly, bulky, and not suitable for integration, limiting their applications in large-scale arrays. An alternative approach involves using tunable matching networks to dynamically adjust for antenna impedance mismatches [22], [23], [24], [25]. However, these methods necessitate complex feedback control systems with sensing and execution units, adding to the system's complexity, cost, and size. A promising direction is integrating tuning capabilities directly into the PA stage,

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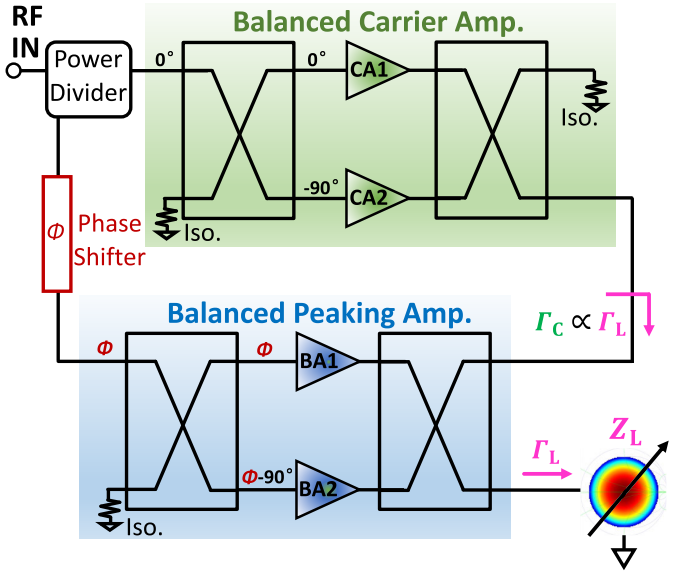

Fig. 1. Overview of single-input load-modulated double balanced amplifier with intrinsic load insensitivity.

with recent advancements in reconfigurable load-insensitive PA designs [26], [27], [28], [29], [30]. These designs utilize techniques like variable gate biasing, adaptive power splitting, and tunable phase offsets to maintain PA performance across different load conditions. Similarly, a generic multi-port load-modulation combiner [31] has been developed for better load mismatch tolerance, bandwidth, and adjustable output back-off. Additionally, innovative Doherty PAs have been designed to be insensitive to load variations by using variable DC supply voltages and multi-input phase tuning [32], [33], [34]. Overall, while these solutions offer improved performance under varying loads, they often involve complex impedance sensing and multiple parameter reconfigurations, leading to increased system complexity as well as energy and latency overhead.

To address the discussed challenges, the double-balanced amplifier emerges as a promising solution to load mismatch issues [35], [36], [37], [38]. These preliminary studies effectively demonstrated the topology's insensitivity to load mismatches. However, they lack comprehensive and detailed theoretical proof or practical validation of its effectiveness against mismatch. In this work, the following aspects are expanded upon author's previous work [38]: 1) A comprehensive analysis and theoretical derivation is unveiled for the first time revealing the intrinsic immunity of the PD-LMDBA topolgy to load mismatch without requiring reconfiguration; 2) Robust verification of the theory through circuit simulation using an emulated model; 3) Detailed practical design demonstration, specifically focusing on phase alignment using the signal path method; 4) Validation of full Front-End operation of PD-LMDBA, highlighting the seamless integration of our proposed approach. Specifically, Sec. II demonstrates a comprehensive theory of intrinsic mismatch-resilient PD-LMDBA is analytically established covering its operation in both low-power and high power load-modulation scenarios. This analysis reveals that by leveraging the balanced architecture's inherent tolerance to load mismatch for both regions, the PD-LMDBA exhibits load-modulation characteristics akin to a LMBA, while maintaining efficiency and linearity across various load conditions similar to a standard balanced amplifier. Next, in Sec. III, the theoretical derivation is effectively verified by circuit simulation using an emulated PD-LMDBA model demonstrating that the linearity profile can be well sustained versus load mismatch without any reconfiguration up to 4 : 1 VSWR. Based on the developed theory, a prototype is experimentally presented and evaluated at 2.1 GHz in Sec. IV and Sec. V, which not only exhibits the desired back-off efficiency enhancement at 50 Ω load but also achieves the desired mismatch-resilient operation under 2 : 1 VSWR. Furthermore, the measurement results using modulated signals clearly outperform the linearizability at realistic mismatched loads, which solidly demonstrate the effectiveness of proposed method and hold a promising potential for application to array-based massive MIMO systems.

II. Theoretical Analysis of PD-LMDBA With Intrinsic Load Insensitivity

The PD-LMDBA circuitry contains a primary balanced amplifier (BA) and a balanced control amplifier (CA), as shown in Fig. 1. A standard balanced amplifier can be designed over a wide bandwidth and possesses the intrinsic load insensitivity [39]. The operation of PD-LMDBA is generally divided into two regions: 1) *Low-Power region* with CA solely operating and 2) *High-Power* region with all PAs turned on. Although a brief analysis of the load-insensitive behavior within the low-power range of the PD-LMDBA is covered in [38], the load insensitivity is not fully theoretically explained in the high-power region. This section aims to theoretically illustrate that the load-insensitive property can be sustained across the full output power range of the PD-LMDBA.

A. Generalized PD-LMDBA Theory Under Arbitrary Load

PD-LMDBA can be simplified as two couplers with four transistors represented by ideal current sources as shown in Fig. 2. The load modulation behavior and the load-insensitive property of PD-LMDBA can be analyzed by leveraging the Z-matrix of the coupler and appropriately setting the boundary conditions of matrices.

The Z-matrix of BA can be expressed as

$$\begin{bmatrix} V_{b1} \\ V_{b2} \\ V_{b3} \\ V_{b4} \end{bmatrix} = Z_0 \begin{bmatrix} 0 & 0 & +j & -j\sqrt{2} \\ 0 & 0 & -j\sqrt{2} & +j \\ +j & -j\sqrt{2} & 0 & 0 \\ -j\sqrt{2} & +j & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{b1} \\ I_{b2} \\ I_{b3} \\ I_{b4} \end{bmatrix} \quad (1)$$

where $V_{b1} = -I_{b1}Z_L$, $I_{b2} = I_b$ and $I_{b4} = -jI_b$. The input RF currents from BA1 and BA2 are represented as I_b and $-jI_b$, respectively. Z_L refers to the mismatched load. Similarly, The Z-matrix of CA can be expressed as

$$\begin{bmatrix} V_{c1} \\ V_{c2} \\ V_{c3} \\ V_{c4} \end{bmatrix} = Z_0 \begin{bmatrix} 0 & 0 & +j & -j\sqrt{2} \\ 0 & 0 & -j\sqrt{2} & +j \\ +j & -j\sqrt{2} & 0 & 0 \\ -j\sqrt{2} & +j & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{c1} \\ I_{c2} \\ I_{c3} \\ I_{c4} \end{bmatrix} \quad (2)$$

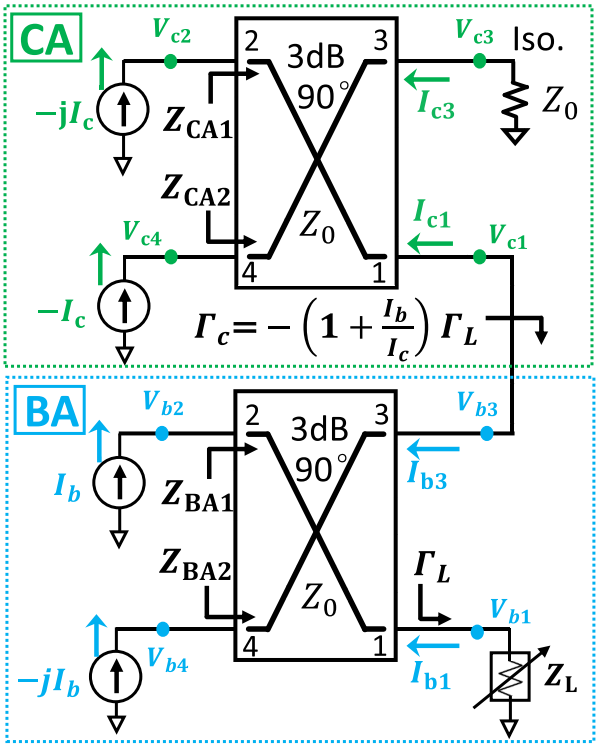

Fig. 2. Schematic of proposed PD-LMDBA with transistors represented as ideal current sources.

where $V_{c3} = -I_{c3}Z_0$, $I_{c2} = -jI_c$ and $I_{c4} = -I_c$. The input RF currents from CA1 and CA2 are represented as $-jI_c$ and $-I_c$, respectively. Since port one of the CA coupler is connected to port three of the BA coupler, the boundary condition at theses ports can be written as

$$\begin{aligned} V_{c1} &= V_{b3}, \\ I_{c1} &= -I_{b3}. \end{aligned} \tag{3}$$

In (1)-(3), we have twelve unknown voltage/current parameters and twelve equations, which include the boundary conditions at the load and the isolation port. The voltage/current parameters can be determined from these equations, allowing for the calculation of the impedance and power at each port based on the resulting voltage and current values. The load impedances of BA1, BA2, CA1 and CA2 under mismatched condition are given by:

$$Z_{\mathrm{BA1}} = Z_0[1 + 2\Gamma_{\mathrm{L}} + 2(1+\Gamma_{\mathrm{L}})\frac{I_c}{I_b}]; \tag{4}$$

$$Z_{\mathrm{BA2}} = Z_0[1 - 2\Gamma_{\mathrm{L}} + 2(1-\Gamma_{\mathrm{L}})\frac{I_c}{I_b}]; \tag{5}$$

$$Z_{\mathrm{CA1}} = Z_0[1 - 2\Gamma_{\mathrm{L}}(1+\frac{I_b}{I_c})]; \tag{6}$$

$$Z_{\mathrm{CA2}} = Z_0[1 + 2\Gamma_{\mathrm{L}}(1+\frac{I_b}{I_c})]; \tag{7}$$

The impedance observed by the CA output is given by:

$$Z_{\mathrm{c}} = \frac{V_{c1}}{-I_{c1}} = -Z_0\frac{\Gamma_L I_b + (\Gamma_L - 1)I_c}{\Gamma_L I_b + (\Gamma_L + 1)I_c}, \tag{8}$$

and Z_{c} can be rewritten as:

$$Z_{\mathrm{c}} = Z_0\frac{1-(1+\frac{I_b}{I_c})\Gamma_{\mathrm{L}}}{1+(1+\frac{I_b}{I_c})\Gamma_{\mathrm{L}}}. \tag{9}$$

Thus, the corresponding reflection coefficient at the CA output is derived as:

$$\Gamma_{\mathrm{c}} = -(1+\frac{I_b}{I_c})\Gamma_{\mathrm{L}}, \tag{10}$$

where $\Gamma_{\mathrm{L}} = (Z_{\mathrm{L}} - Z_0)/(Z_{\mathrm{L}} + Z_0)$. Note that the phase of input signals in Fig. 2 are set properly based on the ideal operation of PD-LMDBA. As a verification, for the matched case where $\Gamma_{\mathrm{L}} = 0$, the load impedances of BA and CA are simplified as:

$$Z_{\mathrm{BA}} = Z_0(1 + 2\frac{I_c}{I_b}); \tag{11}$$

$$Z_{\mathrm{CA}} = Z_0. \tag{12}$$

Eqs. (4)-(7) denote the impedance seen by each transistor, and Eqs. (8)-(10) show the impedance seen by CA output. Furthermore, the load-modulation behavior is also described by these equations under mismatched condition. It is interesting to note that for the matched case the impedance equations for PD-LMDBA are slightly different from the original equations [9]. In (11), the factor before I_c/I_b is 2 instead of $\sqrt{2}$. This is because I_c refers to the current of two sub-amplifiers in the balanced CA (see Fig. 2), while in the original formula I_c refers to the total CA current at the isolation port of the BA coupler.

B. Intrinsic Load Insensitivity of PD-LMDBA in Low-Power Region

In this region, only CA operates while BA is turned off. By plugging in $I_b = 0$ into Eqs. (6), (7) and (10), the impedances seen by CA1 and CA2 can be written as

$$Z_{\mathrm{CA1,LP}} = Z_0(1 - 2\Gamma_{\mathrm{L}}); \tag{13}$$

$$Z_{\mathrm{CA2,LP}} = Z_0(1 + 2\Gamma_{\mathrm{L}}); \tag{14}$$

where 'LP' stands for low-power region. The reflection coefficient at the CA output is given by

$$\Gamma_{\mathrm{c,LP}} = -\Gamma_{\mathrm{L}}. \tag{15}$$

By observation, the relationship between $Z_{\mathrm{CA1,LP}}$ and $Z_{\mathrm{CA2,LP}}$ are then given by

$$Z_{\mathrm{CA1,LP}} + Z_{\mathrm{CA2,LP}} = 2Z_0. \tag{16}$$

With this complementary relationship from (16), the total forward power generated by the CA transistors in the low-power region is given by:

$$\begin{aligned} P_{\mathrm{Forward,LP}} &= \frac{1}{2}\Re(Z_{\mathrm{CA1,LP}})I_{\mathrm{c}}^2 + \frac{1}{2}\Re(Z_{\mathrm{CA2,LP}})I_{\mathrm{c}}^2. \\ &= Z_0 I_{\mathrm{c}}^2 \end{aligned} \tag{17}$$

The power delivered to the load can be calculated as:

$$P_{\mathrm{L,LP}} = \frac{1}{2}\Re(-V_{\mathrm{b1,LP}}I_{\mathrm{b1,LP}}^*) = P_{\mathrm{Forward,LP}}(1 - |\Gamma_{\mathrm{L}}|^2), \tag{18}$$

and the power absorbed by the isolation port is expressed as:

$$P_{\mathrm{ISO,LP}} = \frac{1}{2}\Re(-V_{\mathrm{c3,LP}} I^{*}_{\mathrm{c3,LP}}) = P_{\mathrm{Forward,LP}}|\Gamma_{\mathrm{L}}|^2. \quad (19)$$

If the efficiency of the PA under matched case is η_0, the efficiency under mismatched condition, η_{L}, is given by:

$$\eta_{0,\mathrm{LP}} = \eta_{\mathrm{L,LP}}(1 - |\Gamma_{\mathrm{L}}|^2). \quad (20)$$

Even though the impedances seen by CA1 and CA2 are functions of the output reflection coefficient, Γ_{L}, as described by (13) and (14), they are actually complementary to each other, and the sum of them is always equal to twice the impedance under matched case as indicated by (16). This constant sum leads to a constant P_{Forward} regardless of the variation of Γ_{L}, as denoted by Eq. (17), which implies that the balanced topology creates a good isolation between the mismatched load and the PA. Note that a portion of the forward power is reflected by Z_{L}, rather than returning to the source, and is dissipated at the isolation port [40], as indicated by Eqs. (18)-(19). As a result, the impact of the reflected wave on the source is minimized. This power loss eventually leads to efficiency degradation as a function of $|\Gamma_{\mathrm{L}}|$, as denoted by (20). Furthermore, for a realistic PA, the transistor is no longer a perfect current source, and it requires an optimum impedance to generate a decent power and efficiency. Since each sub-PA still sees an impedance deviated from the designed value due to Γ_{L}, more power and efficiency degradation may be induced under higher VSWR. A constant sum of impedances can compensate for some extent of this degradation. For a PA designer, these degradation can be evaluated using power and efficiency contours from loadpull, and subsequently mitigated by properly selecting the optimum load to be somewhere between the centers of both contours. In this case, when Z_{CA1} moves toward the low efficiency/power region, Z_{CA2} is likely to move toward the high efficiency/power region, so that they can compensate for each other.

With this complementary relationship, the proposed PD-LMDBA tends to maintain its performance under various load conditions, which enhances its resilience against load mismatch. From (15), it can be seen that the BA coupler functions as an impedance inverter, resulting in the same VSWR at the CA output but with inverted impedance. This characteristic of load insensitivity exactly inherits the property found in the original balanced topology [41].

C. Intrinsic Load Insensitivity of PD-LMDBA in High-Power Load-Modulation Region

In the high-power region, CA continues its operation, while BA is turned on with BA currents rapidly escalating in response to the increased input power due to the characteristic of Class-C PA. As a result, the current ratio I_c/I_b decreases so as the impedance seen by BA, which is the load-modulation mechanism of PD-LMBA.

The impedances seen by CA1 and CA2 are described by (6) and (7) in the high-power region. Although these impedances depend on a common term, $2\Gamma_{\mathrm{L}}(1+I_b/I_c)$, the sum of them is still a constant. Similarly, we have the following relationship

$$Z_{\mathrm{CA1,HP}} + Z_{\mathrm{CA2,HP}} = 2Z_0, \quad (21)$$

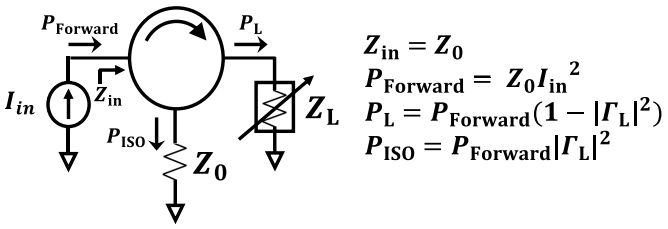

Fig. 3. PA terminated by a circulator under mismatched condition.

where 'HP' stands for high-power region. Notably, despite the increase in the reflection coefficient observed by CA due to the presence of non-zero BA current in the high-power region (as outlined in (10)), the influence of CA power becomes relatively smaller compared to that of BA power. This means the majority of the power is generated by the BA in the high-power region (e.g., the power ratio between BA and CA is roughly equal to 10:1 at peak power). Consequently, the impact of mismatch on CA is considered insignificant in this region.

Furthermore, by taking the sum of (4) and (5), the relationship between Z_{BA1} and Z_{BA2} in the high-power region is given by

$$Z_{\mathrm{BA1,HP}} + Z_{\mathrm{BA2,HP}} = 2Z_0(1 + 2\frac{I_c}{I_b}). \quad (22)$$

With this complementary relationship from (21) and (22), the total forward power generated by the CA and BA transistors is given by:

$$\begin{aligned} P_{\mathrm{Forward,HP}} &= \frac{1}{2}\Re(Z_{\mathrm{CA1,HP}})I_{\mathrm{c}}^2 + \frac{1}{2}\Re(Z_{\mathrm{CA2,HP}})I_{\mathrm{c}}^2 \\ &\quad + \frac{1}{2}\Re(Z_{\mathrm{BA1,HP}})I_{\mathrm{b}}^2 + \frac{1}{2}\Re(Z_{\mathrm{BA2,HP}})I_{\mathrm{b}}^2 \\ &= Z_0(I_{\mathrm{c}} + I_{\mathrm{b}})^2. \end{aligned} \quad (23)$$

The power delivered to the load is expressed as:

$$P_{\mathrm{L,HP}} = \frac{1}{2}\Re(-V_{\mathrm{b1,HP}} I^{*}_{\mathrm{b1,HP}}) = P_{\mathrm{Forward,HP}}(1 - |\Gamma_{\mathrm{L}}|^2), \quad (24)$$

and the power absorbed by the isolation port is expressed as:

$$P_{\mathrm{ISO,HP}} = \frac{1}{2}\Re(-V_{\mathrm{c3,HP}} I^{*}_{\mathrm{c3,HP}}) = P_{\mathrm{Forward,HP}}|\Gamma_{\mathrm{L}}|^2. \quad (25)$$

In the high-power region, η_{L} is also given by:

$$\eta_{\mathrm{L,HP}} = \eta_{0,\mathrm{HP}}(1 - |\Gamma_{\mathrm{L}}|^2). \quad (26)$$

The voltage at the load can be written as:

$$V_{\mathrm{b1}} = -\sqrt{2}Z_0(1 + \Gamma_{\mathrm{L}})(I_{\mathrm{c}} + I_{\mathrm{b}}), \quad (27)$$

Eq. (22) shows that the sum of BA impedances is still equal to a constant, twice of each BA impedance under matched case, regardless of Γ_{L}. Note that the load modulation is now involved in (22). Likewise, this constant sum leads to a load-insensitive load-modulation behavior of BA in terms of power and efficiency in the high-power region, as proved by Eqs. (23)-(26). By adopting the balanced topology in both BA and CA, the overall PD-LMDBA offers a good isolation

between the load and the PA, even though some portion of the power is still dissipated at the isolation port of the CA. Specifically, Eqs. (23)-(24) indicate that the gain and efficiency curves tend to maintain the same shape, leading to a consistent load modulation behavior. This is because the correlation between I_c and I_b is unaffected by Γ_L, and P_L is scaled down consistently over different power levels by the same factor of $(1-|\Gamma_L|^2)$. Similarly, Eq. (27) implies that the phase curve (i.e., AM-PM) of the output signal tends to maintain the same shape, since the phase at different power levels is shifted up or down by the same amount of $\angle(1+\Gamma_L)$.

To further demonstrate the load-insensitivity of the proposed architecture, we compare PD-LMDBA with a standard PA terminated by a circulator, which is widely adopted in base station applications. As depicted in Fig.3, the PA is represented as a current source, and the circulator is connected to a mismatched load Z_L. By utilizing the Y-matrix [42] or S-matrix of the circulator, the impedance and power properties can be derived. The first observation is that the PA always sees a constant impedance Z_0 for any Γ_L, and this leads to almost the same properties as PD-LMDBA, also indicated in Fig.3. In a circulator, similarly, the reflected power is routed to the isolation port, ensuring the source remains unaffected by the reflected wave. The only difference is that in PD-LMDBA although the sum of the impedances is a constant, the individual impedance of each PA is still affected by Γ_L. In summary, the proposed PD-LMDBA architecture, which does not rely on a bulky circulator, is a promising solution for maintaining PA performance against load mismatch.

III. Verification Using Emulated PD-LMDBA Model

To verify the theory of load-mismatch insensitive PD-LMDBA theory proposed in Sec. II, an ideal simulation model is emulated using two different types of bare-die GaN transistors, ideal quadrature couplers, and ideal transformers for impedance matching, as shown in Fig. 4. Specifically, peaking balance amplifier (BAs) are built with CGH60015 model from Wolfspeed, and control balance amplifier CAs are built with a smaller size model CGH60008 due to its lower output power than BA. Using the dedicated designed negative capacitance ($-C_{DS}$, $-C_{GD}$) and negative source-degeneration inductance ($-L_S$), the intrinsic parasitics of transistors are fully de-embedded. Therefore, the emulate models can well imitate ideal transistor devices as voltage-controlled current sources. The established emulation model of the entire PD-LMDBA is simulated in ADS.

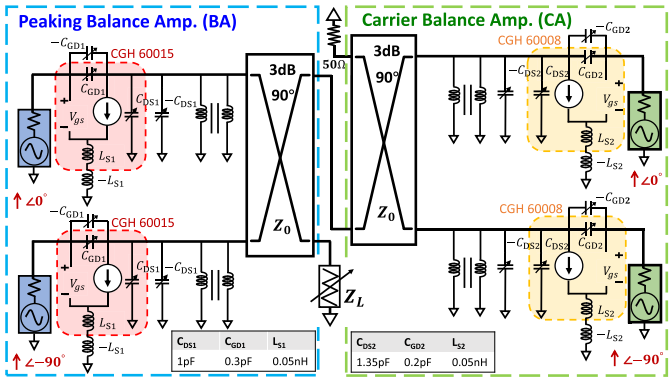

Fig. 4. Emulated model setup of the proposed PD-LMDBA with bare-die GaN transistors for verification.

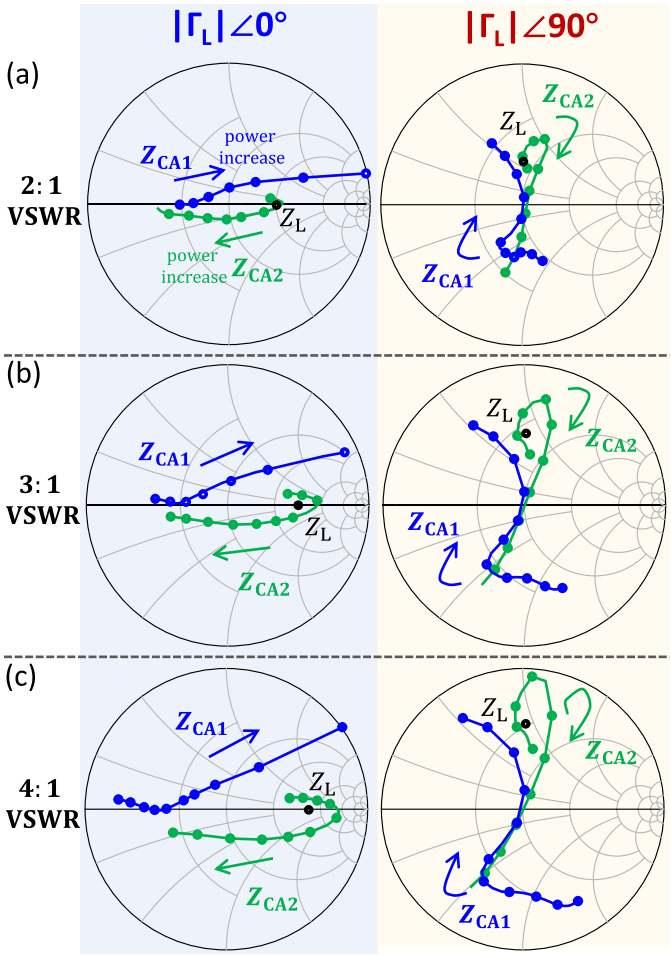

Fig. 5. Load mismatch analysis of balanced control amplifier (CAs) for representative load cases up to 4:1 VSWR. (Due to symmetry, the cases of $|\Gamma_L|\angle 180°$ and $|\Gamma_L|\angle 270°$ have similar effects on CA load with Z_{CA1} and Z_{CA2} trajectories exchanged from the cases of $|\Gamma_L|\angle 0°$ and $|\Gamma_L|\angle 90°$, respectively.)

A. Low-Power Region

The detailed analysis of load-modulation behavior of PD-LMDBA is performed and the load impedance of CAs and BAs over the entire power region can be calculated using (4)-(7). In low-power region, the balanced BA is turning off indicating that $I_b = 0$ and the impedance of BA1 and BA2 is close to open ideally. In this condition where only CA is active, the entire PA can be examined as a single balanced amplifier circuit under load-mismatch conditions. Here, the quadrature coupler acting as an inverter can be clearly proved by Fig. 5 which clearly indicates that the impedance of CA1 and CA2 always present opposing deviations from the optimum value Z_0 up to 4 : 1 VSWR, and their sum is nearly constantly equal to $2Z_0$ as expected from the theoretical relationship in (16)). Fig. 6 shows the output power and drain efficiency of CA1 and CA2 in low-power region under different load conditions. When load is mismatched, one of

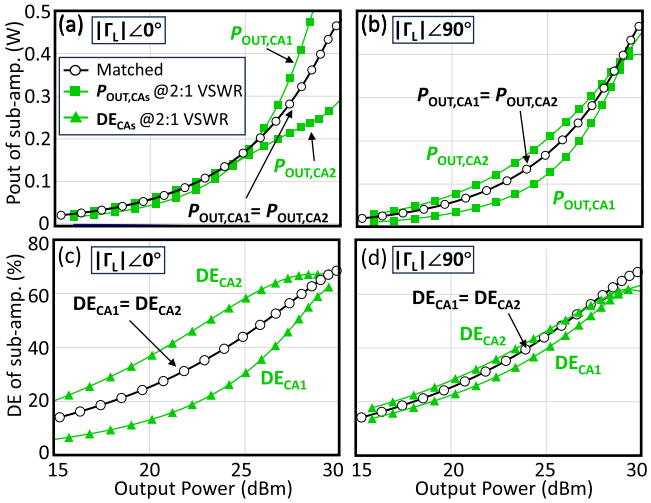

Fig. 6. P_{OUT} and DE of CA1 and CA2 in low-power region with matched and mismatched load over 2:1 VSWR. (a) $P_{OUT}@|\Gamma_L|\angle 0°$, (b) $P_{OUT}@|\Gamma_L|\angle 90°$, (c) DE@$|\Gamma_L|\angle 0°$, (d) DE@$|\Gamma_L|\angle 90°$. (The cases of $|\Gamma_L|\angle 180°$ and $|\Gamma_L|\angle 270°$ have same effects as the cases of $|\Gamma_L|\angle 0°$ and $|\Gamma_L|\angle 90°$, respectively, with $P_{OUT,CA1}$ and $P_{OUT,CA2}$, DE_{CA1} and DE_{CA2} exchanged accordingly.)

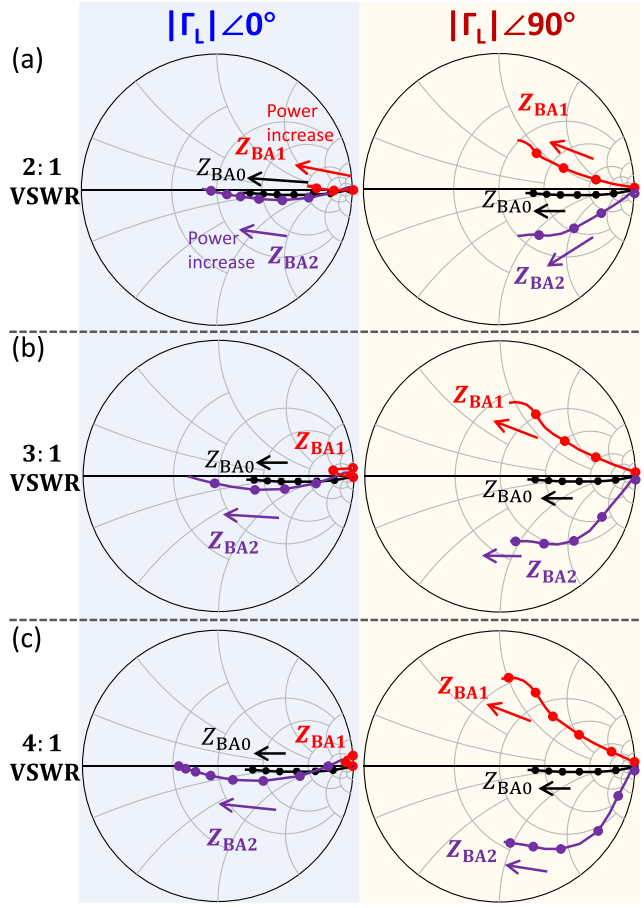

Fig. 7. Load modulation analysis of balanced peaking amplifier (BAs) for representative load mismatch cases up to 4:1 VSWR. (The cases of $|\Gamma_L|\angle 180°$ and $|\Gamma_L|\angle 270°$ have similar effects on BA load modulation with Z_{BA1} and Z_{BA2} trajectories exchanged from the cases of $|\Gamma_L|\angle 0°$ and $|\Gamma_L|\angle 90°$, respectively.)

the CAs will generate more power than the other due to their opposite load trajectories. This behavior ensures that their combined output power remains approximately equal to the

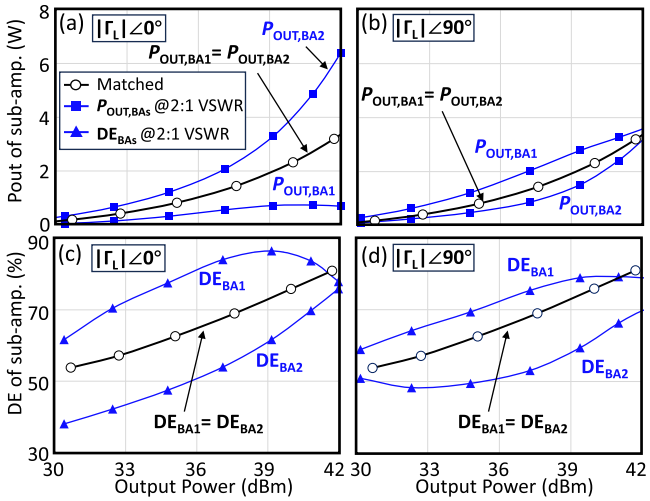

Fig. 8. P_{OUT} and DE of BA1 and BA2 in high-power region with matched and mismatched load over 2:1 VSWR. (a) $P_{OUT}@|\Gamma_L|\angle 0°$, (b) $P_{OUT}@|\Gamma_L|\angle 90°$, (c) DE@$|\Gamma_L|\angle 0°$, (d) DE@$|\Gamma_L|\angle 90°$. (The cases of $|\Gamma_L|\angle 180°$ and $|\Gamma_L|\angle 270°$ have same effects as the cases of $|\Gamma_L|\angle 0°$ and $|\Gamma_L|\angle 90°$, respectively, with $P_{OUT,BA1}$ and $P_{OUT,BA2}$, DE_{BA1} and DE_{BA2} exchanged accordingly.)

power generated in matched condition. From the perspective of drain efficiency, while the overall efficiency cannot be directly represented as the sum of the individual sub-amplifier efficiencies, Fig. 6(c) and (d) demonstrate the same complementary behavior, where one sub-amplifier achieves higher efficiency relative to the other when mismatch occurs. This also verifies the robustness of the complementary relationship derived in Sec. II-B. Consequently, the overall output performance of the PA in this region becomes substantially resilient to variations of load.

B. High-Power Load-Modulation Region

In high-power region where CA reaches its saturation, the peaking device BA starts to generate power. As the current ratio I_b/I_c in (6) and (7) increase, the impedance seen by CAs exhibits a same tendency as low-power region with opposing deviations from the optimal value of Z_0. Specifically, Fig. 5 indicates this trend as every midpoint of the line connecting Z_{CA1} and Z_{CA2} invariably falls upon the nominal impedance value, Z_0. This phenomenon not only corroborates the applicability of the derivation in Sec. II-B across the entire power region but also validates its efficacy in accommodating higher VSWR levels.

Moreover, in terms of the peaking device BA, as it starts to load modulated by CA output signal. The current ratio I_c/I_b in (4) and (5) starts to decrease from infinite value ideally, indicating a reciprocal term of the impedance of BA1 and BA2. This quantitative analysis demonstrates that the load modulation behavior of BA1 and BA2 starts from open and towards opposite direction as plotted in Fig. 7 where Z_{BA1} and Z_{BA2} are conjugate during load modulation. Additionally, the impedance of BA1 and BA2 are properly modulated with a complementary dependence of Z_{BA0}. Specifically, the nominal impedance value, Z_0 precisely located on the midpoint of the line connecting Z_{BA1} and Z_{BA2} as plotted in Fig. 7.

Additionally, Fig. 8 shows the power generated by BA1 and BA2 in the high-power region under different load conditions, where the CA power is not given as it is insignificant in this region. The result indicates that BA1 and BA2 exhibit a similar compensatory trend as the balanced CA under load mismatch. Specifically, when the mismatch load phase is 0 degrees, as shown in Fig. 8(a), BA2 dominates the combined power since BA1 sees a much larger impedance, as explained by (4), (5) and Fig. 7. Moreover, with the complementary load modulation, the whole BA generates same amount of power as the matched case, as illustrated in Fig. 8(b). Therefore, the total output power in this region can be well sustained when encountering impedance mismatches.

To further verify the load insensitivity of PD-LMDBA, Fig. 9 illustrate several emulated PA configuration under load mismatch up to 4:1 VSWR. More specifically, Fig. 9 (a) shows the original PD-LMBA's performance under mismatched condition, which is subject to a large variation for DE and linearity profiles. Next, by terminated the PD-LMBA with a ideal circulator as shown in Fig. 9 (b), the the load variations at different VSWR levels are perfectly isolated from PA. More importantly, as shown in Fig. 9 (c), the proposed PD-LMDBA shows a quasi-isolation to load very similar to the effect of circulator without having to perform any reconfiguration or relying on magnetic device. Therefore, the theory presented in Sec. II is solidly proven.

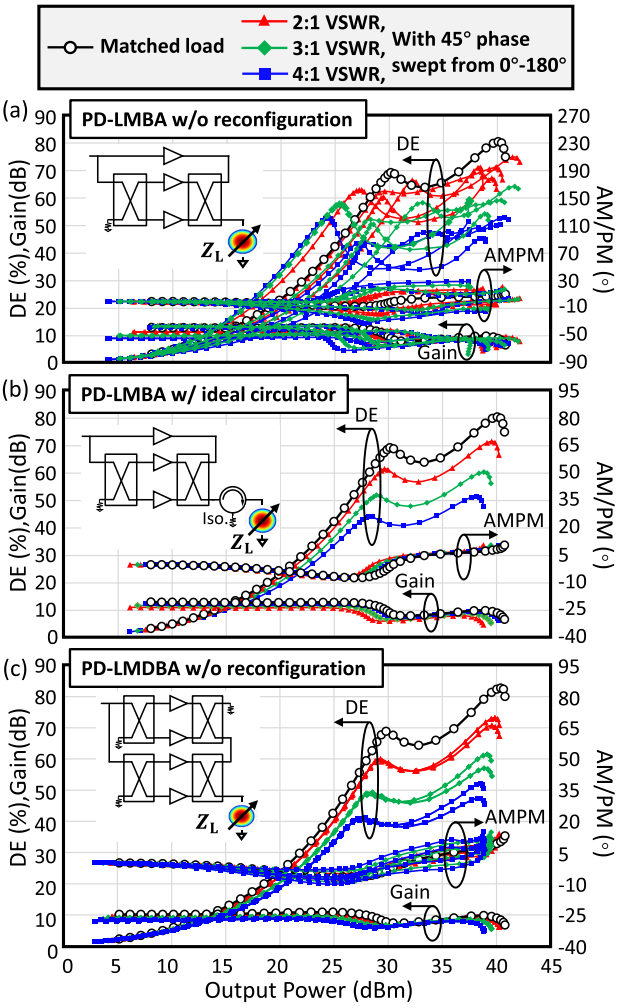

Fig. 9. Simulated performance comparison for load mismatch case up to 4:1 VSWR using different emulated model: (a) PD-LMBA without out reconfiguration. (b) PD-LMBA with ideal isolator connected between RF output and load. (3) PD-LMDBA with intrinsic load mismatch resilience.

IV. Practical Design of PD-LMDBA Prototype

A physical prototype is designed and implemented using GaN devices (CGH40006P) at 2.1 GHz to verify the proposed architecture. The realized circuit schematic with detailed values of all actual circuit element is shown in Fig. 10. Four 50-Ω single-section branch-line quadrature hybrid couplers are inserted at the input and output ends to create the CA and BA in balanced structure. In order to accommodate the high PAPR of emerging 5G signals, a back-off range of 10-dB is selected for this prototype. Both the input matching networks (IMNs) of CA and BA have been implemented using a transmission-line-based low-pass matching network, while the output matching network (OMN) is primarily established through the utilization of the coupler as a transformer and a bias line (which works as a shunt inductor) which reduce the complexity of the load-modulation control and phase dispersion.

A. Phase Alignment Design Based on Signal-Flow Analysis

Since the load modulation across the two sub-amplifiers mainly relies on the phase difference between them. The optimal phase alignment between CA and BA is required for the PD-LMDBA setup to extract the best performance in terms of efficiency and output power. This phase alignment can be qualitatively analyzed by using the signal-flow graph introduced in our previous study [43], [44]. The corresponding signal paths of BA and CA are illustrated in Fig. 11, respectively, the signal path delay of BA (in blue) starts from the input of input quadrature coupler then splits into I (in-phase signal) and Q (quadrature signal) paths. The amplifier stage includes input matching network (IMN), OMN, parasitic network and GaN device.

From the viewpoint of the CA signal, before the injection signal port, i.e, the BA isolation port, it exhibits the same phase delay which is the signal path of standard balanced PA. Then, the combined CAs signal is fed into the output coupler of BA, where it is also divided into I and Q. It's important to note that, in comparison to the BA path, the CA path experiences additional delays due to the inclusion of two extra segments, which essentially involve the signal making a round trip through the BA output network, i.e, OMN and parasitic network, as shown in Fig. 11. Thanks to the simplest design of BA's output network (the additional delay in CA path), which resonates with the parasitic network. As a result, This setup minimizes the delay caused by this network and offers a straightforward solution through the use of a 50-Ω transmission line with optimally adjusted electrical lengths at the BA's input end as illustrated in Fig. 11 [43], [45].

B. Full Front-End Operation of PD-LMDBA

The RF circulator plays a crucial role in enabling duplex communication by providing isolation between the transmit

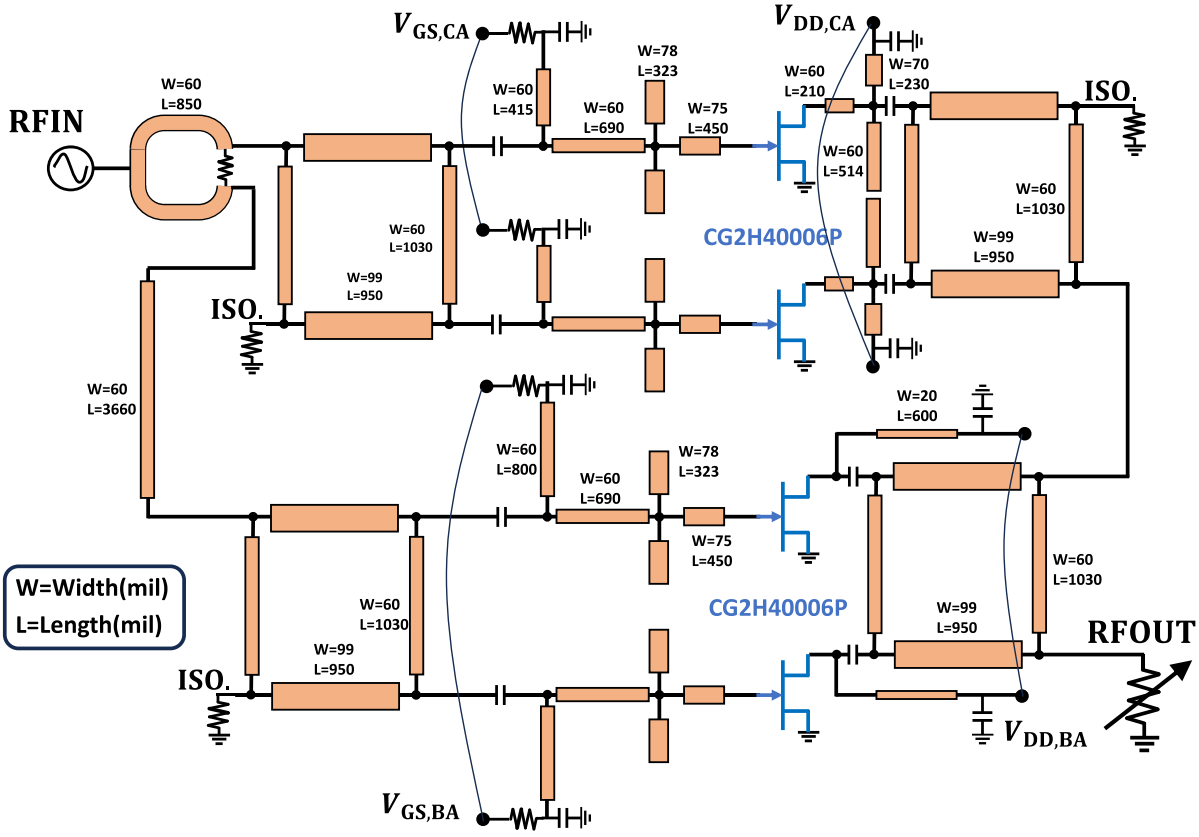

Fig. 10. Circuit schematic overview of designed PD-LMDBA.

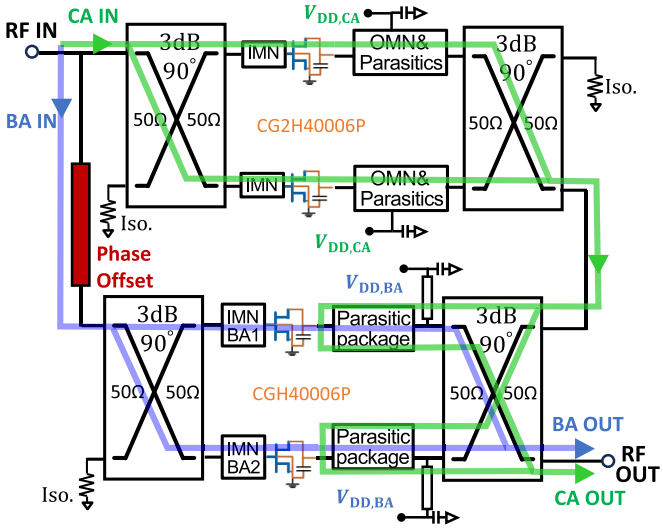

Fig. 11. Signal flow graph for the designed PD-LMDBA with circuit implementation based on GaN transistors and branch-line hybrid couplers.

(TX) and receive (RX) pathways, thereby facilitating directional routing of signals. Traditionally, these ferrite or magnetic materials based circulators are bulky, expensive, and incompatible with conventional integrated circuits. As a result, there has been significant research into non-magnetic alternatives to achieve non-reciprocity, culminating in the development of non-magnetic RF circulators.

In parallel with these developments, in our design, the structural configuration is adeptly tailored to serve as a low-loss receiver (RX) device within the RF front-end, employing a novel approach where the CA's isolation port is designated as the output port of the receiver while the input port is the load port of TX mode as depicted in Fig. 12, similar to [46]. From the perspective of the signal path, the received signal from the antenna port is first quadrature-split to reach the output of two sub-PAs of the BA then identically reflected and quadrature-combined. This signal then goes through an identical split-reflect-combine path in the CA's path and finally reaches the isolation port of CA's output coupler as the orange path plot in Fig. 12. It is important to note that, during the RX configuration of PD-LMDBA, the CA and BA transistors are turned off to ensure a sufficiently high reflection coefficient such that the RX signal can be strongly reflected and minimize the receive loss. Additionally, Fig. 12 illustrates the simulated power loss from the RX input to RX output, it can be seen that the loss at center frequency is near 0.7 dB from the BA path and at 1.35 dB for the total power loss such that this mechanism essentially allows our design to operate with equivalent circulation capability similar to a PA-circulator cascade. Such a configuration enhances the efficiency of system and simplifies the RF front-end architecture by integrating dual functionalities within a single structural setup.

C. Overall Simulation Results

With the detailed design described in this section, the overall simulated efficiency and linearity profiles versus output power is shown in Fig. 13. These results clearly indicate that under load mismatch, the first efficiency peak is maintained around 10-dB OBO, and the high efficiency is kept towards the peak

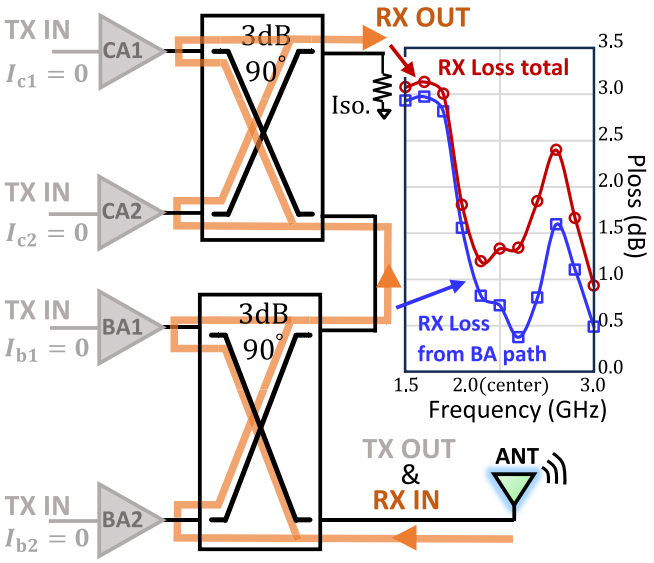

Fig. 12. Receiver (RX) operation and loss analysis of PD-LMDBA in time-division duplex (TDD) system, where PA is off during RX time-slot.

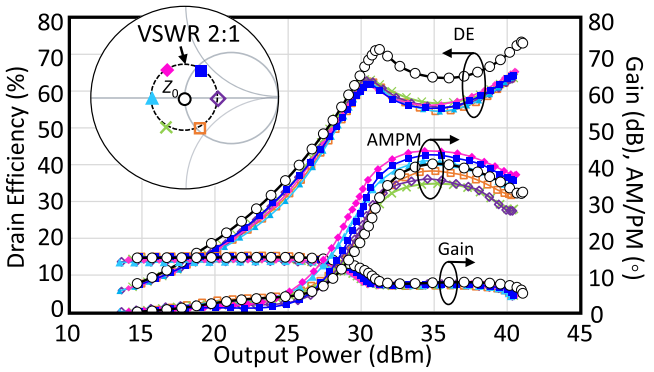

Fig. 13. Simulated efficiency and linearity profile versus P_{OUT} of designed PD-LMDBA at 2.1 GHz under different load conditions shown in Smith chart.

power while the AM/AM and AM/PM responses are sustained as well without any reconfiguration. It is demonstrated that the PA performance of the proposed PD-LMDBA is nearly independent of the load variation across 2 : 1 VSWR, which is equivalent to the cascade connection of PA and isolator.

V. Fabrication and Measurement Results

Fig. 14 shows the photograph of fabricated PD-LMDBA and the measurement system setup. The circuit is implemented on a 0.5-mm (20-mil) thick Rogers Duroid-5880 PCB board with a dielectric constant of 2.2 and the board size is 140 mm × 100 mm. A Keysight PXIe vector transceiver (VXT M9421) is used as signal generator and analyzer for CW and modulated measurement. A driver stage provides power level and a directional coupler after isolator is used to accurately sample and measure the input power. The balanced CA is biased in Class-AB mode with $V_{GS,CA}$ of −2.9 V. $V_{DD,CA}$ is set to 12 V to ensure its saturation is maintained at 10-dB power back-off. The balanced BA is biased in Class-F/F^{-1} mode with a $V_{GS,BA}$ of −5 V. The drain voltage biasing of BA, $V_{DD,BA}$, is set to 28 V to achieve its maximum output power.

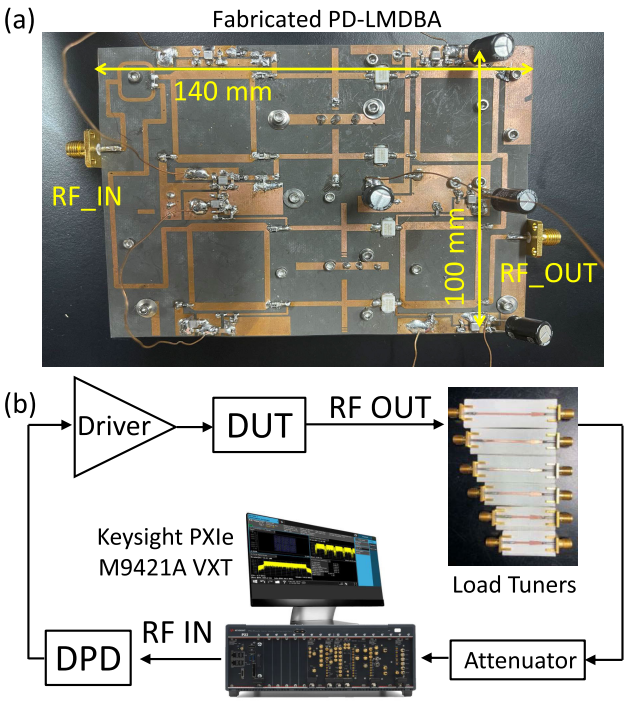

Fig. 14. (a) Fabricated PD-LMDBA prototype. (b) Modulated measurement set up. (DPD setting is unchanged for matched and mismatched load conditions.)

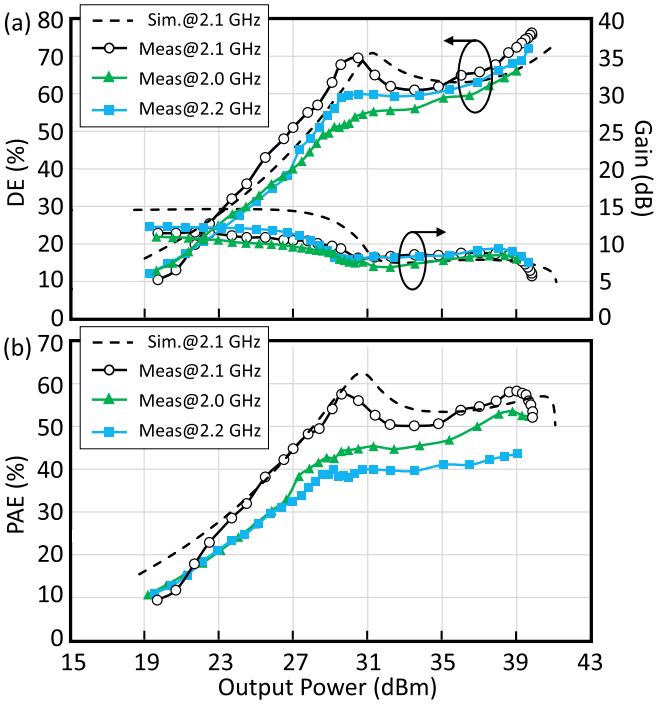

Fig. 15. Measured drain efficiency, gain and PAE with CW signal under matched condition at 2.0, 2.1 and 2.2 GHz.

A. Continuous-Wave Measurement

Under the condition of a standard matched load impedance of 50 Ω, the fabricated prototype is first measured with a single-tone continuous-wave (CW) stimulus signal. At center frequency of 2.1 GHz, the proposed circuit with an optimal CA-BA phase offset and biasing setting achieves an maximum

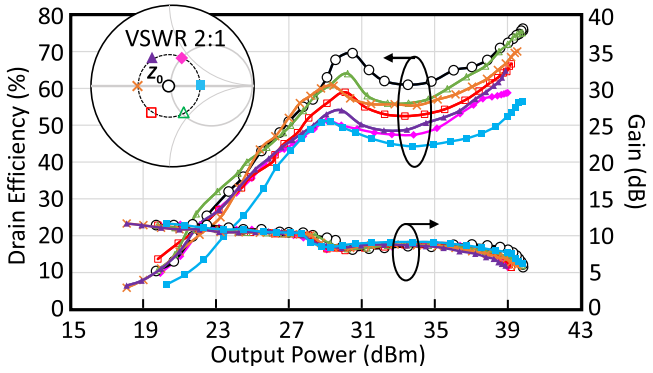

Fig. 16. Measured drain efficiency and gain with CW signal under mismatched condition at 2.1 GHz.

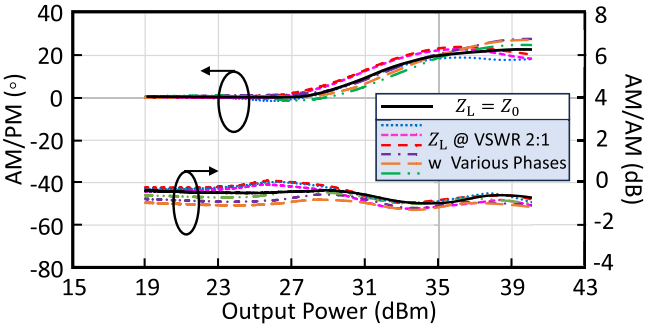

Fig. 17. Measured linearity performance using VNA under different load mismatch conditions at 2.1 GHz.

drain efficiency (DE) of 76.2% and power added efficiency (PAE) of 58.3% at saturated output power of 40.5 dBm. Additionally, a DE of 69.5% and PAE of 58.1% are measured at 10-dB OBO as shown in Fig. 15. The board is then measured within an extended bandwidth at 2.0 and 2.2 GHz as depicted in Fig. 15 as well,at peak power, the measured DE is from 65.1% to 72.1% and the PAE is from 43.6% to 53.6% at peak power. A DE from 50.8% to 59.8% and PAE from 40.1% to 45.4% are measured at 10-dB OBO. The measured gain is around 8 dB at 10 dB OBO level within the bandwidth. It is also important to note that this design can be further extended to wider bandwidth by implementing wideband quadrature coupler and multistage matching networks [47].

In order to verify the intrinsic mismatch recovery capability of PD-LMDBA, the PA output is connected to several designed impedance transformer, which covers the 2 : 1 VSWR circle on Smith Chart with the phase swept at 30° step as shown in Fig. 14(b). Fig. 16 shows the measured DE and gain versus swept output power at various loads across the 2 : 1 VSWR circle at 2.1 GHz. A DE up to 72.5% is measured at peak power of 40.1 dBm under various load mismatch conditions, and the measured DE at 10-dB OBO is up to 64.1%. It is clearly seen that the efficiency profiles under load mismatch well replicate the shape at matched condition. The mismatch measurement is then extended by using VNA at the same frequencies for extracting the dynamic linearity response. Fig. 17 shows the measured linearity performance with a comparison between matched load and various mismatched load conditions. It is clearly demonstrated that both the AM/AM and AM/PM profile can be well maintained against 2 : 1 VSWR without any reconfiguration which robustly validate the proposed theory.

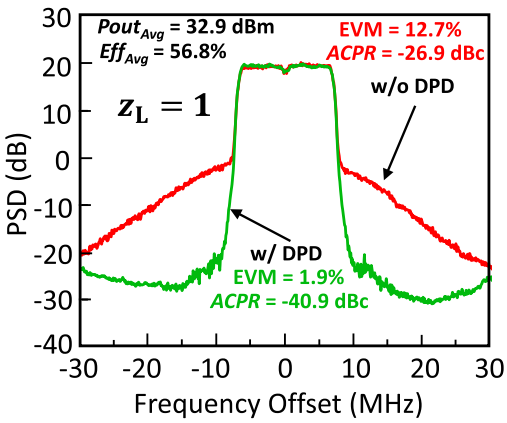

Fig. 18. Modulation signal measurement result at 2.1 GHz under matched condition.

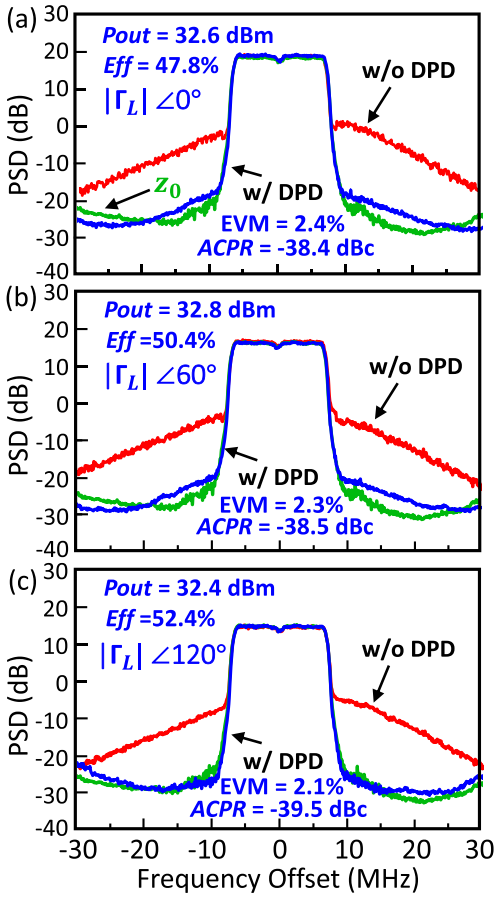

Fig. 19. Modulation signal measurement result comparison between match and mismatch load at 2.1 GHz: (a) $|\Gamma_L| \angle 0°$, (b) $|\Gamma_L| \angle 60°$, (c) $|\Gamma_L| \angle 120°$.

B. Modulated Measurement

In order to validate the linearity of the proposed circuit under realistic communication condition, the modulated measurement is presented with a 20 MHz modulation-bandwidth and 11.5 PAPR single-carrier 64 QAM LTE signal at 2.1 GHz. The measurement first performed under matched condition.

TABLE I
COMPARISON WITH STATE-OF-THE-ART OF RECENTLY REPORTED MISMATCH-RESILIENT PAS

Ref./ Year	This Work		[30] TMTT-2024		[32] TCAS-2023		[28] TMTT-2021		[34] TMTT-2021		[33] TMTT-2022	
Technology	GaN-PCB		GaN-PCB		GaN-PCB		GaN-PCB*		LDMOS-PCB		GaN-PCB*	
Freq (GHz)	2.1		2.0		2.4		3.5		0.9		3.6	
Reconfiguration against VSWR	Intrinsic mismatch-resilient (No reconfiguration needed)		2-D		3-D		3-D		2-D		4-D	
Load (Z_0/VSWR)	50 Ω (2GHz-2.2GHz)	2:1	50 Ω	2:1	50 Ω	2:1	50 Ω	2:1	50 Ω	2:1	50 Ω	2:1
P_{Max} (dBm)	39.4-40.5	39.1-40.2	46.4/46.7	44.8/46.3	43.4-43.7	41.5-43.3	42*		29.4	29.4	43.5	42
DE_{Max}/PAE_{MAX} (%)	65.1-76.2 /43.6-58.3	57.9-72.5	70.3/72.2	50.2/65.8	69.1-70.8 / -	52.8-60.7 / -	63.5-70.1 / -	-	59.1 /56.2	46.5-51.3 /44.1-58.3	64* / -	58 / -
DE/PAE @10dB OBO(%)	50.8-69.5 /40.1-58.1	51.4-64.1	25* / -	40*-55* / -	25*-42* / -	10*-42* / -	34*-36* / -		25* /-	18*- 30*/ -	32* / -	27*- 35* / -
Modulation Signal	64-QAM 20 MHz		64-QAM 80 MHz		-		64-QAM 20 MHz		64-QAM 3.86 MHz		LTE 5 MHZ	
$P_{OUT,avg}$ (dBm) / DE_{avg} (%)	30.9-31.5 /56.4-62.0	29.8-30.6 /47.8-52.4	37.6 /51.7-53.2	36.5-37.3 /45.7-52.2	-		37.2/ 47.3	33-34.2/ 32.5-42.5	22 /24.4	22 / 21-23	43.5 /46.4	42* /43
ACPR(dBc)	-40.9†	< -38.4†	< -46.1†	< -45†	-		-41#	-	< -48†	< -45†	-31.8#	<-28.8#

* Graphically estimated, † with DPD, # without DPD

Fig. 18 shows the the measured power spectral density (PSD) under matched conditions, where an adjacent channel power ratio (ACPR) of −26.9 dBc is measured originally, and a −40.9 dBc is achieved after applying DPD. To further validate the load isolation of the PD-LMDBA architecture, we only changed the load condition to 2 : 1 VSWR ($|\Gamma_L| = 1/3$ with different phases) without updating the DPD model. It is found that the linearity performance of down to −39.5 of ACPR can be well maintained against various load conditions as shown in Fig. 19, together with up to 52.4% of average efficiency that is also very close to the matched condition.

The PD-LMDBA is intrinsically non-linear due to the over-driving of CA, which leads to the high ACPR. There are multiple ways to mitigate this CA over-driving issue, such as digital-assisted dual-input design [48] and equipping CA with load modulation through asymmetrical biasing of BA [45], [49]. Moreover, DPD has been successfully applied to LMBA in literature. Together with the recent advances in load-mismatch tolerable DPD [50] and array-level DPD [51], [52], [53], the presented PD-LMDBA can be effectively linearized in both matched and mismatched conditions which leads to a further research topic of enhancing the performance of PD-LMDBA.

Table I presents a comparison between this design and other recently published active-load-modulation PAs with mismatch-resilient reconfigurations. It is important to emphasize that the proposed PD-LMDBA exhibits the first ever intrinsic mismatch insensitivity while offering a very competitive profile in terms of the DE efficiency, back off range and operation simplicity. More important is that under mismatched condition, our design demonstrate an overall higher efficiency and linearity profile without any reconfiguration, which robustly verifies the effectiveness of the proposed theory.

VI. CONCLUSION

This paper introduces a novel PD-LMDBA architecture, demonstrating a remarkable capability for quasi-isolation to varying load conditions. Through comprehensive theoretical analysis, it has been established that this topology not only preserves the advantageous load modulation characteristics inherent to traditional LMBA systems but also incorporates the intrinsic mismatch tolerance synonymous with classic balanced amplifiers. The proposed theory is first verified through emulated model, proving that both the control and peaking balance amplifiers inherit the load insensitivity behavior from balanced architecture and also present a complimentary load modulation mechanism that ensures a constant overall performance. A prototype is then realized at 2.1 GHz to experimentally validate the theory. It achieves peak DE of 76.2% and 69.5% at 10-dB OBO under matched load. When loading with 2 : 1 VSWR mismatch, the DE can be maintained up to 72.5% at peak power and 64.1% at 10-dB OBO. When processing an OFDM signal with 11.5 dB PAPR, a high ACPR of −42-dB with DPD is measured. Notably, this high linearity is sustained even under 2 : 1 VSWR load mismatch, utilizing the same DPD model parameters as in the matched condition. The significance of these findings extends beyond the immediate performance enhancements and offers a promising solution to the persistent challenges of scan-impedance issues and main-beam distortion in array-based massive MIMO systems. By addressing these critical obstacles, the proposed PD-LMDBA paves the way for more energy-efficient and spectrum-efficient wireless communications. This breakthrough has the potential to revolutionize the design and operation of future wireless communication systems.

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