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Highly Power Dense DC to Three-Phase AC Modular Converters with Tiny Module Capacitors

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by

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Abstract

A Modular Multilevel Converter (MMC) is an attractive candidate in high power conversion due to its modularity and scalability. The energy storage element, namely the module capacitance in the MMC submodule circuit, is typically large and when scaled to convert high power, requires very bulky module capacitors. In addition to deteriorating the power density, the design necessitates the use of electrolytic capacitors, which further affects the overall converter efficiency and reliability. This research presents an MMC submodule topology and the accompanying modulation approach that reduces the submodule capacitance requirements significantly compared to conventional MMC topology (few micro-farads versus several milli-farads). This can permit the use of *only* film capacitors thus improving overall converter reliability. This thesis explores the analytical models of the approach along with a comparative study. The work is verified using circuit simulations and a laboratory-scale experimental prototype.

Dedication

Dedicated to my parents, who continue to inspire me through their actions.

Acknowledgements

Words cannot express my deepest gratitude to my advisor and chair of my thesis committee, Dr. Mahima Gupta, for her invaluable patience and immense support. Her knowledge and guidance helped me gain a deeper understanding of research and grow at the professional and personal levels. Thank you for providing me with the opportunity to be part of the Power Electronics team.

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I would like to acknowledge my husband, Ethan Lew, for his support and technical

insights that helped me better understand engineering. I would be remiss in not mentioning my American host family, Bob and Sue Young, for their sponsorship with my education.

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Acronyms

ESS Energy Storage System

FBSM Full-Bridge Submodule

FPGA Field Programmable Gate Array

HBSM Half-Bridge Submodule

HVDC High Voltage Direct Current

KCL Kirchoff's Current Law

KVL Kirchoff's Voltage Law

LUT Lookup Table

MMC Modular Multilevel Converter

MVDC Medium Voltage Direct Current

PCB Printed Circuit Board

PLECS Piecewise Linear Electrical Circuit Simulation

PWM Pulse Width Modulation

RB-IGBT Reverse-Blocking Insulated Gate Bipolar Transistor

SPDT Single Pole Double Throw

SPWM Sine Pulse Width Modulation

ZPUC Z Packed U-Cell

1 Introduction

1.1 Problem Statement

MMC is a popular converter choice in various applications including integration of renewable energy systems such as photovoltaics and wind farms, HVDC systems, energy storage systems, high power industrial motor drives and so on. Its popularity in such applications can be attributed to its modularity and scalability. Additionally, an MMC design is not limited to one power conversion type and can be used for DC/DC, DC/AC, AC/AC and AC/DC power conversions. Various research efforts have been conducted to improve MMC performance. Recent reviews of these efforts discussing challenges in MMC and different topologies proposed are detailed in [1]-[2].

Fundamental design challenge in conventional MMC module topology include large capacitor size requirement in each module, which is imposed *by design*. High power conversion requires larger module capacitor size, which limits the capacitor type that is applicable for such application. An electrolytic capacitor is commonly used to meet the high capacitance value requirement due to its physical design that allows for a range of high capacitance values. However, an electrolytic capacitor is less realiable compare to other

capacitor types such as thin film and ceramic capacitors, which typically have smaller range of capacitance values. Sudden voltage change can easily damage electrolytic capacitors and cause fire [3]. In fact, capacitors are considered to be the least reliable component in a power electronic conversion system [4] and become the first component to fail, affecting the overall converter performance. In this research work, a new module topology is proposed that is capable of significantly reduced module capacitance requirements, permitting the use of a more reliable capacitor technology such as thin film capacitor that is less bulky compare to electrolytic capacitance. The reduction in capacitor size leads to higher power density of the modular power converter and improved reliability.

1.2 Objectives of Work

The motivation of this work is to reduce a module capacitance requirements by understanding and analyzing the fundamental cause leading to the large capacitor requirement in conventional modular power converter topologies. The objectives of this work include:

- An integrated module design analysis and development as a new proposed design, addressing fundamental disadvantages of conventional modules.
- Analysis of proposed module and its characteristics that permits significantly smaller module capacitance requirements.
- Design of a modulation approach suitable for proposed module.

- Design verification through simulation and experimental work along with comparative analysis.

2 Literature Review

The modular power converter was first introduced in 2001 and has been gaining traction in various applications ever since [1]. This is due to several advantages that modular power converters provide, including:

- Its structure permits connection between multiple submodule circuits – *modularity*. This conventional structure and its characteristics are discussed in the next chapter.
- Flexibility of module design based on specific applications; the structure of an MMC is used as a blueprint for various submodule circuits based on design needs. Examples of submodule circuits include half-bridge, full-bridge, clamp double, three-level flying capacitor, five-level cross connected [2],[5].
- Ability to scale based on power conversion needs using desired type of submodule circuit. This includes hybrid modular power converters [6],[7],[8].
- Modulation for MMC also allows for high frequency modulation approaches applicable for any number of submodules [2].
- Some MMC designs provide DC fault-blocking capability [6],[9],[10].

Different types of MMC configurations with specific benefits are discussed with details in [2].

Applications of MMC are numerous due to its flexibility, permitting designs based on specific needs. A summary table of different MMC topologies, their specific applications and features are provided in [1]. Some examples of MMC applications are:

- Energy Storage System (ESS) [11].
- High Voltage Direct Current (HVDC) applications [12],[13],[14].
- Medium Voltage Direct Current (MVDC) applications [15].
- Variable speed motor drives [16].
- Photovoltaic systems [17].
- Synchronous static compensators [8].

The flexibility and scalability of MMCs for industrial and commercial applications, such as high power conversion and renewable energy integration, continue to encourage improvements in MMC designs. However, one of the challenges conventional MMC design presents is the large energy storage element requirements, namely in the *submodule capacitors*, which affect the converter power density potential due to the capacitor size and volume. In this thesis work, an analysis behind the large capacitor requirements in conventional submodule is provided.

2.1 Bulky Capacitors in Modular Power Converter

Modular power converters require a capacitor in each submodule, called a *submodule capacitor*. The submodule capacitor is placed in parallel with an SPDT switch, allowing power transfer division between submodules. A high power conversion need would require a high number of modules. Submodule capacitor size is a function of its *ripple current*. Conventional MMC module designs impose a high single-phase low-frequency AC current ripple, resulting a high ripple voltage and an increased capacitance requirements. Electrolytic capacitors are typically used because they provide a large range of capacitance values. However, it is known that electrolytic capacitors have lower reliability, due to their physical structure, compared to other types of capacitors such as ceramic or film capacitors. Thus, the use of electrolytic capacitors in modular power converter deteriorates the overall reliability of the converter, affecting performance and efficiency.

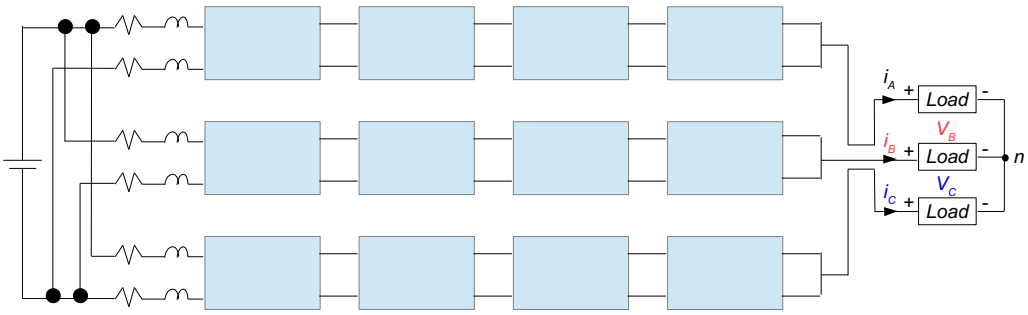
2.2 Proposed Solutions to Large Capacitor requirements

Numerous research efforts have focused on finding solutions to reduce submodule capacitor voltage ripple leading to better commercially-available capacitor options. In summary, capacitor size reduction increases power density of modular power converters, improves reliability, performance, efficiency and the overall life cycle. In this section, two types of research to reducing capacitor size requirements are discussed; topology-focused and

control-focused.

2.2.1 Topology Designs

Conventional MMC module topology for a DC-to-three-phase AC conversion consists of three arms in positive and negative sides of the converter where each arm is populated by a desired number of submodules. A single-arm MMC design is proposed in [18] to reduce the total capacitance requirements in the modular power converter. The authors conducted simulations and experiment for design verification. For a DC to three-phase AC conversion, a prototype was tested at 400 V_{DC} input voltage with four submodules in each phase, using a $1.2\ mF$ submodule capacitance and 2% capacitor voltage ripple with switching frequency of 2 kHz. A high level diagram of this proposed design is shown in Figure 2.1.



[18]

Figure 2.1: A block diagram of the single-arm MMC design proposed with the objective of reducing total capacitance in each submodule.

A hybrid MMC design, shown in Figure 2.2, consists of a Full-Bridge Submodule (FBSM) and a Half-Bridge Submodule (HBSM). This design is optimized, in addition to optimizing the control strategy, reducing the capacitance requirements by up to 38% in

[19] compared to a conventional hybrid MMC. Experimental parameters include 300 V_{DC} dc-link voltage and 2 mF submodule capacitance, operating at 4 kHz switching frequency.

A bidirectional modular three-phase AC/AC power converter configuration applicable for high voltage and high current applications is proposed in [20]. The authors used film capacitor, which improved power density and reliability of the converter. The authors proposed the used of *power cells* using three-phase AC/AC converters with a small capacitor with unidirectional and bidirectional capabilities. Simulation of 10 kW power, 500 V_{AC} input and 230 V_{AC} output using two power cells resulted in the use of 0.2 μF capacitance on the primary and secondary sides. As highlighted earlier, modular power converters can be designed for specific applications, such as this research work. Although the work in [20] results in a very small capacitance value, it is achieved by using AC/AC converters as power cells for higher AC/AC power conversion need. The focus of this thesis work is high power of DC to three-phase AC conversion need.

A topology configuration called ZPUC is proposed as a new type of modular power converter in [21]. The ZPUC topology uses six switches and three capacitors, as shown in Figure 2.3. The topology can be used for rectifier of inverter applications. Simulations and experiments were conducted for a stand-alone mode; DC to three phase AC converter with one ZPUC in each positive and negative arms (six total arms for a three-phase system). The parameters include 100 V_{DC} input, 1 kHz switching frequency, and 2 mF capacitance for all three capacitors in each ZPUC.

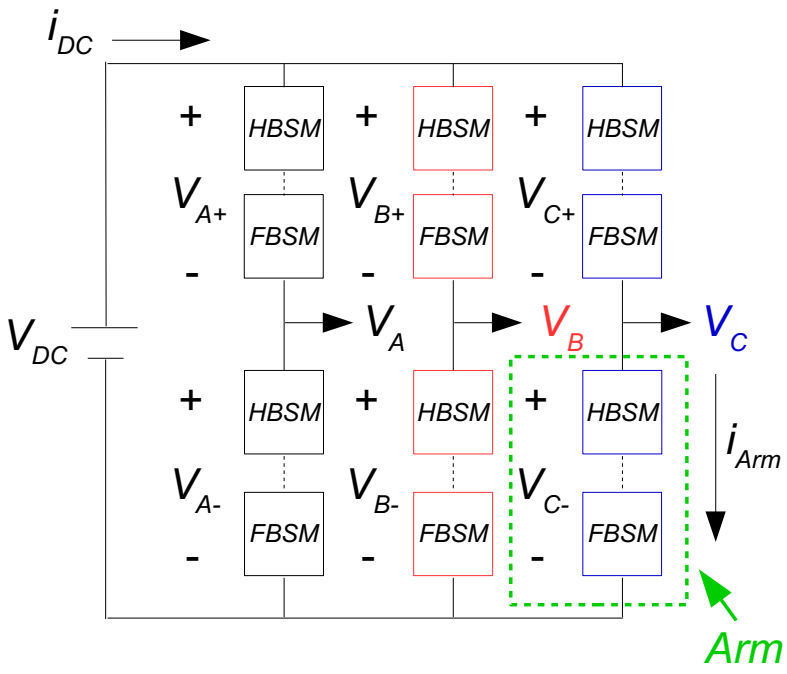
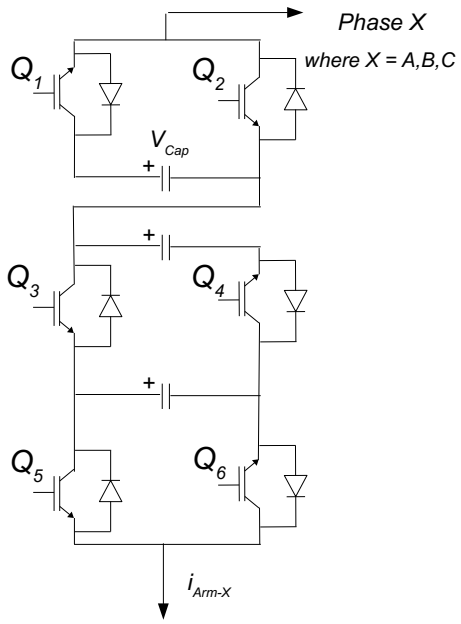


Figure 2.2: A hybrid modular power converter uses full-bridge and half-bridge submodules.

2.2.2 Control Approaches

Another approach to reduce submodule capacitance in modular power converters focuses on the control strategy. A review of different control strategies to reduce capacitance size by reducing low frequency voltage ripple is discussed in [22]. The authors focus on DC to three-phase AC MMC with five-level (five submodules in each arm). The finding concludes that adding a shared capacitor in the top and bottom submodules, in addition to injecting second order harmonic current to the circulating current, provides the highest reduction in submodule capacitor voltage ripple, which is a smaller capacitance requirement.

Second harmonic current injection is also used in [23], with an adjustable control strategy.



[21]

Figure 2.3: The ZPUC topology used in to form a new modular MMC. For a DC to three-phase AC modular power converter, one ZPUC can be used as a submodule.

The experiments used 320 V_{DC} input voltage, eight submodules per arm, 2 kHz switching frequency, which resulted in $8.3\ mF$ minimum capacitance requirement. A 20.3% reduction in capacitance value of $6.6\ mF$ was accomplished with the proposed adaptive circulating current injection.

Second harmonic circulating current injection is widely used as a control strategy to reduce capacitor voltage ripple and power loss in different MMC applications. A reduction of submodule capacitance by 40% is achieved in [24] in a DC wind turbine application. Some efforts focus on optimizing the circulating current injection method. In [25], a modulation index, m, is adjusted to an optimal value of $m = 1.155$ and compared with an FBSM-MMC

without circulating current injection where $m = 1$, resulting in reduced total capacitance by 17%.

Other control strategies focus on injecting third harmonic voltage to reduce FBSM voltage second harmonics components, providing 16% energy storage reduction [26]. Combining circulating current injection with specific modulation index of 1.414 while boosting the AC voltage, reduced capacitance by 34% to $6.56\ mF$ for a system with 12kW power and 440 V_{DC} input-voltage in [27]. A combination of modulation ratio adjustment, circulating current injection and third harmonic voltage injection reduced the capacitor voltage ripple by 80% in [28] with under 0.9 to 1 power factor. A modified MMC with reduced voltage ripple by 12.2% uses a sorting algorithm in the control strategy to determine when the largest capacitance components are required [29]. A topology proposed in [30] uses a Reverse-Blocking Insulated Gate Bipolar Transistor (RB-IGBT) combined with optimization of the amplitude of the second-order and fourth-order harmonic currents when applying third-order harmonic voltage injection, reducing capacitance by 37%.

2.2.3 Summary

Research efforts in reducing capacitance requirements typically propose modified module circuits or MMC configuration, adjusted control strategies, or a combination of both. Past studies have made good progress, resulting in a minimum in the *milli-farads* range of capacitance values and reduction by 20% to 40% in some cases. The goal of this thesis

is to reduce capacitance value to a minimum of *micro-farads* for high power application such as HVDC to three-phase AC conversion. The focus is to analyze a new module circuit design that is capable of reducing the size of capacitance requirements to *micro-farads* in high power conversion requirements, eliminating the need for electrolytic capacitors. The concept behind the new design is discussed in details in the next chapter.

3 DC to Three Phase Converter Design Methodology

The design methodology consists of multiple steps leading to the proposed design. Analytical work on classical DC-to-three-phase AC converter and conventional MMC topology has been done to understand their limitations. The main contribution of this thesis work is analyzing, designing, and verifying a new circuit topology that can be used for high power conversion in a form of an MMC. It is necessary to discuss topics that are building blocks that lead to a step-by-step process in designing a new topology. The topics in this chapter include:

- Half-bridge converter configuration in which the voltage and current analysis are applicable to the proposed design.
- Conventional module topology characteristics and its limitations.
- Capacitor sizing of a conventional module, its capacitor voltage and current, and why they matter in this thesis work.
- Classical DC-to-three-phase AC converter and the circuit limitations in regards to MMC application.

- Proposed integrated module topology and its characteristics.
- Capacitor sizing of an integrated module and the reasons for reduction in size.

3.1 Modular Configuration

A half-bridge configuration can be used for DC/DC and DC/AC power conversion. A simplified block diagram of a modular power converter is shown in Figure 3.1. Say $X = [A, B, C]$ to reflect each phase, where V_{X+} is the voltage across positive arm_X, and V_{X-} is the voltage across negative arm_X. The points of connection of the positive and negative arms interface to the three AC phase outputs.

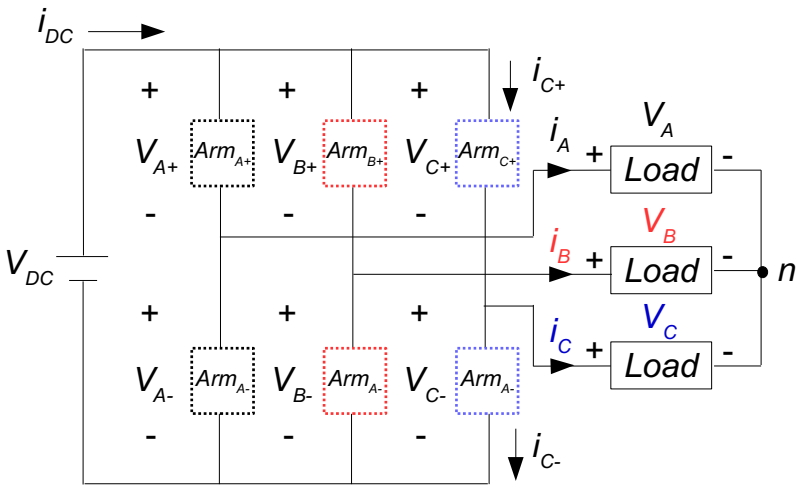


Figure 3.1: A simplified block diagram showing three independent positive (top) and three negative (bottom) arms for each phase and the voltages across each arm.

The voltage and current of each arm can be derived using Kirchoff's Voltage Law (KVL) and Kirchoff's Current Law (KCL). KVL states that the sum of voltages in a closed loop

of a circuit is zero. It is sufficient to analyze one phase consisting of one positive and one negative arms. Figure 3.2 highlights two closed loops for the KVL analysis, and a *Node 1* for the KCL analysis.

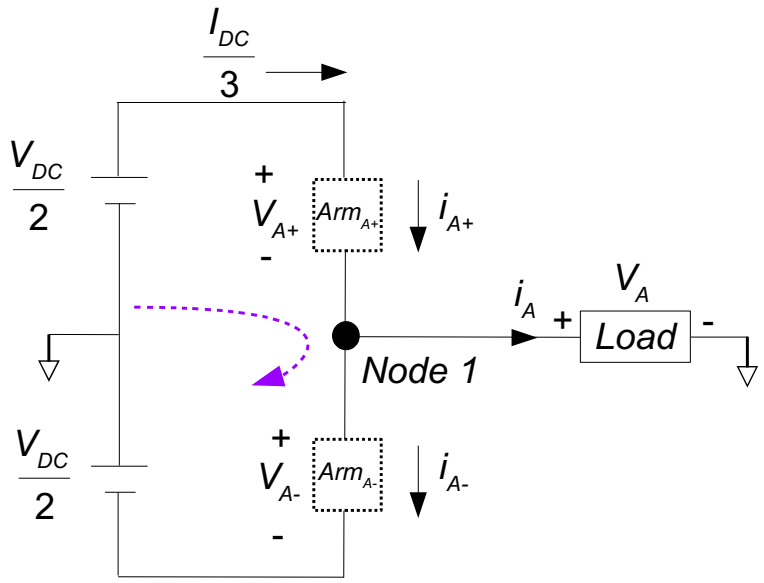


Figure 3.2: A single-phase half-bridge configuration, demonstrating one arm that is divided into a positive side (top arm) and a negative side (bottom arm). The DC current flowing into the arm is $\frac{I_{DC}}{3}$ for a three-phase system consisting of three arms.

The voltageof the positive arm of the converter, arm_{X+}, is characterized by Equation 3.1, and the voltage across the negative arm of the converter, arm_{X-}, is characterized by Equation 3.2.

$$\text{Positive arms:} \begin{cases} V_{A_+} = \frac{V_{DC}}{2} - V_A \\ V_{B_+} = \frac{V_{DC}}{2} - V_B \\ V_{C_+} = \frac{V_{DC}}{2} - V_C \end{cases} \tag{3.1}$$

$$\text{Negative arms:} \begin{cases} V_{A_-} = \frac{V_{DC}}{2} + V_A \\ V_{B_-} = \frac{V_{DC}}{2} + V_B \\ V_{C_-} = \frac{V_{DC}}{2} + V_C \end{cases} \tag{3.2}$$

The input DC current I_{DC} is divided into three arms for a three phase system, shown in Figure 3.1. The current flowing into each arm is derived using KCL, where the sum of currents in a selected node is zero. Figure 3.2 shows *Node 1* where the the sum of currents flowing into it is zero. The current going into the positive arm the converter, arm_{X+}, is characterized by Equation 3.3, and on the negative arms, arm_{X-}, the currents are shown in Equation 3.4.

$$\text{Positive arms:} \begin{cases} I_{A_+} = \frac{I_{DC}}{3} + \frac{I_A}{2} \\ I_{B_+} = \frac{I_{DC}}{3} + \frac{I_B}{2} \\ I_{C_+} = \frac{I_{DC}}{3} + \frac{I_C}{2} \end{cases} \tag{3.3}$$

$$\text{Negative arms:} \begin{cases} I_{A_-} = \frac{I_{DC}}{3} - \frac{I_A}{2} \\ I_{B_-} = \frac{I_{DC}}{3} - \frac{I_B}{2} \\ I_{C_-} = \frac{I_{DC}}{3} - \frac{I_C}{2} \end{cases} \tag{3.4}$$

The half-bridge converter configuration is then used as a design blueprint where each arm can be populated with a desired circuit topology to satisfy the voltage and current

requirements imposed by the above equations. There are six independent arms for a DC-to-three-phase AC conversion, three each on the positive side (top) and negative side (bottom) of converter. Thus, the half-bridge converter voltage and current analysis are applicable for the proposed designs.

3.2 Conventional Submodule Topology

A half-bridge MMC has n number of submodules in each arm. Figure 3.3 demonstrates how the submodules are connected in each arm with a half-bridge configuration. If each arm consists of five submodules, the converter can be said to be a five-level converter – the multilevel idea in the MMC. The conventional MMC submodules are populated with the conventional submodule topology which is discussed next.

The conventional submodule topology uses one SPDT and a submodule capacitor across the SPDT. A half-bridge circuit, shown in Figure 3.4, demonstrates three submodules for a DC-to-three-phase AC MMC. The three submodules are independent from each other, meaning that they are connected to separate submodule capacitors. The distributed arm inductor L_{arm} is shown between two connected submodules to indicate current stiffness between the two modules. In summary, one conventional submodule typically feature three main electronic components; a capacitor, an SPDT switch, and an arm inductor.

When the switch S_X, where $X = [A, B, C]$, is in position "1", the submodule is in an active state and the current from the DC input charges the submodule capacitor C^n. The

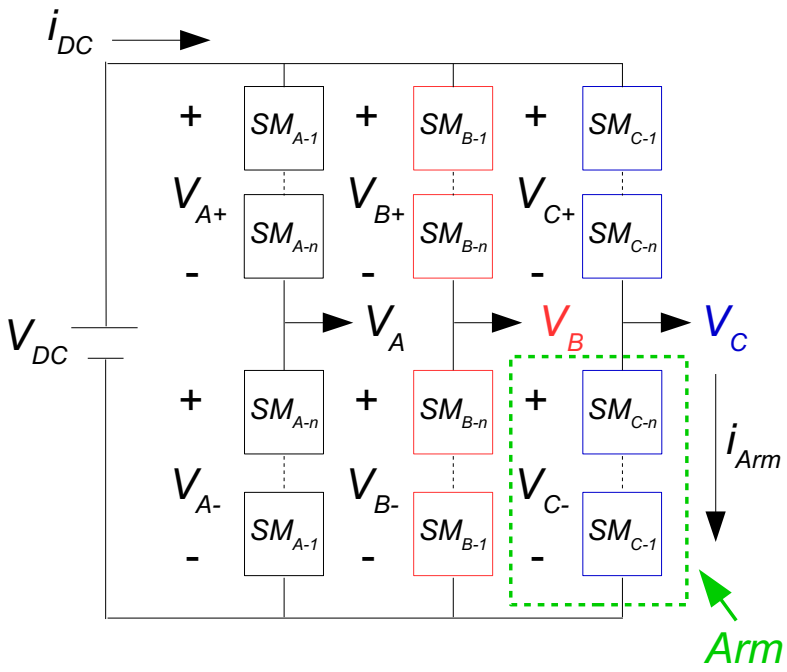


Figure 3.3: A diagram of conventional MMC structure for a DC-to-three-phase AC conversion with n number of submodules in each arm, highlighted in green. There are positive and negative arms for each phase, resulting in six independent arms.

submodule capacitor current, i_{Cap}, is the arm current of that particular submodule. When the switch S_X is in position "0", the input current flows into another switch connected to the next submodule underneath it and the submodule is in a zero state. The conventional SPDT module is implemented using two transistor devices, as demonstrated in Figure 3.4(b). The output voltage, reflected in the arm voltage V_{Arm-X} for $X = [A, B, C]$, is V_{Cap} during an active state, and zero during a zero state as summarized in Figure 3.4(c).

The modulation functions are the functions determining the duration of the switches in the active state (on). Each independent arm is controlled by a specific modulation function

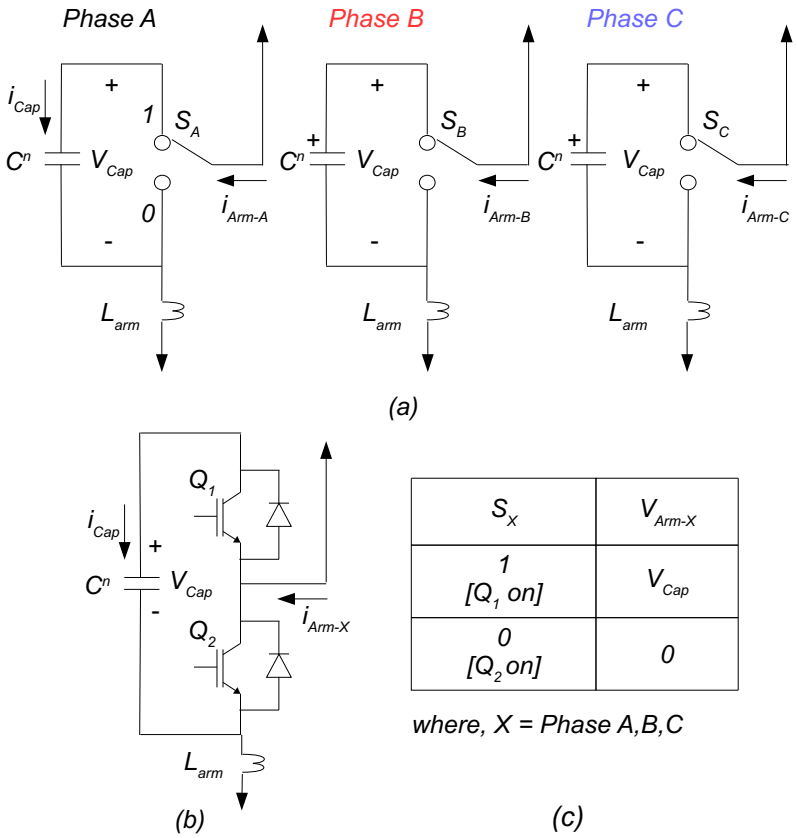


Figure 3.4: (a) Conventional submodule for a three-phase system demonstrating three independent submodules, each with an SPDT swicth, a submodule capacitor, and an arm inductor. The size of the submodule capacitor and the arm inductor are the same for all submodules. (b) The SPDT switch in each submodule is realized using two transistor devices. (c) The arm voltage V_{Arm-X} equals the capacitor voltage V_{Cap} during active state (SPDT switch in position "1") and zero during zero state (SPDT switch in position "0").

derived from its *arm voltage*. The arm voltage is the sum of the voltage across the module capacitors in each arm. For the six arms, three phase arms from each of the positive and negative sides, the voltage characteristics in relation with the modulation functions are expressed in Equation 3.5 and Equation 3.6. The variables $m_{A,B,C\pm}$ are the modulation functions of the positive and negative arms for phase A, B and C, respectively, and $V_{A,B,C\pm}$

are the voltage across the positive and negative arms.

$$\text{Positive arms:} \begin{cases} m_{A+} \times n \times V_{Cap}^{n} = V_{A+} \\ m_{B+} \times n \times V_{Cap}^{n} = V_{B+} \\ m_{C+} \times n \times V_{Cap}^{n} = V_{C+} \end{cases} \tag{3.5}$$

$$\text{Negative arms:} \begin{cases} m_{A-} \times n \times V_{Cap}^{n} = V_{A-} \\ m_{B-} \times n \times V_{Cap}^{n} = V_{B-} \\ m_{C-} \times n \times V_{Cap}^{n} = V_{C-} \end{cases} \tag{3.6}$$

The voltages across each arm of the three phases are the same as in the half-bridge converter, given in Equation 3.1 and Equation 3.2. These voltages consist of the input DC voltage and the corresponding output AC voltage. To derive the modulation functions, the following design specifications must be determined by the power converter designer:

- The input DC voltage value, V_{DC}.
- The desired output AC voltage, V_A, V_B, V_C.
- The number of submodules in each arm, n.

3.2.1 Conventional Submodule Capacitor Sizing

The modulation functions for conventional topology are applicable for the proposed topology because both designs use the half-bridge configuration MMC. Due to the half-bridge configuration, the sum of voltage across the submodule capacitors in each arm is

$$\sum_{n=1}^{n} V_{Cap}^{n} = \frac{V_{DC}}{2} \tag{3.7}$$

where V_{C^n} is the voltage across submodule capacitor C^n and V_{DC} is the input DC voltage. The submodule capacicor is sized based on fundamental capacitance characteristic shown in Equation 3.8, where C^n is the capacitance value, i_{Cap} is the capacitor current, and $\frac{dv}{dt}$ is the change in voltage over a certain period of time. The capacitor current, i_{Cap}, is a function of the input power. The voltage ripple, dv, is a periodic variation of the capacitor voltage. The submodule capacitor voltage consists of the arm voltage, $V_{X\pm}$ for $X = [A, B, C]$, where each of the arm voltage has sinusoidal AC waveforms from the AC output. Recall Equations 3.5-3.6 and Equations 3.1-3.2. Due to the existence of single-phase AC frequency current in each module capacitor, the ripple voltage dv is periodic with an AC frequency of 60 Hz, resulting in higher voltage ripple. A higher voltage ripple increases the capacitor size requirement.

$$i_{Cap} = C^n \frac{dv}{dt} \tag{3.8}$$

The capacitor sizing requirements are characterized using the voltage and current requirements imposed by the conventional circuit topology and the power conversion specifications.

Recall that in a conventional module, the submodule capacitor current is the arm current in each phase. For example, the submodule capacitor current in phase A arm can be written as $i_{Cap} = I_{A+}$. The submodule capacitor current of all six arms can then be expressed using Equation 3.9 and Equation 3.10, where the switches are in an active state for the duration of the *duty ratio*, d.

$$\text{Positive arms:} \begin{cases} i_{Cap_{A+}} = m_{A+} \times I_{A+} \\ i_{Cap_{B+}} = m_{B+} \times I_{B+} \\ i_{Cap_{C+}} = m_{C+} \times I_{C+} \end{cases} \tag{3.9}$$

$$\text{Negative arms:} \begin{cases} i_{Cap_{A-}} = m_{A-} \times I_{A-} \\ i_{Cap_{B-}} = m_{B-} \times I_{B-} \\ i_{Cap_{C-}} = m_{C-} \times I_{C-} \end{cases} \tag{3.10}$$

where $i_{Cap_{X\pm}}$ is the submodule capacitor current in each phase $X = [A, B, C]$ for positive and negative arms, $m_{X\pm}$ respective modulation function for each phase $X = [A, B, C]$ in positive and negative arms shown in Equations 3.5-3.6, and $I_{X\pm}$ is the arm current for each phase $X = [A, B, C]$ in the positive and negative arms shown in Equations 3.3-3.4.

Note that both the modulation functions and the arm currents consist of sinusoidal waveforms from the AC outputs. Expanding Equations 3.9-3.10 provides capacitor current

results expressed in Equation 3.11 and Equation 3.12.

$$\text{Positive arms:} \begin{cases} i_{Cap_{A+}} = \left(\frac{V_{DC}/2 - V_A}{n \times V_{Cap}^n}\right)\left(\frac{I_{DC}}{3} + \frac{I_A}{2}\right) \\ i_{Cap_{B+}} = \left(\frac{V_{DC}/2 - V_B}{n \times V_{Cap}^n}\right)\left(\frac{I_{DC}}{3} + \frac{I_B}{2}\right) \\ i_{Cap_{C+}} = \left(\frac{V_{DC}/2 - V_C}{n \times V_{Cap}^n}\right)\left(\frac{I_{DC}}{3} + \frac{I_C}{2}\right) \end{cases} \tag{3.11}$$

$$\text{Negative arms:} \begin{cases} i_{Cap_{A-}} = \left(\frac{V_{DC}/2 + V_A}{n \times V_{Cap}^n}\right)\left(\frac{I_{DC}}{3} - \frac{I_A}{2}\right) \\ i_{Cap_{B-}} = \left(\frac{V_{DC}/2 + V_B}{n \times V_{Cap}^n}\right)\left(\frac{I_{DC}}{3} - \frac{I_B}{2}\right) \\ i_{Cap_{C-}} = \left(\frac{V_{DC}/2 + V_C}{n \times V_{Cap}^n}\right)\left(\frac{I_{DC}}{3} - \frac{I_C}{2}\right) \end{cases} \tag{3.12}$$

where n is the number of submodules, V_{Cap}^n is the submodule capacitor voltage, V_{DC} is the input DC voltage, V_A, V_B, V_C are the output AC voltages, and I_A, I_B, I_C are the output AC currents with the following sinusoidal functions

$$\text{Output AC Voltages:} \begin{cases} V_A = \hat{V_A}\ cos(\omega t) \\ V_B = \hat{V_B}\ cos(\omega t - 120°) \\ V_C = \hat{V_C}\ cos(\omega t + 120°) \end{cases} \tag{3.13}$$

$$\text{Output AC Currents:} \begin{cases} I_A = \hat{I_A}\ cos(\omega t) \\ I_B = \hat{I_B}\ cos(\omega t - 120°) \\ I_C = \hat{I_C}\ cos(\omega t + 120°) \end{cases} \tag{3.14}$$

Using $X = [A, B, C]$ to represent each phase in Equation 3.11 and Equation 3.12, the equations can be generalized as

$$i_{Cap_{X+}} = \left(\frac{V_{DC}}{2nV_{Cap}^{n}} - \frac{V_X}{nV_{Cap}^{n}}\right)\left(\frac{I_{DC}}{3} + \frac{I_X}{2}\right), \tag{3.15}$$

$$i_{Cap_{X-}} = \left(\frac{V_{DC}}{2nV_{Cap}^{n}} + \frac{V_X}{nV_{Cap}^{n}}\right)\left(\frac{I_{DC}}{3} - \frac{I_X}{2}\right). \tag{3.16}$$

Note that V_X and I_X are sinusoidal functions consisting of ω term, the AC frequency of the three-phase system. The positive and negative arm notations are not included because the multiplication products give the same results. The products of Equation 3.15 and Equation 3.16 can then be expressed as

$$\boxed{i_{Cap_{X\pm}} = \frac{1}{n \times V_{Cap}^{i}}\left(\underbrace{\frac{V_{DC}I_{DC}}{6}}_{\text{dc term}} - \underbrace{\frac{V_X I_X}{2}}_{\omega^2 \text{ term}} + \underbrace{\frac{V_{DC}I_X}{4}}_{\omega \text{ term}} - \underbrace{\frac{V_X I_{DC}}{3}}_{\omega \text{ term}}\right)} \tag{3.17}$$

The conventional MMC approach imposes low-frequency AC currents into the DC module capacitors due to which the DC capacitances are voluminous for high-performance operation. The capacitance value of a capacitor is proportional to the capacitor current and its voltage ripple; recall Equation 3.8. The higher the capacitor current, the higher the capacitance value, which translates to bigger capacitor size requirement. The module capacitor DC current expressed in Equation 3.17 consists of AC currents from low frequencies which requires bulky and voluminous capacitance for high performance operations. ***Equation 3.17 summarizes the main disadvantage of the conventional MMC topology, which requires a large and bulky submodule capacitor, thereby reducing the converter power density.***

Electrolytic capacitors are commonly used as the module capacitors in modular power converters because of their ability to provide higher capacitance values. However, due to their physical structure, electrolytic capacitors are not the most reliable commercially-available capacitors. Sudden changes in the capacitor voltage can damage an electrolytic capacitor and even cause fire. In modular power converters that utilize electrolytic capacitors, these capacitors are the first component to fail due to their short life cycle, which affects the overall performance of the modular power converter. More on electrolytic capacitor characteristic is discussed in [3]. In conventional design, electrolytic capacitors are typically used to meet a large capacitance requirement. Using this type of capacitor is a disadvantage in high power conversion applications. The motivation of this thesis work is to reduce the module capacitor size for high power conversion applications to avoid using electrolytic capacitors, and to use more reliable commercially-available capacitors, such as thin-film capacitors.

3.3 Conventional Three-Phase AC Bridge Circuits

The idea of designing a module topology consisting of a three-phase system is an attractive option because the sum of voltages and currents in a balanced three-phase system are zero. Recall that in the conventional module, the capacitor current, i_{Cap}, is imposed with AC frequency, which increases the capacitance size requirement due to a single-phase module topology. With a balance three-phase system, the net current is zero. Therefore, a module is

designed based on the conventional three-phase AC bridge circuit such that the net capacitor voltage and current are zero, reducing capacitor size requirement.

A half-bridge converter for DC-to-three-phase AC is achieved by adding two additional identical arms across the DC input. The SPDT switches are then populated using transistors, as shown in Figure 3.5. This design is referred to as the *classical three phase inverter*.

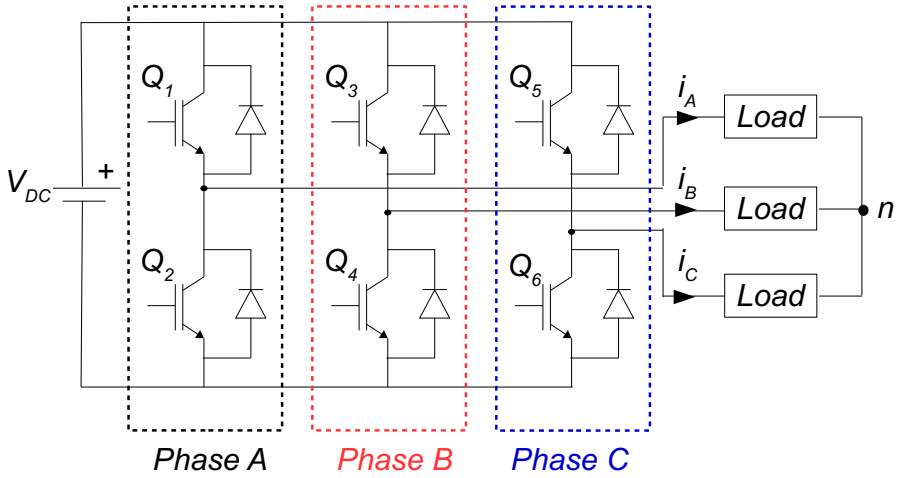


Figure 3.5: Classical DC-to-three-phase AC converter.

Modular power converters are built by connecting multiple modules to achieve high power conversion capability. Classical DC-to-three-phase AC power converter cannot be connected together to form a modular power converter because a connection between two cannot be established properly. Figure 3.6 shows two connected DC-to-three-phase AC converters. When the switches are in position "0", the connection between two switches are shorted by the negative side of the converter. As such the circuit cannot be used as a module.

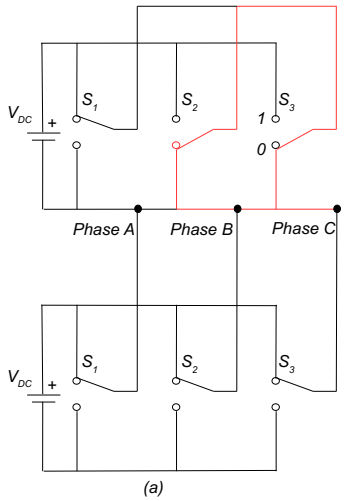


Figure 3.6: Classical three phase AC bridge circuit used as two connected submodules with top two switches, S_2 and S_3 in zero state. This topology is not applicable for an MMC due to the shorted circuit, which prevent module capacitor charging. The capacitor is shorted.

3.4 Proposed Module Topology

The proposed topology is an *integrated module*, referred to as "module" in this thesis. Several modules can form modular power converters, with the connections between modules shown in Figure 3.7. By connecting two or more modules together, the input power can be distributed to each of the modules for DC-to-AC power conversion.

The proposed module topology uses a half-bridge configuration at the modular level, as demonstrated in Figure 3.8. Unlike the classical three-phase inverter in Figure 3.5, the proposed module topology uses two SPDT switches rather than one, permitting modules to be connected together. The module consists of a shared module capacitor, C^n_{ABC}, unlike the conventional topology that uses one capacitor per submodule, as demonstrated in Figure

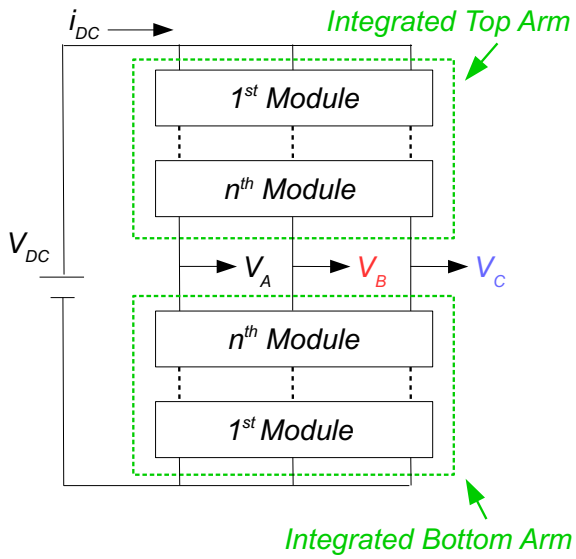


Figure 3.7: A block diagram of an MMC with integrated module design. The top and bottom integrated arm includes n modules.

3.4. In the proposed module, one module capacitor is shared between the three phase arms, reducing the number of module capacitors required to form modular power converter.

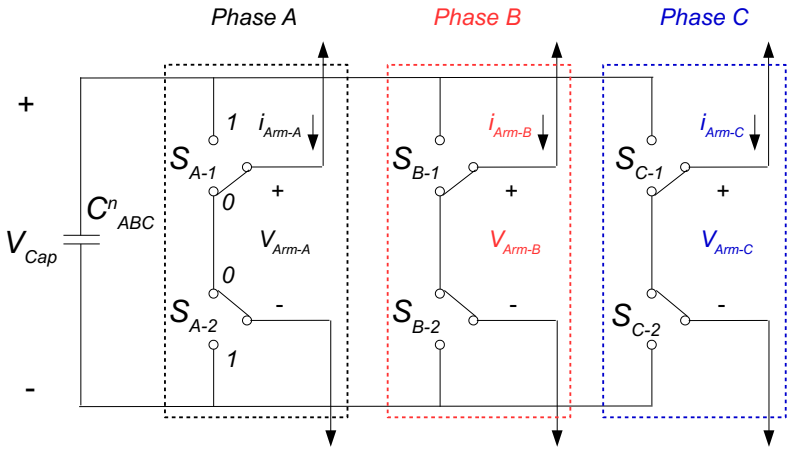


Figure 3.8: Circuit topology of an integrated module design with two SPDT switches. A shared module capacitor is connected with phase A, B, and C arms.

The SPDT switches are in the active state (on) when the switches are in position "1", as shown in Figure 3.8, or in the zero state (off) when the switches are in position "0", as shown in Figure 3.9. The active state is when power transfer from the DC input to the module capacitor occurs, charging the capacitor (storing an intermediate energy) for a specified period of time. Unlike the classical DC-to-three-phase AC converter, multiple modules of the proposed design are achievable in both switching states, which eliminates the shorted connection between two switches. Figure 3.9 demonstrates connected switches between two modules when the switches are in position "0".

An inductor is placed between two connected switches to indicate *current stiffness*, similar to the conventional design. In the conventional submodule, recall Figure 3.4, one *arm inductor* is required for each submodule in each phase. In this proposed module, the net *arm inductance* is carefully distributed across multiple inductors placed in between two connected switches. The distribution factors starts from K^1 to K^{n+1}, where K^1 indicates the first inductor prior to the first module of a modular power converter. The distribution factors are derived to meet voltage blocking capabilities of the transistor devices, which is discussed toward the end of this section.

3.4.1 Modular Power Converter Schematic with Proposed Module

The proposed modular power converter schematic has the desired number of modules, n, in an MMC half-bridge configuration, shown in Figure 3.7. Using the proposed module

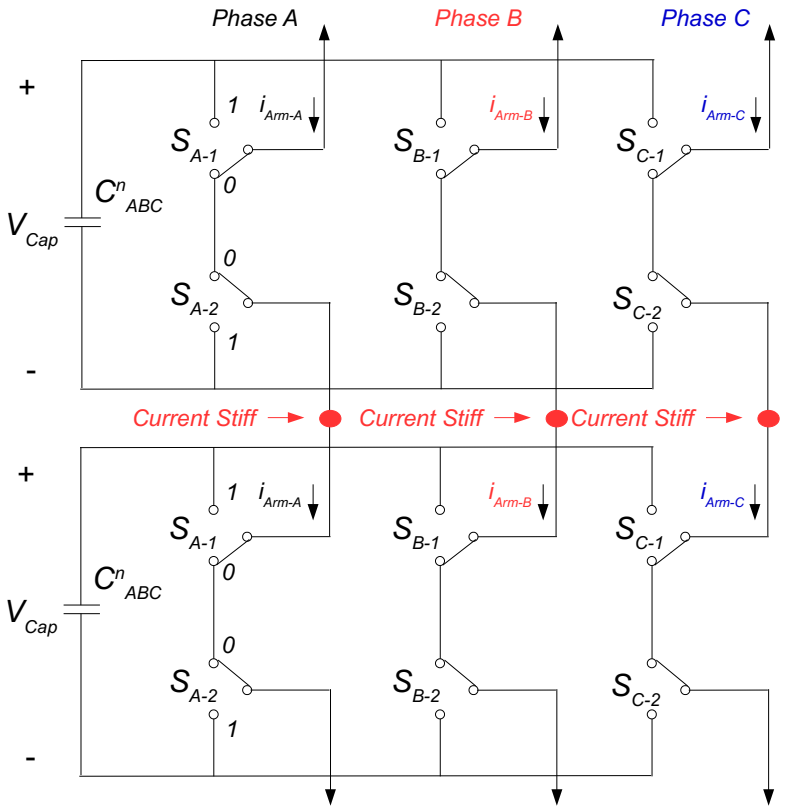


Figure 3.9: An integrated module design allows connection modules for power transfer due to the use of two SPDT swictces with proper placement. Current stiff points are highlighted to emphasize the need for inductor usage in each point.

shown in Figure 3.8, and placing an inductor between connected modules provide a high-level overview of a modular power converter with proposed module topology. Figure 3.10 demonstrates an n-level DC-to-three-phase AC MMC with the proposed module design in each module. The integrated positive (top) and negative (bottom) arms, highlighted in Figure 3.10, of the converter are symmetrical, meaning that each arm has the same number of modules, n.

The structure of modular power converter design follows a half-bridge configuration,

shown in Figure 3.1. Conventional and proposed designs have identical arm voltages and currents due to the same structural characteristic that are used to build an MMC. The voltages across the positive arms expressed in Equation 3.1 and the voltages across the negative arms in Equation 3.2 are applicable for the proposed MMC. Similarly, the currents expressed in Equations 3.3-3.4 can be used in the proposed MMC.

Two SPDT switches in each arm allow for energy storage sharing through the shared module capacitor when the switches are in active state. The SPDT switches are realized using MOSFET devices, demonstrated in Figure 3.11. The switches Q_1 and Q_2 are operated synchronously, meaning that the switches receive the same control signals. Switch state "1" and "0" correspond to a module output voltage $V^n_{arm-x} = V_{Cap}$ and $V^n_{arm-X} = 0$ respectively, where superscript i refers to the n^{th} module, and $X = [A, B, C]$ phase.

The module capacitor current in the proposed topology is the sum of the currents from all of the integrated three phase arms in the module characterized by Equation 3.18 for the positive arms and Equation 3.19 for the negative arms.

$$i_{Cap+} = m_{A+} \times I_{A+} + m_{B+} \times I_{B+} + m_{C+} \times I_{C+} \tag{3.18}$$

$$i_{Cap-} = m_{A-} \times I_{A-} + m_{B-} \times I_{B-} + m_{C-} \times I_{C-} \tag{3.19}$$

Using the derived modulation functions in Equations 3.5-3.6, and the current across each arm in Equations 3.3-3.4, the module capacitor current in the proposed scenario can be

written as

$$i_{Cap+} = \left(\frac{V_{DC}}{2nV^i_{Cap}} - \frac{V_A}{nV^i_{Cap}}\right)\left(\frac{I_{DC}}{3} + \frac{I_A}{2}\right) + \left(\frac{V_{DC}}{2nV^i_{Cap}} - \frac{V_B}{nV^i_{Cap}}\right)\left(\frac{I_{DC}}{3} + \frac{I_B}{2}\right) + \left(\frac{V_{DC}}{2nV^i_{Cap}} - \frac{V_C}{nV^i_{Cap}}\right)\left(\frac{I_{DC}}{3} + \frac{I_C}{2}\right), \tag{3.20}$$

$$i_{Cap-} = \left(\frac{V_{DC}}{2nV^i_{Cap}} + \frac{V_A}{nV^i_{Cap}}\right)\left(\frac{I_{DC}}{3} - \frac{I_A}{2}\right) + \left(\frac{V_{DC}}{2nV^i_{Cap}} + \frac{V_B}{nV^i_{Cap}}\right)\left(\frac{I_{DC}}{3} - \frac{I_B}{2}\right) + \left(\frac{V_{DC}}{2nV^i_{Cap}} + \frac{V_C}{nV^i_{Cap}}\right)\left(\frac{I_{DC}}{3} - \frac{I_C}{2}\right). \tag{3.21}$$

The products of Equation 3.20 and Equation 3.21 are identical. Hence, the shared capacitor current for the positive and negative arms is

$$\boxed{i_{C_{ABC}} = \frac{1}{nV^i_{Cap}}\Big(\underbrace{\frac{V_{DC}I_{DC}}{2} - \frac{V_AI_A + V_BI_B + V_CI_C}{2}}_{\text{zero per } T_{SW}} + V_{DC}\underbrace{\frac{I_A + I_B + I_C}{4}}_{\text{zero per } T_{SW}} - I_{DC}\underbrace{\frac{V_A + V_B + V_C}{3}}_{\text{zero per } T_{SW}}\Big)} \tag{3.22}$$

where V_A, V_B, V_C are the output AC voltages, and I_A, I_B, I_C are the output AC currents. The average output AC voltage and current over one switching period is zero, and can be calculated using Equation 3.23.

$$V_{X_{Avg}} = \frac{1}{T_{SW}}\int_0^{T_{SW}} V_X(t)dt$$
$$I_{X_{Avg}} = \frac{1}{T_{SW}}\int_0^{T_{SW}} I_X(t)dt \tag{3.23}$$

Comparing the proposed capacitor current in Equation 3.22 and the conventional capacitor current in Equation 3.17, the module capacitor average current with the proposed design is zero because the average AC voltage and current per switching period are zero. In contrast, the conventional capacitor current carries AC current due to the existence of the ω term, imposing AC current in the submodule capacitor. The zero average capacitor current in the proposed topology is the key advantage permitting significant reduction in the capacitor size requirement in a module. This increases the power density of a modular power converter.

3.4.2 Proposed Module Capacitor Sizing

The size of the capacitor is determined by the capacitor ripple voltage, dv, as previously discussed in the conventional case. In the proposed integrated module, the capacitor voltage, V_{Cap}^{n}, is a function of a three-phase AC system per switching cycle. As a result, the ripple voltage is periodic with the switching frequency, f_{SW}, 24.4 kHz in this thesis work. This is in contrast to conventional design where the capacitor ripple voltage is a function of the low AC frequency of 60 Hz due to single-phase design per module. Recall Equation 3.8, given the same voltage ripple requirement, say dv is limited to 5%, it is clear that an integrated module significantly reduces capacitor size requirement due to the reduction in voltage ripple period. dt.

3.4.3 Arm Inductor Distribution in Proposed Topology

The focus of this section is to discuss how the values of the inductors between the proposed modules are optimized. The optimization objective is to achieve positive voltage across each of the switch device. This is due to the fact that unidirectional MOSFETs are used in this thesis work. Although bidirectional switches can operate with the proposed design, these are not used in this thesis work because with the current available switch technologies, the number of switches required to realize bidirectional functionality is twice that of unidirectional switch.

In the conventional topology, an arm inductor is required in each module. The proposed design distributes an arm inductor between connected modules. An arm inductor, L_{arm}, is distributed into $n+1$ number of inductors such that the sum of the distribution factor, K^n, is one, as expressed in Equation 3.24.

$$\sum_{i=1}^{i} K^i = 1 \tag{3.24}$$

The relationship between the voltage across the module capacitors and the voltage across each switch can be used to determine optimal values of the distribution factors, K^n to K^{n+1}. For analysis purposes, Figure 3.12 shows three connected modules, specifically the positive arms of phase A and phase B.

In Figure 3.12, phase A arm has switches in position "1" (active state), and phase B arm, highlighted in red, has switches in position "0" (zero state). The switches in phase B

arm are labelled S_1 to S_6 and the voltages across each switch are labelled V_{S1} to V_{S6} with the positive polarity of each voltage shown. There are four distributed inductors across the three-level modules with the distibution factors $K_1 : K_2 : K_3 : K_4$. The voltages across the module capacitors in terms of the switches voltages are

$$\text{Capacitor voltages: } \begin{cases} V_{C1} = V_{S1} + V_{S2} \\ V_{C2} = V_{S3} + V_{S4} \\ V_{C3} = V_{S5} + V_{S6} \end{cases} \tag{3.25}$$

where V_{S1} to V_{S6} is the voltage across the corresponding switch in Figure 3.12. The inductor design criteria is such that the voltages across the switches must be positive due to the unidirectional switch blocking capability. The voltages across the switches can be expressed as

$$\begin{aligned} V_{S1} &= K^1(V_{AB} + V_{Cap}) \\ V_{S2} &= \frac{V_{Cap}}{n} - K^1(V_{AB} + V_{Cap}) \\ V_{S3} &= \frac{V_{Cap}}{n} - (K^1 + K^2)(V_{AB} + V_{Cap}) \\ V_{S4} &= (K^1 + K^2)(V_{AB} + V_{Cap}) \\ V_{S5} &= (K^3 - K^1 - K^2)(V_{AB} + V_{Cap}) \\ V_{S6} &= K^4(V_{AB} + V_{Cap}) \end{aligned} \tag{3.26}$$

where V_{AB} is the line-line output AC voltage between V_A and V_B, n is the number of integrated modules, and V_{Cap} is the sum of capacitor voltage across an integrated arm.

Solving for the distribution factors, K^1 to K^{n+1}, provides a range of values that meet the design criteria. The two SPDT switches are realized using MOSFETs or IGBTs, as shown in Figure 3.11. The voltage across the synchronized switches, V_{Q1} and V_{Q2}, when analyzed between two phases, say phase x and y, is generally characterized by Equation 3.27.

$$\begin{aligned} V_{Q2}^{n} + V_{Q1}^{n+1} &= K^{i}(V_{arm}^{x} - V_{arm}^{y}) \\ V_{Q2}^{n} &= V_{Cap} - V_{Q1}^{n} \end{aligned} \tag{3.27}$$

where V_{Q1} and V_{Q2} refer to the top and bottom switches in Figure 3.11. Superscript n refers to the n^{th} module, V_{arm}^{x} and V_{arm}^{y} refer to the arm voltages of the two phases. Proper choice of K^n coefficients ensures unidirectional blocking voltages across transistors, $Q1$ and $Q2$, and reduces semiconductor sizing. The net arm inductance is similar to the conventional design arm inductance.

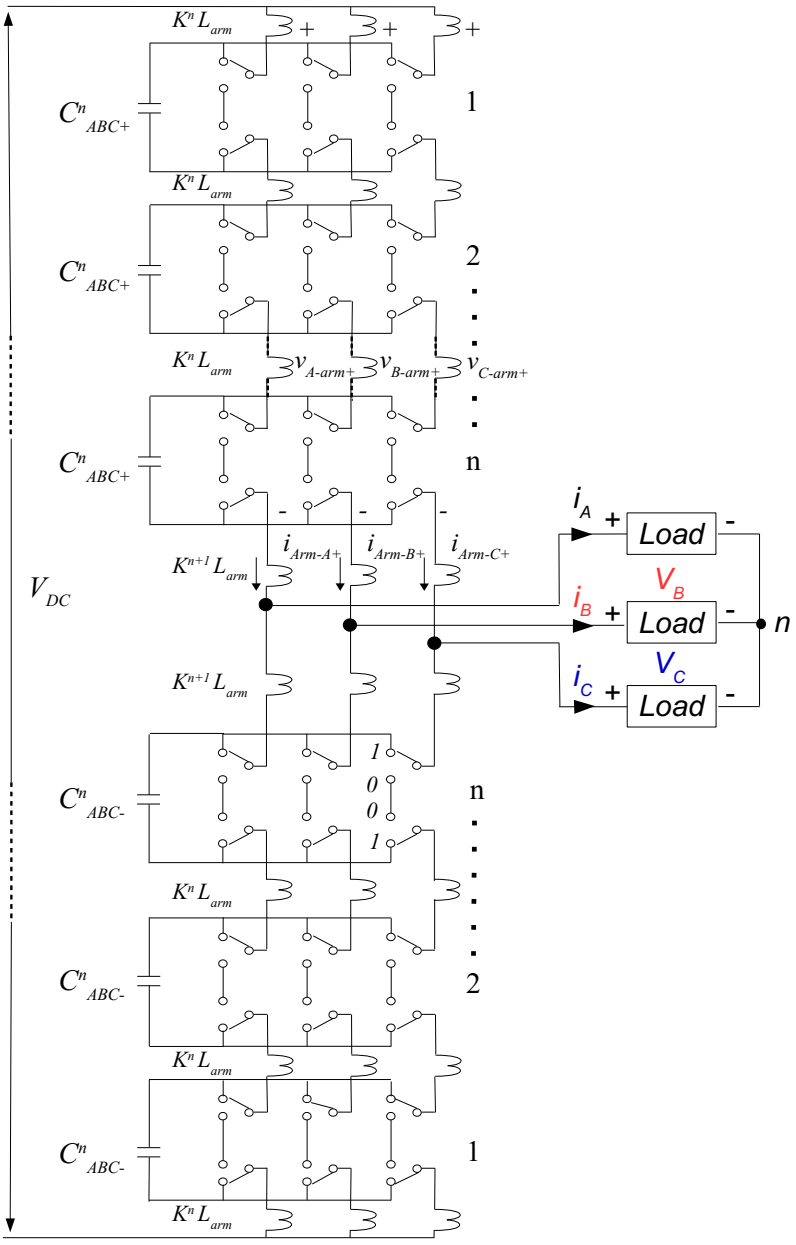
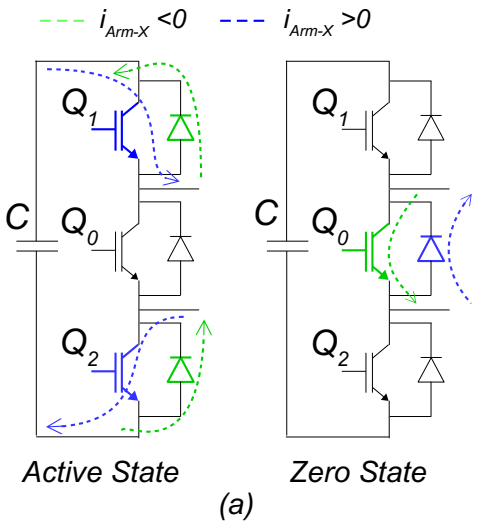


Figure 3.10: A complete overview of an MMC with n module using integrated module design. An inductor is placed between two connected modules. The number of inductors needed for n modules is $n + 1$ and the net inductance is the same as the arm inductance of a conventional module design.



$S_{X\text{-}1}$ & $S_{X\text{-}2}$	$V_{Arm\text{-}X}$
1 [Q_1 & Q_2 on]	V_{Cap}
0 [Q_0 on]	0

where, X = Phase A,B,C

(b)

Figure 3.11: (a) The realization of two SPDT switches in an integrated module uses three transistor devices. Transistors Q_1 and Q_2 are syncrhronized, receiving the same control signal while transistor Q_0 receives the complementary control signal. (b) The summary of the arm voltage during active state (Q_1 and Q_2 on) and zero state (Q_0 on).

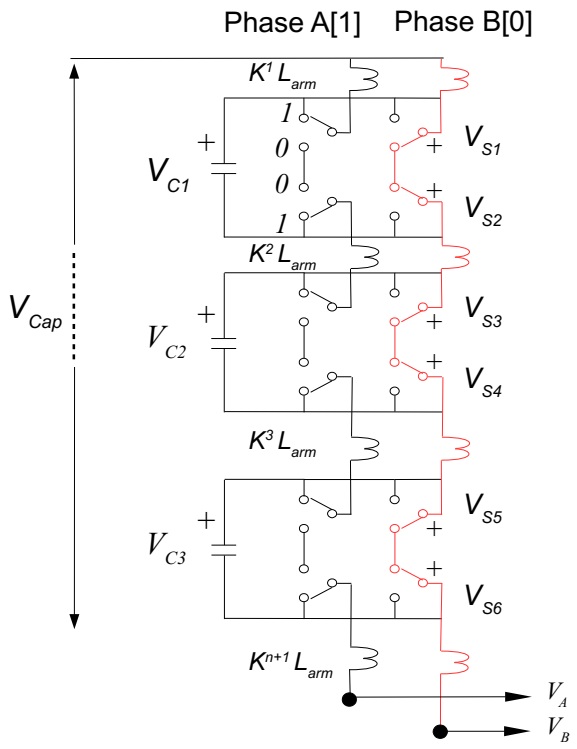


Figure 3.12: Overview of the positive arm showing phase A in active state and phase B in zero state. During an active state, the intermediate energy storage is achieved through the module capacitors. During a zero state, the intermediate energy storage is achieved through the distributed arm inductor.

4 Converter Modulation and Control Design Considerations

This section focuses on control methods with the proposed DC/AC Modular Converter topology. Power converters are typically controlled with different types of modulation approaches. In this thesis work, an open-loop control design is developed for the DC-to-three-phase AC modular power converter. The focus of this work is to verify the integrated module design for an MMC application, the circuit analysis, and the necessary modulation needed as proof of concept. Closed-loop control control can be implemented based on application-specific considerations. However, it is not the focus of this section.

The use of three transistors, Q_0-Q_2 to realize the SPDT switches in the proposed module, recall Figure 3.11, is translated to having switch Q_1 and Q_2 controlled by the same modulation function (synchronous), and switch Q_0 controlled by the complementary modulation function, $m_{X\pm}$.

For the proposed topology, the maximum duty ratio is $d_{X\pm} = \frac{1}{3}$. This means that the three-phase arms in the integrated proposed module cannot be in the active state (on) at the same time to prevent circulating currents between the three-phases. A control design criteria

can then be established by the limit shown in Equation 4.1

$$m_{x\pm} \leq \frac{1}{3}. \tag{4.1}$$

4.1 Duty Ratios Staggering

The shared capacitor in the proposed module means that only one phase of the three-phase arms can be in an active state at any given time during the switching period, T_{SW}, to prevent circulating AC currents between the three-phases. In the conventional module, the three-phase modules are not integrated, recall Figure 3.4, requiring one capacitor in each module. In the proposed integrated module, the three-phase arms can share one module capacitor.

For the proposed topology, the switches are controlled using the derived modulation functions in Equations 3.5-3.6 to meet desired output voltages. The established duty ratio boundaries for the three-phases means that the duty ratios are staggered, as demonstrated in Figure 4.1. The maximum duty ratio of phase A, B, C in the modulation functions is $\frac{1}{3}$. The carrier signals, shown in Figure 4.1, is the signals used to compare the modulation functions on the FPGA which create the swhiching signals, h_{Ax}, h_{Bx}, and h_{Cx}.

4.2 Modulation Implementation

The modulation functions are implemented using an FPGA board to output 12 SPWM signals, including the complementary signals, with time shifts. Although the theoretical

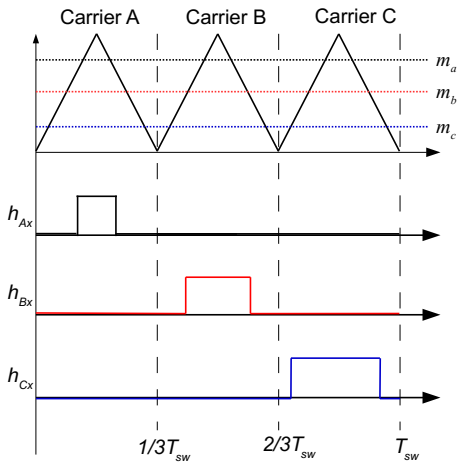


Figure 4.1: Switching function implementation of h_{Ax}, h_{Bx}, h_{Cx} where $x = \pm$ for positive and negative arms. Only one switch can be in the active state in positive of negative arm to prevent AC current circulation among the three phases due to the integrated module design connecting the three-phase arms with a shared capacitor.

maximum duty ratio is $\frac{1}{3}$ or 0.33, the chosen duty ratio is $0.3T_{SW}$, providing a margin of safety to prevent active-state overlap between switches of the three-phases when the control signals are implemented on the hardware while maximizing AC output voltage magnitude. SPWM can be implemented by several methods, one of which is to generate a list of values from a sinusoidal waveforms that can be used as duty ratios generating PWM, saved as a lookup-table of values.

Figure 4.2 shows how the SPWM are implemented on the FPGA board for this thesis work. A master clock with a frequency of 100 MHz is used as an input clock for the scaling block and the PWM block. The scaling block generates a slower clock of $100\ MHz/2^{12}$ or 24.4 kHz used to read a LUT consisting of sinusoidal waveforms values. There are 12 lookup tables consisting of the sinusoidal modulation function. These LUT values are then

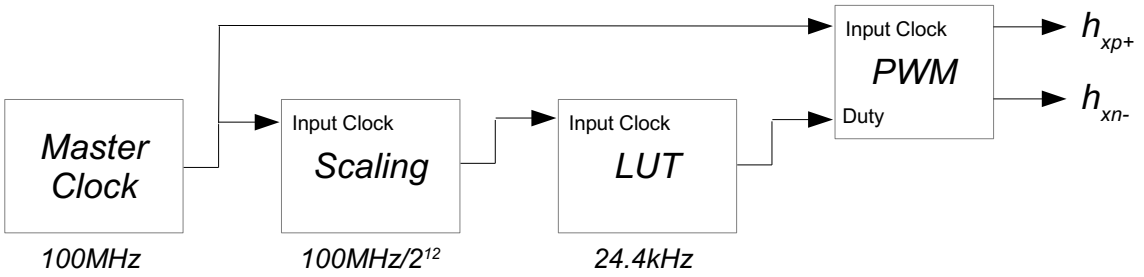


Figure 4.2: A block diagram of modulation function implementation for prototype testing using an FPGA board. Each block consists of a program with specific objective. The scaling block scales the master clock to a slower PWM output which is used as a clock for the lookup table block. The LUT block consists of a lookup table consisting a list of duty ratio values to implement SPWM that is then sent to the next block at every rising edge of the clock. The PWM block outputs switching functions $h_{xn\pm}$ to control the transistor devices.

fed to the PWM block as duty ratios with the switching frequency $f_{SW} = 24.4\ kHz$. The PWM block outputs 12 SPWM signals with time shifts at every, h_{Xp+} and h_{Xn-}, where $X = [A, B, C]$ phase and the subscripts p and n demonstrate the positive (top) and negative (bottom) arm respectively, and the subscript $+$ demonstrates the modulation function control signal $m_{X\pm}$ while the subscript $-$ is the complementary output of $m_X\pm$. Note that the number of SPWM signals are constant for any n number of modules in the converter.

The PWM block shown in Figure 4.2 operates by using state machines shown in Figure 4.3. The duty ratio value, d, is read from the look-up table at every rising edge of the clock. When the duty ratio value is greater than zero, the PWM output is high (PWM=1), and stays high until the value of d is equal to the constant value read from the lookup table when the PWM output then becomes low (PWM=0). The PWM output stays low until d reaches a specified boundary. A new duty ratio value is then read again from the lookup table in the load-duty state at the end of the specified boundary.

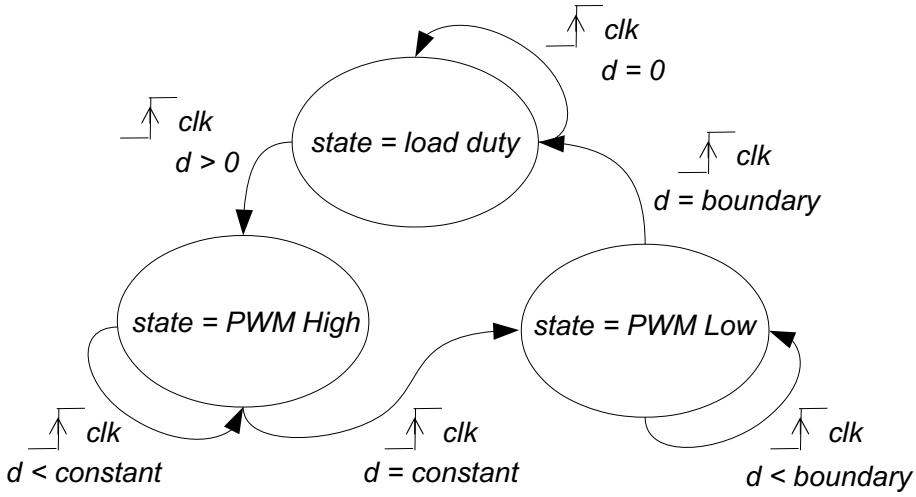


Figure 4.3: State machines of PWM program used in the PWM block shown in Figure 4.2.

The modulation functions implemented in the positive (top) and negative (bottom) arms are characterized by Equation 3.5 and Equation 3.6, respectively. d_{dc} and d_{ac} in terms of the input DC voltage and the output AC voltage can be written as

$$d_{dc} = \frac{V_{DC}}{2nV_{Cap}^{n}} \; ; \;\; d_{ac} = \frac{V_X}{nV_{Cap}^{n}} \tag{4.2}$$

where d_{dc} is the vertical shift implemented, such that the LUT values that the FPGA reads are positive, and d_{ac} is the AC amplitude of the three-phase outputs. The maximum duty ratio must fall under the limit expressed in Equation 4.1, say $d_{dc} = 0.2$ and $d_{ac} = 0.1$, where modulation functions are shown in Figure 4.4. Note that the three-phase AC outputs corresponds with the d_{ac} value, the higher the d_{ac} value, the higher the amplitude of AC outputs. For this modulation design example, the voltage transfer ratio between the DC and

AC side can be expressed as

$$\frac{d_{dc}}{d_{ac}} = \frac{V_{DC}}{2nV_{Cap}^{n}}\left(\frac{nV_{Cap}^{n}}{V_X}\right) = \frac{V_{DC}}{2V_X}. \tag{4.3}$$

For $d_{dc} = 0.2$ and $d_{ac} = 0.1$, the voltage transfer ratio between the DC and AC side is

$$V_X = \frac{V_{DC}}{4} \tag{4.4}$$

where X represents phase A, B, C.

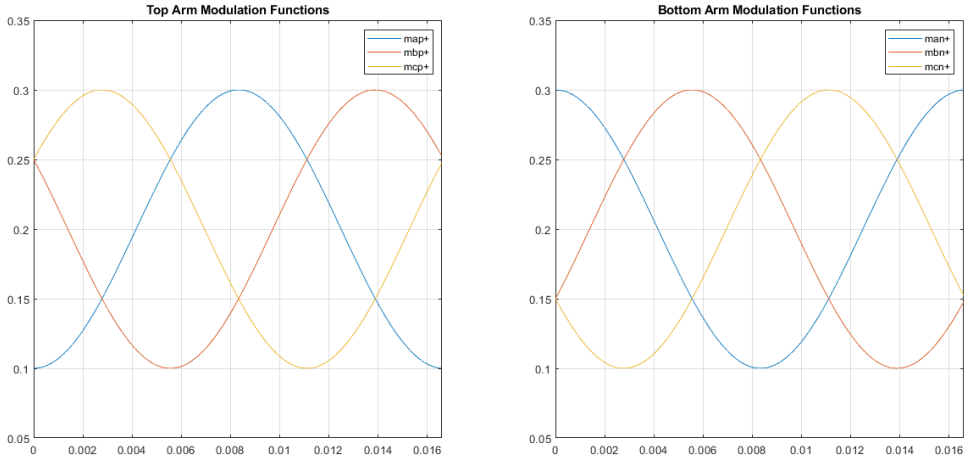


Figure 4.4: Example of modulation functions that can be implemented for modular power converter with integrated module design. These functions were implemented on FPGA board for prototype testing.

The proposed modulation implementation is independent of the AC output frequency. The modulation approach is applicable for any desired AC frequency such as 50 Hz and 60 Hz power systems. The number of values in the LUT determines the AC output frequency, which is characterized in Equation 4.5.

$$k_{LUT} = \frac{f_{SW}}{f_{AC}} \tag{4.5}$$

where k_{LUT} is the number of values in the LUT, f_{SW} is the switching frequency, and f_{AC} is the desired AC output frequency. In short, this modulation approach can be implemented for power converters requiring varied duty ratios with time shifts.

5 Results & Analysis

This section presents results from circuit simulations and experiments conducted with a laboratory-scale prototype. The objective is to verify the analytical work conducted on the new topology design. The simulation results of the conventional topology and proposed topology are compared to highlight the significant reduction in submodule capacitor.

5.1 Simulation Results

The proposed MMC topology is simulated using a circuit simulation software; Piecewise Linear Electrical Circuit Simulation (PLECS) for design verification. The size of the module capacitor in the proposed design is in the lower magnitude range of μF, a significant reduction in size and volume of the converter compared with conventional modules. One set of the design parameters for high power conversion simulation used in the PLECS simulation are shown in Table 5.1. These parameters are used in the proposed topology and conventional topology with one different parameter; the module capacitor size.

The simulation results for the conventional MMC and the proposed MMC are shown in Figure 5.1 respectively. The same amount of input DC voltage requires a larger capacitor size

Simulation Parameter	Value	Unit
Power, P	0.5	MW
Input DC Voltage, V_{DC}	11	kV
Output AC Line Voltage, V_{AC}	4.16	kV
Arm Inductance, L_{arm}	10	mH
Module Capacitor, C^n (Conventional versus Proposed)	100 versus 3	μF
Load Inductance, L_{Load}	5	mH
Load, R_{Load}	36	Ω

Table 5.1: Design parameters used in simulations for conventional and proposed MMCs.

in the conventional topology, in this case, 33 times higher than the proposed design. Note the net arm inductance for the conventional topology and proposed topology are the same. The proposed design distributes this net arm inductance between two connected modules with distribution factors $K^1 : K^2 : K^3 : K^4$ implemented with values of $0.08 : 0.42 : 0.42 : 0.08$ for a three-level ($n = 3$) DC to three phase AC MMC.

The module capacitor size is determined by the ripple voltage of the capacitor, Δv, recall Equation 3.8. The conventional MMC simulation is designed by limiting the submodule voltage ripple, Δv to a maximum of 5%. The conventional module simulated in this case is designed with 3% voltage ripple.

In the last row of Figure 5.1, the averaged capacitor current of the conventional topology and the proposed topology are shown. In the conventional module, the capacitor current is imposed with AC frequency current, recall Equation 3.17, resulting in a periodic averaged capacitor current with frequency of 60 Hz. The capacitor current of the proposed design in the bottom Figure 5.1(b) shows that using a small capacitor size of 3 μF, the averaged current

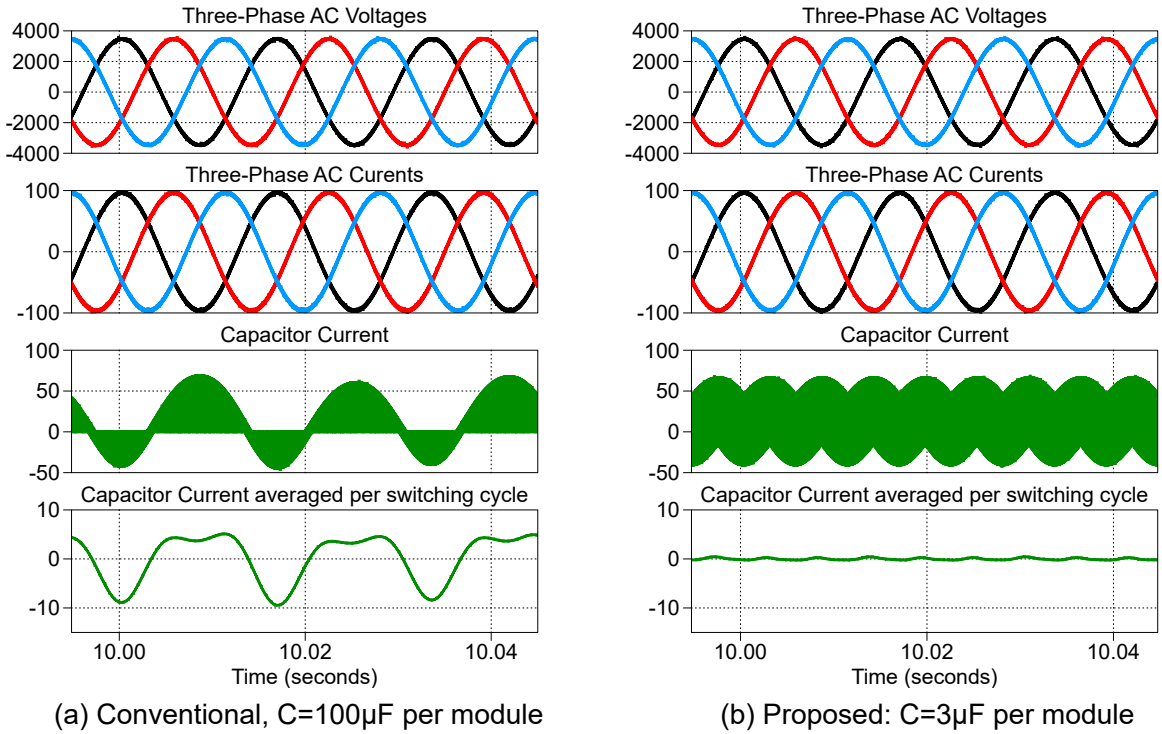


Figure 5.1: Simulation waveforms of the three-phase AC output voltages, three-phase AC output currents, module capacitor current, and module capacitor current averaged over one switching cycle for (a) conventional design with C=100μF and (b) Proposed design with C=3μF.

over one switching cycle is nearly zero and significantly reduces ripple. In comparison to the conventional design, the capacitor averaged current in Figure 5.1(a), with capacitor size of 100 μF, is higher.

5.2 Experimental Results

The proposed topology is verified experimentally using a laboratory-scale prototype, tested at different power levels. The prototype is a three-level DC-to-three-phase AC MMC, meaning the integrated arm has three connected modules with the overall circuit schematic

demonstrated in Figure 3.10. The experiment parameters for prototype testing of the proposed design are shown in Table 5.2. The arm inductance is distributed with distribution factors of $0.17 : 0.25 : 0.41 : 0.17$ in each arm. The prototype setup is shown in Figure 5.2. The collected experimental data include the three phase AC output currents and a module capacitor voltage. The prototype with parameters shown in Table 5.2 was tested at increasing input DC voltage from 10 V_{DC} to 75 V_{DC}.

Experimental Parameter	**Value**	**Unit**
Arm Inductance, L_{arm}	2	mH
Module Capacitor, C^i	3	μF
Load Inductance, L_{Load}	10	μH
Load, R_{Load}	10	Ω

Table 5.2: Experimental parameters used for prototype testing.

The modulation approach is implemented using an FPGA board, outputting 12 SPWM signals to control the switches at a switching frequency of 24.4 kHz. The proposed module in Figure 5.2 is on the purple Printed Circuit Board (PCB). The distributed arm inductance is distributed to $n + 1$ number of inductors, with a three-level ($n = 3$) MMC. There are four inductors in each arm. These inductors are on the green PCBs between the proposed module boards shown in Figure 5.2. A 1 μF thin film module capacitor is on each purple module board. The three capacitors are in parallel in an integrated module for the three-phase, totaling in 3 μF module capacitor.

The experimental results with an input DC voltage of 75 V (100W power) are shown in Figure 5.3. The top plot shows the measured module capacitor voltage with a zoomed-in

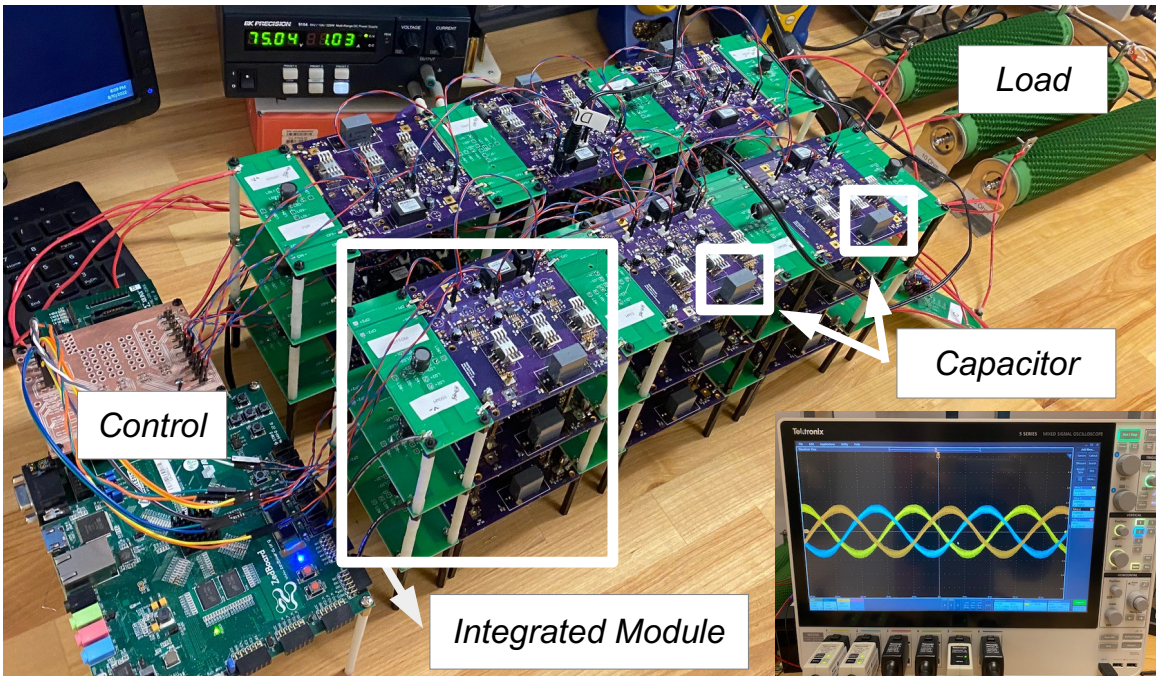


Figure 5.2: A laboratory-scale prototype of proposed DC to three phase AC MMC running a test at 75 V_{DC} (100W). The three phase output AC currents are shown in the lower right corner.

point detailing the module capacitor voltage that follows the switching period, T_{SW}. The bottom plot shows measured output AC currents for the three-phase system

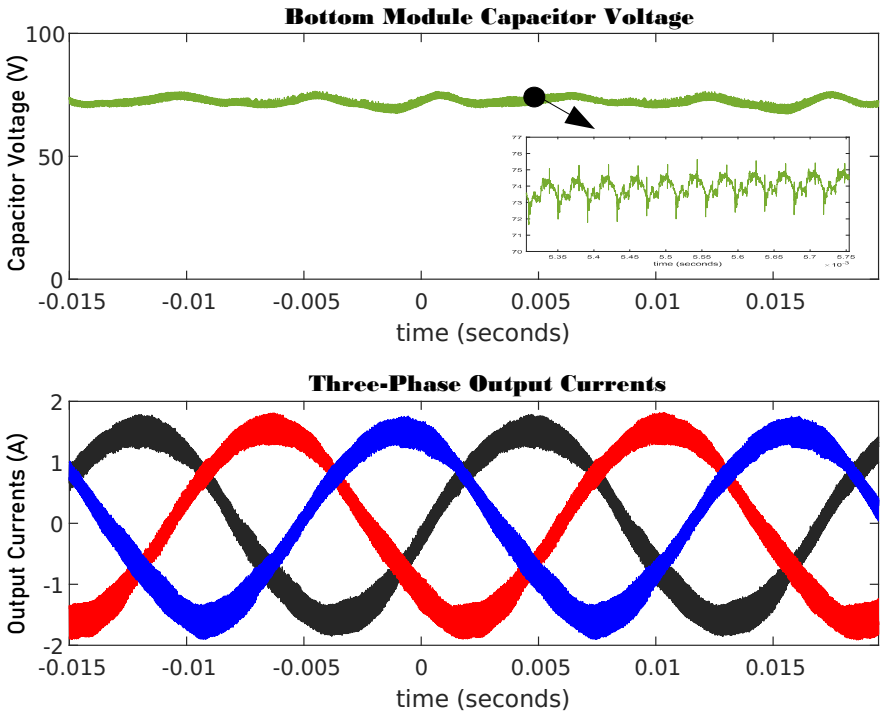


Figure 5.3: Measured module capacitor voltage (top) at 75 V_{DC} input voltage, highlighting voltage ripple based on switching period. Measured three-phase AC currents (bottom) at 75 V_{DC} input voltage.

6 Discussion

The simulation and experimental results verify that the proposed topology reduces module capacitor size requirements which improves power density of the modular power converter. Design tradeoffs include:

- The proposed design reduces the number of module capacitor(s) required per one module; one shared capacitor in the proposed design vs. three independent submodule capacitors in conventional design.
- An integrated module design significantly reduces capacitance size, permitting the use of more reliable and smaller capacitor such as thin film capacitors rather than bulky electrolytic capacitors.
- The number of transistor devices per phase increases in the proposed design; three transistor devices to realize two SPDT switches per phase vs. two transistor devices to implement one SPDT switch in the conventional design.
- The total arm inductance in the conventional and proposed modules are the same. However, a careful distribution of the arm inductance is required in the proposed

module to meet trasnsistor device voltage-blocking capabilities. Arm inductance distribution needs to be optimized to meet positive-voltage blocking capabilities of the commercially-available transistor devices used in this work.

Further research work includes; exploring bidirectional switches application, exploring ways to find optimal values of arm inductance distribution factors, and formulating optimal approach for third harmonic injection to reduce module capacitor ripple voltage. An optimal application of the proposed design is in high power DC to AC conversion with high step-down requirement, for example, a 10 kV-HVDC to 480 V three-phase AC system, due to lower maximum voltage transfer ratio between the DC input and AC output.

7 Conclusion

This thesis work presents an integrated module design applicable for modular DC-to-three-phase AC converters with minimized intermediate storage requirement. The objective of this work is to reduce the intermediate storage size requirement, namely the module capacitor size. Modular power converters typically use electrolytic capacitors to meet high capacitance value requirement. However, electrolytic capacitors are bulky, and less reliable compared with other commercially available capacitors, making it the least reliable component in modular power converters. Reducing the capacitance requirement permits the use of a smaller capacitor, which in turn increases the power density of modular power converters. There are more capacitor options available for lower capacitance values, permitting the use of thin film capacitors, which are more reliable than electrolytic capacitors.

An integrated module design permits a shared module capacitor between a three-phase system, eliminating the single-phase AC power processing requirements on the capacitor that are imposed on conventional designs. In the absence of low-frequency harmonic content, significantly smaller capacitance can be used (only 3 μF versus 100 μF), thus minimizing the intermediate energy storage requirements. Additionally, the capacitor can be sized to reduce switching frequency ripple current rather than AC frequency. Tradeoffs include

the need for a careful distribution of arm inductance in order to meet the voltage blocking capabilities of the transistor devices.

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Appendix : Modulation Code

A.1 FPGA Code Using Vivado Software

SPWM Code: `https://github.com/wiwinhartini/spwm_fpga`