A CMOS 49–63-GHz Phase-Locked Stepped-Chirp FMCW Radar Transceiver

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***Abstract*— A 49–63 GHz phase-locked stepped chirp frequency modulated continuous wave (FMCW) radar transceiver (TRX) in a 22-nm fully depleted silicon on insulator (FD-SOI) process is presented. To achieve the desired large bandwidth (BW), the frequency range is split into two sub-chirps, each controlled by distinct phase-locked loops (PLLs)—a reference PLL and a mixing PLL. This novel dual-PLL architecture facilitates a wide effective BW without the need for designing ultra-wideband TRX blocks. This radar TRX supports both free-running and phase-locked operations. The CMOS chip is co-integrated with linear arrays of series-fed patch antennas for each frequency band. The measured effective isotropic radiated power (EIRP) is 9 dBm with a phase noise (PN) of −101.09 dBc/Hz at 1 MHz offset at 56 GHz. The receiver (RX) achieves a 10-dB noise figure (NF). The radar field measurement demonstrates a maximum distance of 5 m and a range resolution of 1.4 cm.**

***Index Terms*— 60 GHz, frequency modulated continuous wave (FMCW), phase-locked loop (PLL), radar, range resolution, stepped chirp.**

I. Introduction

With the rapid evolution of advanced driver assistance systems (ADASs) [1], [2], Internet of Things (IoT) [3], smart industry [4], [5], and healthcare, the need for frequency-modulated continuous-wave (FMCW) radar in both the unlicensed 60- and 77-GHz band is growing substantially [6], [7], [8]. Emerging applications such as IoT-based local-area sensing call for large-scale deployment of power-efficient, miniaturized radar nodes [9], [10]. These sensors must cover ranges from 10 cm to 50 m and provide fine detection capability characterized by range resolutions [11]. The range of coverage depends on the transmitted power which should be sufficiently high to overcome the propagation loss of the medium (e.g., air) and achieve acceptable receiver (RX) sensitivity, yet remain within the bounds of existing radiation/communication regulations. In addition, these sensors must operate at high frequencies (i.e., small wavelengths) and across broad bandwidths (BWs), as both BW and frequency of operation contribute to resolution.

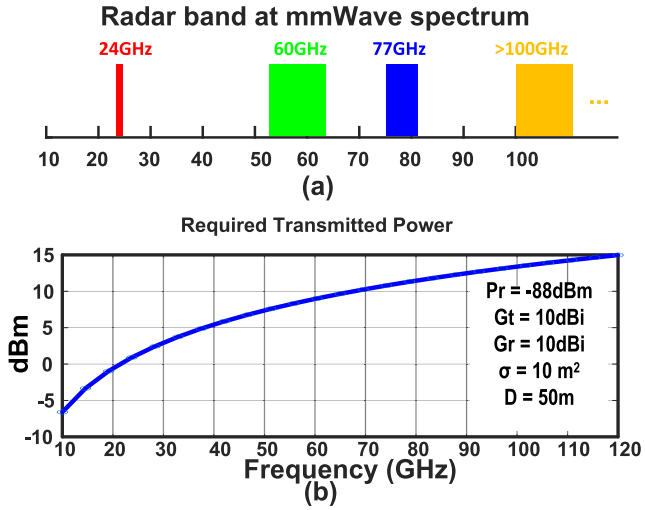

Fig. 1. (a) Radar frequency band at the mm-wave spectrum and (b) received power at 50 m distance versus frequency based on radar Friss equation.

Existing commercial 24-/60-/77-GHz FMCW radar [12], [13], [14], [15], [16] exhibit relatively narrow BWs [see Fig. 1(a)], which inherently limits the range resolution. While operating above 100 GHz [17] facilitates broader BWs for a smaller fractional BW, the power generation efficiency and RX sensitivity are severely degraded, thereby limiting the range. As shown in Fig. 1(b), for an RX sensitivity of −88 dBm, transmitter (TX) and RX antenna gains of 10 dBi and target with a radar cross section (σ) of 10 m^2 located 50 m away, the required transmitted power to produce detectable signals on the RX side based on radar's Friis equation for frequencies above 100 GHz should be higher than 13 dBm [18], [19]. Generating such levels of power in light of severely limited output power available from an MOS device beyond 100 GHz is challenging [20]. Another issue that becomes increasingly more significant at high frequencies is the signal transfer from the TRX chip to the high-gain antenna. In particular, the RF signal transfer to the package antennas encounters increased insertion loss and group delay variation at higher frequencies due to skin effect [21], chip-to-package parasitic impedances [22], and the interconnect dimensions becoming

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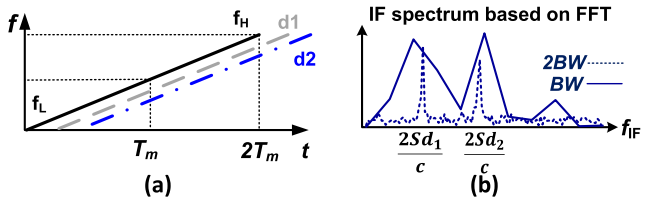

Fig. 2. Relationship between range resolution and synthetic BW. (a) FMCW chirp profile in the time domain. (b) Range resolution comparison using FFT for bandwidths of BW and 2BW.

comparable to the wavelength. For example, a 500-μm wire-bond behaves as a $\lambda/4$ transmission line at 150 GHz.

Rather than increasing the operating frequency to obtain a broader absolute BW, a potential solution involves deploying multiple lower frequency radars, each covering adjacent frequency sub-bands, and combining them to achieve the desired overall BW. However, this approach mandates precise phase and frequency synchronization across the deployed bands, which poses significant challenges and often results in high power consumption. This work presents a stepped chirp-based FMCW radar transceiver (TRX) which consists of two sub-bands, with each covering 7-GHz BW. By splitting the BW into two frequency bands, the wideband design challenges associated with critical components such as the power amplifier (PA), low noise amplifier (LNA), and voltage-controlled oscillator (VCO) are largely mitigated. More importantly, the two bands are phase and frequency synchronized using a low-power, scalable on-chip mechanism inspired by type-II analog phase-locked loops (PLLs), which is essential for the radar's high-resolution performance. The radar TRX chip is co-integrated with series-fed patch antenna arrays through a chip-to-package impedance matching network.

The rest of the article is organized as follows. Section II explains the necessity of widening the BW to enhance range resolution and the operation of the frequency-segmented phase-locked TRX architecture. Section III introduces the design of critical circuit blocks and chip-to-board and board-to-antenna interface design. Section IV demonstrates the TRX major performance measurements and the radar operation verification. Section V concludes the article.

II. System Architecture of Stepped Chirp Radar

Range resolution is a key radar performance metric that defines the minimum distance between two closely spaced targets that can be distinctly identified by the radar in a single chirp interval [23]. The FMCW radar range resolution (RR) is inversely proportional to the chirp BW [11], [24], as illustrated in Fig. 2, i.e., RR $= c/2$BW where c is the speed of light. Therefore, to improve range resolution, an increase in chirp BW is required. A larger BW can: 1) yield a greater frequency separation (Δf) for the same distance resolution (Δd) and 2) allow the same Δf but with a longer observation window for the same Δd. A snapshot of state-of-the-art phase-locked FMCW radars covering 20–140 GHz including this work is summarized in Fig. 3 [25], [26], [27], [28], [29], [30], [31], [32]. Given the constraints on the fractional BW of chirp generation circuits, such as VCOs utilizing varactor tuning, the majority of previous designs operating below 100 GHz have been limited to sub-10-GHz chirp BW. This highlights

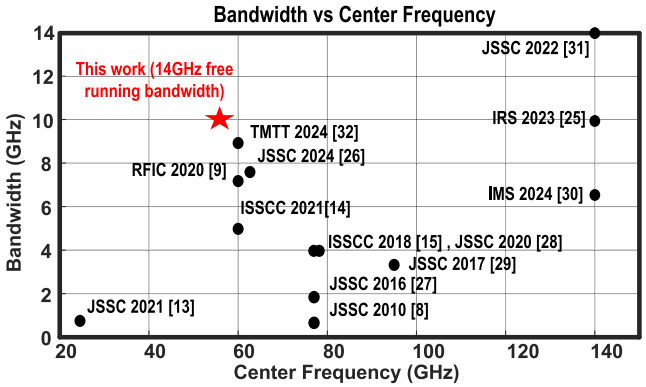

Fig. 3. BW versus center frequency.

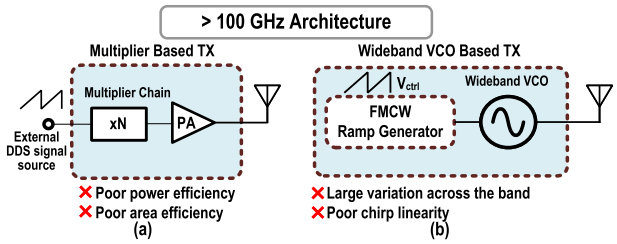

Fig. 4. Above 100-GHz wideband radar TX utilizing (a) multiplier chain and (b) VCO.

the need for innovative frequency synthesis architectures to overcome these BW challenges.

A. Frequency Synthesis Planning

The present implementations of mm-wave radar are mostly centered around two predominant approaches for signal synthesis. To achieve greater BW for range resolution, single-chirp implementations often target operating frequencies above 100 GHz, where radar systems encounter several challenges. As depicted in Fig. 4(a), the first method employs an external FMCW signal generated by a direct digital frequency synthesizer (DDFS), which is subsequently passed through a chain of multipliers and a PA boost the signal's power. This method is inefficient in terms of both area and power consumption due to two main factors: 1) the requirement for additional multiplier stages as the frequency increases owing to challenges in achieving high-frequency DDFS outputs [31] and 2) the reduced gain and efficiency of transistors within the PA as frequency rises. Alternatively, the second method uses wideband VCOs [see Fig. 4(b)], while mitigating some of the issues mentioned in Fig. 4(a). Nonetheless, this approach is not without its drawbacks, including the diminished quality factor of passive components and the augmented intrinsic noise of active devices at higher frequencies. This in turn degrades the oscillator's phase noise (PN), adversely affecting the signal-to-noise ratio (SNR) of the intermediate frequency (IF) signal. In addition, as shown in Fig. 4(b), calibration of the ramp generator to linearize the chirp for VCO-based FMCW radar is necessary to offset the impact of suboptimal K_{VCO} on the chirp's linearity [33].

Addressing the limitations and shortcomings of above 100-GHz configurations in Fig. 4, we explore PLL-based designs that can span below 100 GHz, e.g., a 49–63-GHz frequency

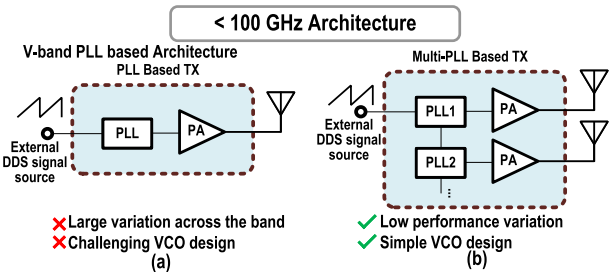

Fig. 5. Below 100-GHz wideband radar TX utilizing (a) one PLL and (b) coupled PLL.

range. Fig. 5 demonstrates two distinct configurations: one that employs a single PLL with wide BW coverage (≥10 GHz), and another that integrates several sub-band PLLs. In Fig. 5(a), it is necessary for the VCO's fractional BW to be accordingly increased, a challenge at mm-wave frequencies predominantly due to the prevailing effect of device parasitics. In Fig. 5(b), segmentation of the frequency band into smaller sub-bands significantly mitigates the design challenges of wideband TRX blocks, such as the VCO, PA, and LNA. This approach lowers PA output power variations, improves the VCO linear tuning range, and reduces the oscillator PN.

It is noted that the design challenge of critical mm-wavefront-end blocks increases substantially with larger BWs mainly due to the limitations on wideband matching. On the radiation side, planar antenna configurations such as series-fed patch antennas, which are currently popular for FMCW radars due to their narrow field-of-view (FoV), can hardly achieve a radiation BW above 10 GHz. This is why despite achieving a total impressive BW of 9 GHz in [32], the design challenges of ensuring all subblocks operate across the same BW result in suboptimal PN and output power compared to [6].

In light of these design challenges, we propose dividing the entire BW into multiple smaller sub-bands, simplifying the design of critical building blocks, such as antennas, for each band. An architecture based on coupled PLLs, shown in Fig. 5(b), provides an effective means of extending the BW while preserving a uniform narrowband chirp profile across various sub-bands. Nevertheless, this approach demands novel synthesizer solutions to reduce power consumption, particularly as the number of PLLs increases.

B. Stepped Chirp TRX Architecture

One solution to divide the BW into smaller sub-bands is the stepped chirp architecture [34]. A stepped-chirp radar sensor can achieve a maximum range resolution of $c/(2\mathrm{BW}_T)$, where BW_T is the total synthetic BW comprised of N subbands with each covering a BW of $\mathrm{BW} = \mathrm{BW}_T/N$. The range resolution associated with BW_T is only obtained if the slopes of chirps corresponding with the sub-bands are identical [35]. This requirement is extremely challenging to meet in practice if the stepped chirps are realized by free-running VCOs, as there is no feedback loop to force the constant frequency difference.

To resolve unwanted variations of free-running oscillators while significantly reducing the power consumption of the radar, we propose a new phase-locked stepped-chirp

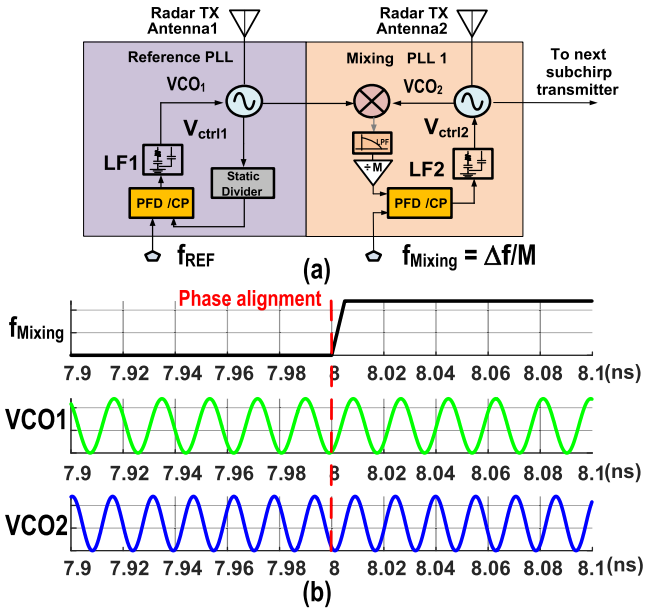

Fig. 6. (a) Simplified TX block diagram and (b) timing diagram of VCO1 and VCO2 with respect to mixing PLL input reference.

generation structure. On the TX side, shown in Fig. 6(a), N sub-bands with frequency coverage of BW and spacing of Δf are realized using a circuit comprising one reference PLL and $N-1$ mixing PLLs. In this structure, the outputs of each pair of adjacent VCOs are fed to a mixer inside a mixing PLL. Under the locking condition, the output frequency of the ith mixing PLL, f_{mix_i} is locked to the mixer's difference frequency component, i.e., $f_{\mathrm{mix}_i} = |f_{\mathrm{osc}_{i+1}} - f_{\mathrm{osc}_i}|$. By placing the mixer inside a PLL [36], the mixing spurs are substantially constrained. Following the phase-locking acquisition, the TX frequency synthesizer in Fig. 6(a) ensures that the frequency difference between two adjacent PLLs is locked to Δf, while also promising the synchronized sweep of their corresponding chirps with respect to the chirp generated by the reference PLL. The linearized loop analysis of a type-II PLL comprising mixers is detailed in [37] and for brevity is not repeated here. The other advantage of this stepped-chirp architecture is the deterministic phase relationship between two adjacent VCOs, as shown in Fig. 6(b), which facilitates the baseband signal stitching, discussed later.

The coupled mixing PLLs offer significant power saving advantage compared to conventional type-II PLLs for the following reason: referring to power consumption breakdown in Fig. 7, an mm-wave type-II PLL consumes a considerable amount of power, as the VCO and divider chain's power consumption becomes increasingly significant with higher frequency/loop-division-ratios. The output frequency of the mixer inside the mixing PLL of the proposed architecture is set to $\Delta f = 7$ GHz rather than the actual sub-band frequency, thereby significantly reducing the loop output frequency to a range manageable by digital dividers. This allows the removal of power-hungry frequency divider chains (e.g., injection-locked frequency dividers (ILFDs) [38] and current-mode logic (CML) dividers [39]) and replacing them with only a low-power mixer inside the loop. Owing to the use of mixing

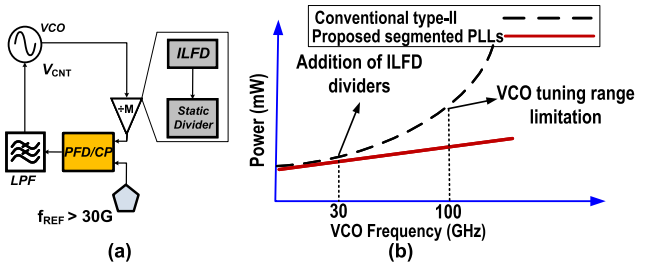

Fig. 7. (a) Conventional type-II PLL architecture with ILFD at above 30 GHz and (b) power saving by adopting mixing PLLs for frequency above 30 GHz instead of type-II PLLs.

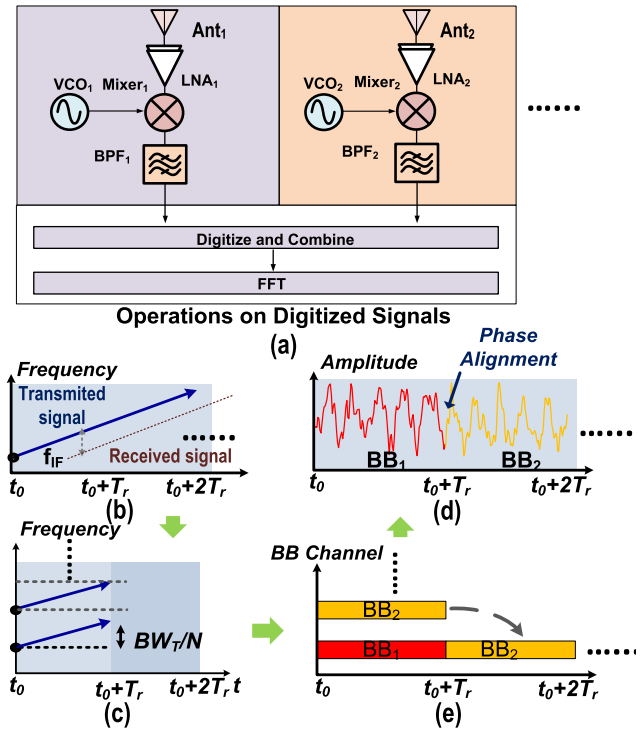

Fig. 8. (a) Proposed stepped-band RX, (b) conventional single-chirp FMCW signal, (c) stepped chirp FMCW signal, (d) stitched baseband signals in the time domain with phase alignment, and (e) resultant combined IF signal.

PLLs, adding more sub-bands to this design leads to a linear increase in power consumption as opposed to the super-linear growth characteristic of type-II PLLs [see Fig. 7(b)].

C. IF Processing and Resolution Enhancement

The proposed RX architecture of the stepped-chirp radar TRX is shown in Fig. 8(a), where the LNA and mixer operate within the BW of each sub-band ($\mathrm{BW} = \mathrm{BW}_T/N$). Therefore, the integrated noise of each sub-band RX is almost $10\log(N)$ smaller than that of the conventional RX ($(N-1)\Delta f + \mathrm{BW}_T$). This smaller BW leads to higher RX sensitivity, which allows for longer ranges of operation. On the other hand, the design of wideband linear LNAs is challenging due to the variations of passive components with wider BW [40]. This issue is resolved in the proposed RX by operating the LNA across the BW of $\mathrm{BW} = \mathrm{BW}_T/N$. Finally, a lower sub-band BW, results in higher achievable SNR than conventional FMCW RXs, thereby relaxing the analog-to-digital converter (ADC) resolution and power consumption, ($P_{\mathrm{ADC}} \propto f_{\mathrm{CLK}} \times 2^{n_{\mathrm{bits}}}$) [41].

As compared with one single-band FMCW radar 1TX–1RX architecture, where a single baseband signal is sampled by one ADC, the stepped chirp architecture has two baseband signals coming from RX_1 and RX_2, which combine in the digital domain to construct the same length of baseband signal as that of the single-chirp architecture. The signal processing is done by stitching different baseband signals [42] in time or frequency domain, as illustrated in Fig. 8(d) and (e). To analytically verify the RX principle of operation, we assume N transmitted chirps correspondings to the sub-bands of the form shown in Fig. 8(c)

$$\mathrm{TX}_i(t) = \cos[2\pi(f_i + St)\cdot t + \theta_i], \quad 0 \le i \le N-1 \tag{1}$$

where f_i is the initial frequency of the ith chirp, $S = \mathrm{BW}/T_r$ is the slope of each chirp, and θ_i is the initial phase of each chirp. Assuming a single target with a reflection coefficient σ_0 at distance R from the radar sensor, the reflected components of the sub-bands can be expressed as follows:

$$\mathrm{RX}_i(t, R) = \sigma_0 \cos\left\{2\pi\left[f_i + S\left(t - \frac{2R}{c}\right)\right]\cdot\left(t - \frac{2R}{c}\right) + \theta_i\right\} \quad 0 \le i \le N-1. \tag{2}$$

The IF signal is obtained by mixing the TX and RX signals and getting the lower frequency part as follows:

$$\mathrm{IF}_i(t, R) = \frac{1}{2}\sigma_0 \cos\left(2\pi S\cdot\frac{2R}{c}\cdot t + 2\pi f_i\frac{2R}{c} - \pi S\left(\frac{2R}{c}\right)^2\right) \quad 0 \le i \le N-1. \tag{3}$$

The term $\pi S((2R/c))^2$ is small enough to be neglected. Therefore, the initial phase of the IF signal is only determined by the initial frequency f_i and round trip time $(2R/c)$. To validate the seamless stitching of the baseband waveform, consider two sub-bands. At the endpoint of the first sub-band ($t = T_r$), the phase of the first baseband is

$$\varphi_{\mathrm{IF},1}(T_r, R) = 2\pi\cdot\frac{2R}{c}\cdot\mathrm{BW} + 2\pi f_1\frac{2R}{c}. \tag{4}$$

At the starting point of the second sub-band ($t = 0$), the phase of the second baseband signal is

$$\varphi_{\mathrm{IF},2}(0, R) = 2\pi f_2\frac{2R}{c}. \tag{5}$$

The phase difference between these two points is given by the following equation:

$$\Delta\varphi_{\mathrm{IF}} = \varphi_{\mathrm{IF},2}(0, R) - \varphi_{\mathrm{IF},1}(T_r, R) = 2\pi\cdot\frac{2R}{c}\cdot\Delta f \tag{6}$$

where $\Delta f = f_2 - f_1$ is the frequency offset between the two sub-bands. In the real implementation, to mitigate frequency pulling, we selected $f_1 = 50$ GHz and $f_1 = 57$ GHz with $\mathrm{BW} = 5$ GHz. The resulting phase difference $\Delta\varphi_{\mathrm{IF}}$ is constant and independent of time. This constancy ensures that the baseband signals of the two sub-bands can be seamlessly aligned by compensating for $\Delta\varphi_{\mathrm{IF}}$.

Moreover, because the chirp slope is identical across sub-bands (enforced by the mixing PLL), the stitched IF signal

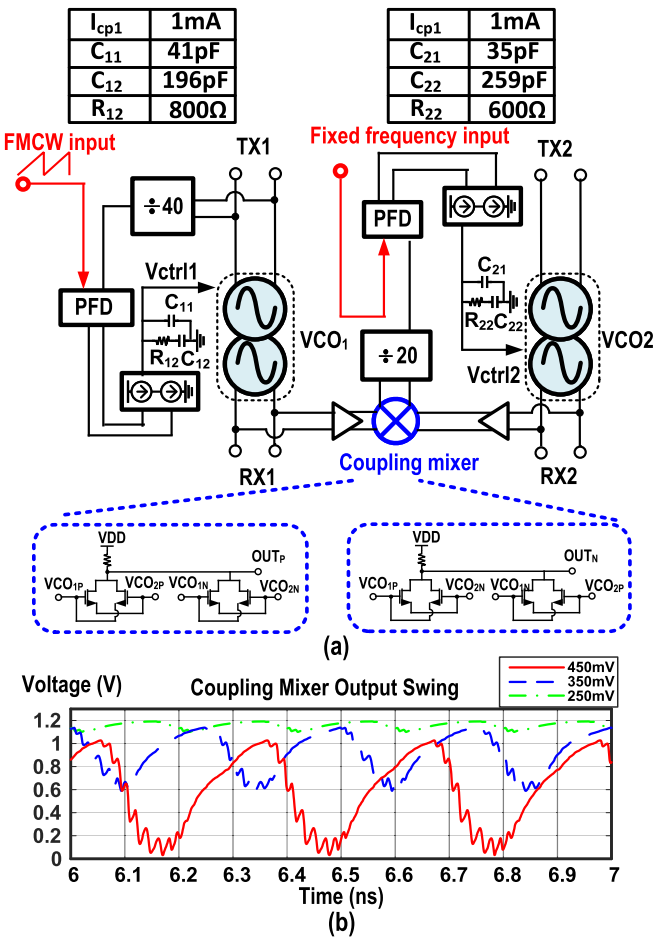

Fig. 9. (a) Frequency synthesizer block diagram with values of *RC* loop filter and the schematic of the fully balanced coupling mixer. (b) Simulated output swing of the coupling mixer for input swings of 250, 350, and 450 mV.

exhibits the same baseband peak as each IF signal. By applying FFT to the stitched baseband, an equivalent BW of $N \cdot \mathrm{BW}$ can be achieved, thus effectively enhancing the radar's range resolution.

III. Circuit Implementation and Package

In this section, we will review the design and simulated performance of the circuit blocks inside the TX and RX, the chip-to-board interface and matching network, and the printed circuit board (PCB) patch antenna arrays.

A. Frequency Synthesizer

The frequency synthesizer block diagram is shown in Fig. 9(a). Both the reference and mixing PLLs are designed with a PFD, a CP, and a second-order loop filter. The outputs from both dual-core VCOs are directed to a low-power cross-connected differential fully balanced mixer block. The mixer's output is subsequently downconverted by a factor of 20. The input swing of the driving signal is crucial for properly driving the coupling mixer. The simulated output swing of the coupling mixer, as shown in Fig. 9(b), demonstrates that a 450 mVpp driving signal is required to achieve a 1 Vpp output swing. To ensure this, we include a common-source (CS) buffer stage between the VCO and coupling mixer,

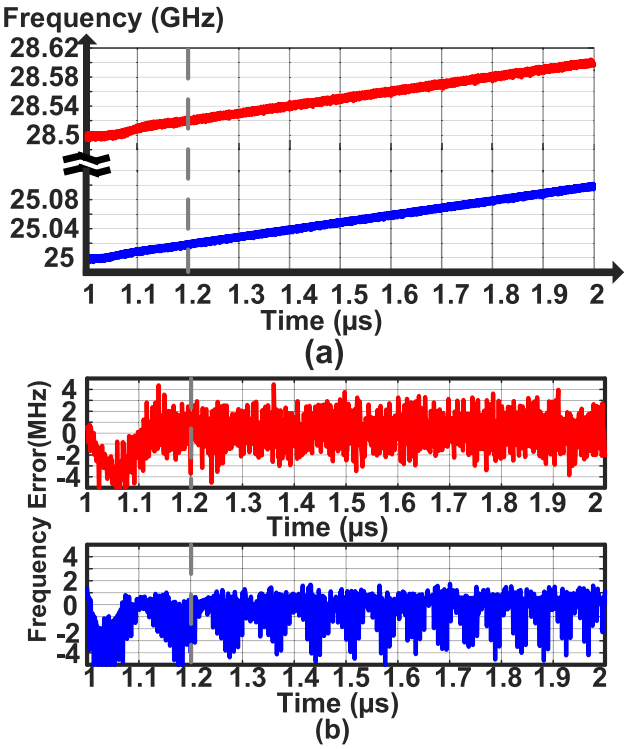

Fig. 10. (a) Simulated chirp profile and (b) simulated frequency error versus ideal chirp.

which guarantees the 450 mV peak-to-peak input swing. The resulting 1 V peak-to-peak output is sufficient to drive the subsequent stage. The values of all the resistors and capacitors used in the second-order loop filter are provided in Fig. 9. The radar's targeted chirp rate is 200 MHz/μs, and the loop BWs of the reference and mixing PLLs are selected to be around 400 and 380 kHz to meet the desired performance. The simulated chirp profile is shown in Fig. 10(a). With the loop filter and charge pump current chosen accordingly, the chirp of the mixing PLL can be locked to that of the reference PLL. The frequency error between the simulated and ideal chirps is presented in Fig. 10(b). Since the modulation of the mixing PLL chirp depends on the reference PLL, the rms frequency error of the mixing PLL is higher than that of the reference PLL. Due to instability at the start of the chirp, the rms frequency error is calculated from 1.2 to 2 μs. The simulated frequency rms of reference PLL and Mixing PLL are 1130 and 1564 kHz, respectively. The simulated power consumption of reference PLL and mixing PLL (excluding the VCOs) is 46.8 and 18.1 mW, respectively.

B. Voltage Controlled Oscillators

The principle of FMCW radar involves mixing the TX signal with a delayed and attenuated version received by the RX. Hence, it is common practice to share the LO signal between the TX and RX. In our design, we implement a dual-core coupled cross-coupled oscillator with source degeneration [43] as the core VCO for each sub-band, as shown in Fig. 11. The use of a dual-core VCO helps reduce signal routing complexity compared to using a single-core VCO combined with buffers and power splitters. In addition, the PN of the

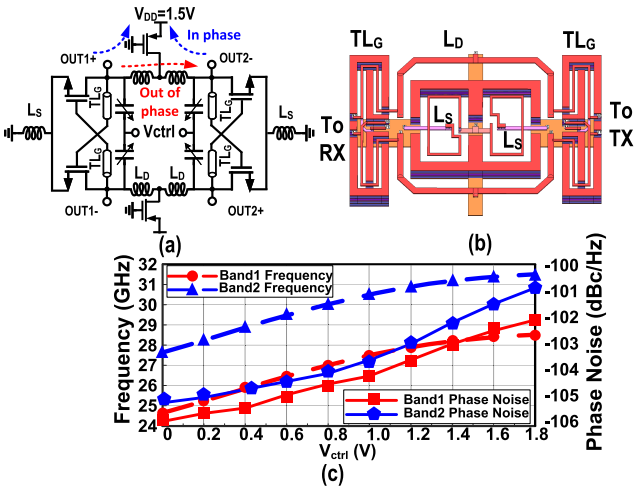

Fig. 11. (a) Dual core VCO schematic, (b) EM structure, and (c) simulated frequency versus V_{ctrl} and PN at 1 MHz offset versus V_{ctrl}.

VCO can be improved by $10\log(2) = 3$ dB by coupling two VCOs [44], [45]. The primary challenge in designing a functional dual-core VCO is the suppression of undesired oscillation modes. As illustrated in Fig. 11(a), when OUT1+ and OUT2− are out of phase, they are in differential mode and the oscillatory current does not pass through the PMOS transistors connected to V_{DD}. Conversely, if OUT1+ and OUT2− are in phase (common mode operation), the current flows through the PMOS devices. In this case, the PMOS devices, with their gates grounded and operating in the triode region, act as lossy resistors that degrade the Q-factor of the LC tank. As a result, the common-mode oscillation is eliminated, allowing only the differential mode to persist.

Compared to conventional cross-coupled VCO, a short T-line is added between the gate and the drain to further boost the voltage swing at the transistor's gate [43]. A thick-oxide transistor is chosen to allow a gate voltage swing of up to 2.4 V ($2V_{\text{DD}}$), which contributes to larger voltage swings for better PN performance, while reducing flicker noise due to the larger gate area ($W \times L$). The layout of each VCO is simulated with EM solvers to capture the coupling effect among the lines and inductors [see Fig. 11(b)]. Post-layout simulation results showing the frequency tuning range and PN characteristics of each sub-band VCO are shown in Fig. 11(c).

C. Doubler and PA

In this design, we adopt a superharmonic configuration where the radiated frequency is twice that of the VCO oscillation frequency in each sub-band. A push-push frequency doubler in Fig. 12(a) is adopted to upconvert the VCO signal, which is followed by a two-stage transformer-coupled differential PA [46], [47]. Since we use the differential signaling, the mutual coupling capacitors only help with differential mode stability [48]. A 4-kΩ resistor R_c is added at each gate bias dc node to suppress the common-mode oscillations.

For the first sub-band, the frequency doubler provides an output power of −5 dBm with an output impedance of $(20 + j10)$ Ω. A thick gate-oxide transistor with a 70-nm gate length is chosen for the PA to support a higher

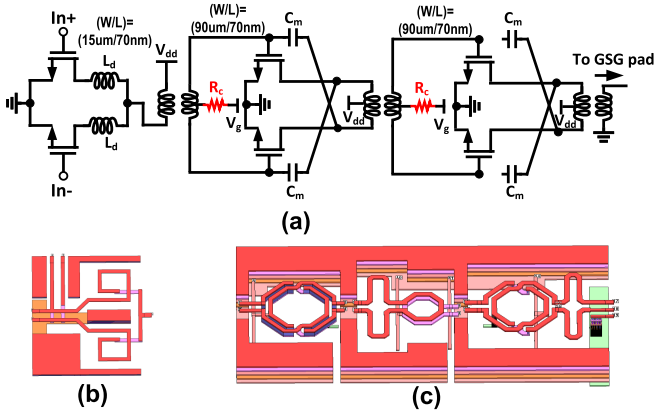

Fig. 12. (a) Schematic of frequency doubler and PA, EM structure of (b) doubler and (c) PA.

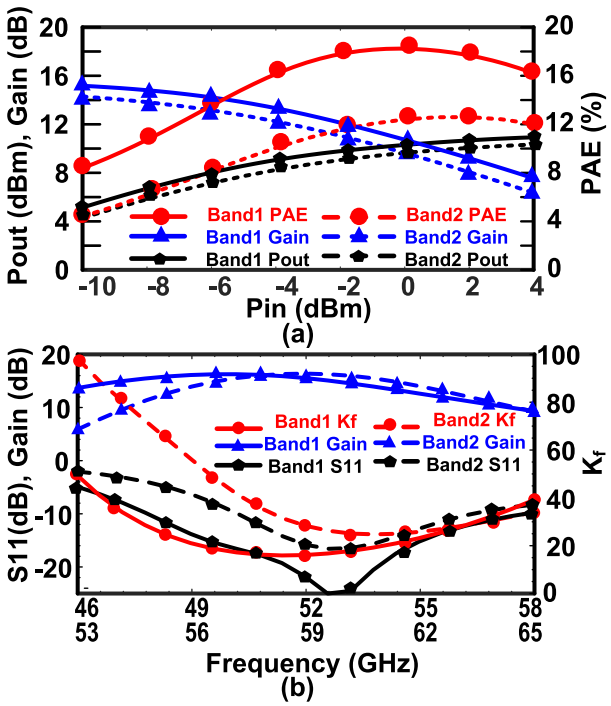

Fig. 13. PA simulation results for band1 and band2 (a) P_{out}, gain and PAE and (b) S_{11}, S_{21}, and K_f.

supply voltage of 1.2 V, enhancing P_{sat}. The transistor widths for both stages are set at 30 μm × 3 for both stages based on the power and gain requirements. Impedance matching between the frequency doubler and PA input is accomplished using an input balun, while the interstage matching is achieved through a stacked transformer. To further enhance impedance matching across a 12-GHz BW, an additional transmission line is incorporated within the matching network. Finally, the output of the second stage is matched to 50-Ω load impedance through the output balun. Both the stages employ the over-neutralization technique [49] to bring the device stability factor above $K_f = 1$, while increasing the gain. The EM-simulated layouts of the doubler and PA are shown in Fig. 12(b) and (c). The insertion loss of the input balun, interstage matching, and output balun varies between 1.2 and 1.8 dB. The S-parameter simulation results are shown in Fig. 13(a) where 10 dB input-return is achieved across 46–58 GHz with a

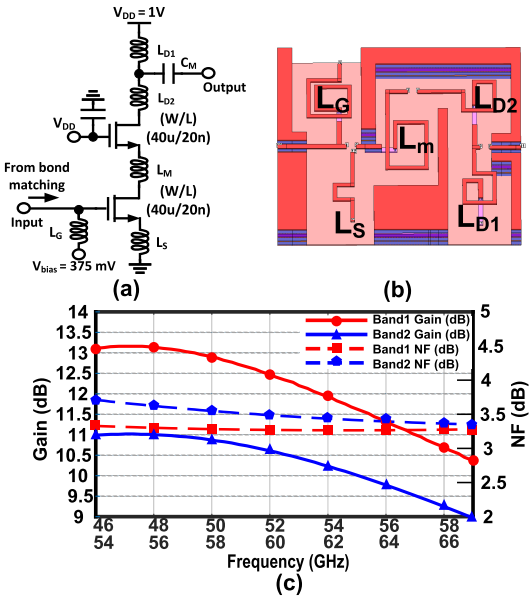

Fig. 14. (a) LNA schematic, (b) LNA EM structure, and (c) simulated conversion gain and NF for the low-frequency band and high-frequency band.

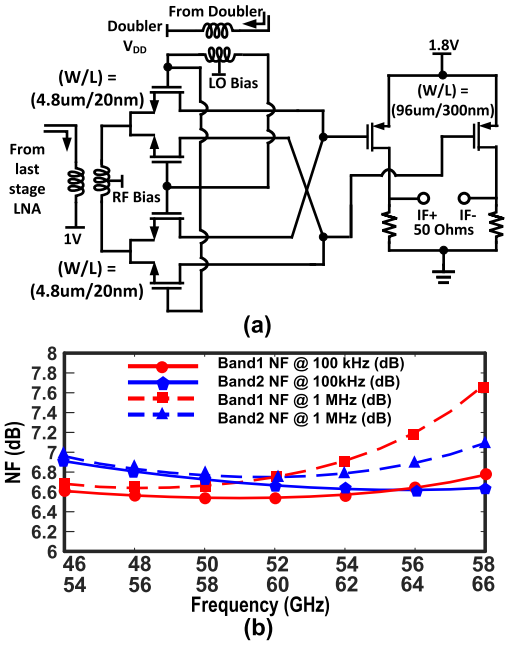

Fig. 15. (a) Passive mixer and buffer schematic and (b) simulated NF at 100 kHz and 1 MHz offset.

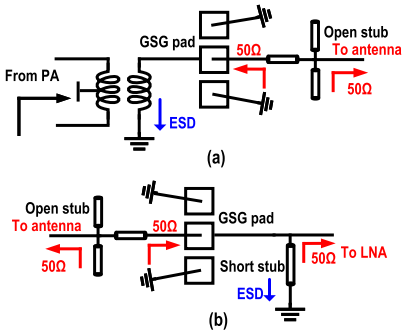

Fig. 16. Illustration of (a) TX packaging matching and (b) RX packaging matching.

peak S_{21} of 16.3 dB and K_f of more than 24.7. The simulation plots for the output power (P_{out}), large signal gain, and power added efficiency PAE are shown in Fig. 13(b). A 6.75-dBm output power, 17.7% of PAE, and a large signal gain of 11.87 dB is attained for an input power of −5 dBm at 53 GHz.

The PA for the second sub-band, covering the 56–63-GHz frequency range, uses the same topology and device dimensions as the first band. The small signal S-parameter simulation results are presented in Fig. 13(a), showing a S_{11} better than rc10 dB, a S_{21} of 14.5–15.8 dB, a K_f of greater than 15.9 across the designed band. The large signal simulation results, shown in Fig. 13(b), indicate that for the doubler's output power of −5 dBm and the output impedance of $(20 + j20)$ Ω, the PA delivers an output power of 6 dBm, a PAE of 11.5%, and a large-signal gain of 11 dB at 60 GHz.

D. LNA and Mixer

A three-stage single-ended cascode LNA is employed in this design, where the first-stage schematic is shown in Fig. 14(a). The LNA's EM layout is shown in Fig. 14(b) where inductors are co-simulated to capture any unwanted mutual coupling. The input transistor is biased at optimum dc current to achieve a lower NF_{min}. An inductor L_M is inserted between CS and common-gate devices for a better power and noise matching [50], [51]. The EM-simulated layout of the LNA is shown in Fig. 14(b) and the simulated LNA single-stage gain and noise figure (NF) for each sub-band are shown in Fig. 14(c).

Following the LNA, a double-balanced passive mixer [see Fig. 15(a)] is deployed. Since no dc current passes through the switching transistor [52], [53], [54], the flicker noise from these switching transistors is substantially reduced. In addition, the mixer is connected to a large PMOS transistor ($W/L = 96$ μm/300 nm), introducing a large capacitive load to reduce the impact of flicker noise on the radar operation. In this design, flicker noise suppression is critical since the baseband range of interest is designed to be below 20 MHz. The total simulated NF at both 100 kHz and 1 MHz offset frequencies for both sub-bands is shown in Fig. 15(b). The NF at 100 kHz offset is just around 1 dB higher than that at 1 MHz, highlighting the advantage of the passive mixer and large capacitive load.

E. Wirebond Matching and Antenna Design

At higher operation frequencies, the design of the chip-to-board interface becomes crucial in minimizing losses between the PA and antenna, ensuring maximum radiated power. Wirebonding, while low cost and highly durable for low-frequency packaging, suffers from large parasitic inductance that limits the BW. This limitation highlights the importance of the stepped chirp architecture, wherein each channel only needs to cover 7 GHz.

For matching on the chip side, electrostatic discharge (ESD) protection at the pad interface must be considered. On the TX side, a balun is used to convert the differential signal to single-ended. The short-to-ground inductor can serve as the ESD protection element while also matching the impedance at the ground-signal-ground (GSG) pad to 50 Ω, as illustrated

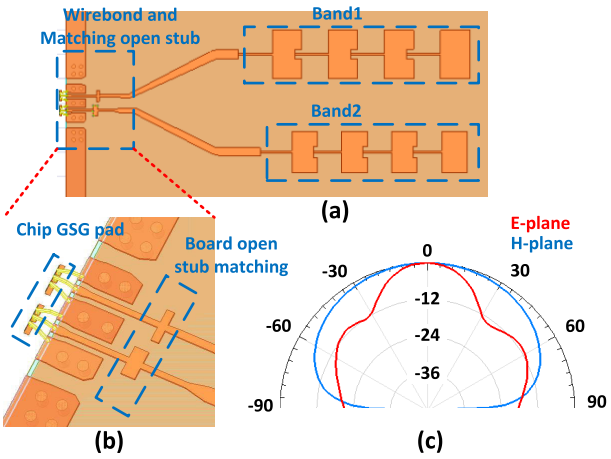

Fig. 17. (a) Top view of antennas and (b) simulated radiation pattern.

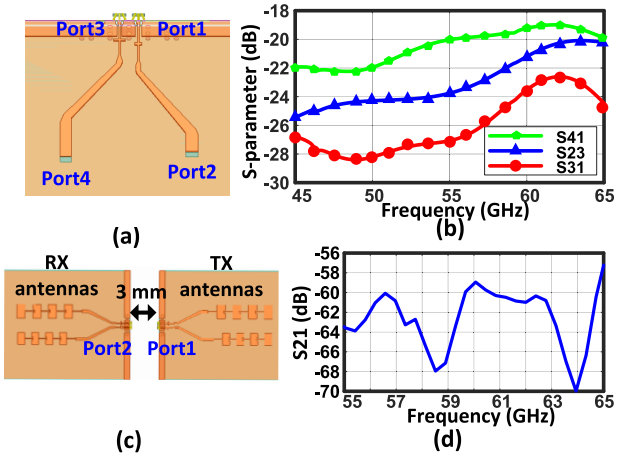

Fig. 18. (a) EM simulation testbench for characterizing isolation between adjacent channels, (b) simulated S_{41}, S_{23}, and S_{31}, (c) EM simulated TX to RX leakage characterization, and (d) simulated S_{21} representing TX to RX leakage.

in Fig. 16(a). An open stub is added on the board to cancel out the parasitic effects introduced by the wirebond and transform the impedance back to 50 Ω for the antenna. The RX side matching is similar to the TX side, as shown in Fig. 16(b). However, since the LNA is single-ended, a short stub is used to match the parasitic capacitance of the GSG pad. The HFSS view of chip-to-antenna interface is shown in Fig. 17(a), with a zoomed-in view of the interface shown in Fig. 17(b). Each sub-band employs a series-fed linear array of microstrip patch antennas. Patch antennas are commonly used in FMCW radars due to their compatibility with planar feed structures and their ability to provide broadside radiation [14], [55]. HFSS simulations indicate that the insertion loss of the interface network stays below 1.5 dB across both frequency bands, justifying the use of a wirebond for the interface. The simulated radiation pattern of the antennas is shown in Fig. 17(c), where more than 7 dBi of realized gain is achieved for each sub-band antenna array. Two-band series-fed patch antennas are designed to balance between the FoV and directivity, e.g., wide beamwidth for H-plane and narrow beamwidth for E-plane, as shown in Fig. 17(c).

The coupling between two adjacent bands was simulated by replacing the series-fed patch antenna with a lumped port, as illustrated in Fig. 18(a). The electromagnetic (EM) simulation results, shown in Fig. 18(b), indicate attenuations exceeding 19 dB. The TX to RX leakage due to the standalone antenna was also simulated, as depicted in Fig. 18(c). The simulation setup places the two antenna boards at a separation distance of 3 mm to accommodate the chip. The isolation between TX and RX is below −58 dB across the 55–65 GHz-frequency range as shown in Fig. 18(d). It should be noted that this simulation only characterizes the coupling between the two antennas due to radiation and does not account for on-chip TX-to-RX leakage. Two other mechanisms in this design provide more isolation between adjacent bands for both TX and RX antennas: 1) the bandpass profile of the antennas, each centered at its designated sub-band frequency and 2) the input matching network comprising the chip-to-board interface and the LNA input matching, designed to capture only the target sub-band BW.

IV. Measurement Results

The complete circuit block diagram of the CMOS TRX excluding the antenna and interface is shown in Fig. 19. Shown in Fig. 20, the proposed radar TRX was fabricated in 22-nm fully depleted silicon on insulator (FD-SOI) CMOS, occupying 4.5 mm^2 of die area including pads. The TX and RX antenna arrays, shown in Fig. 21(a), were fabricated using Rogers 4003C. The two dummy antennas, positioned at the top and bottom, were added to mitigate process variations caused by the bending of the Rogers material [14]. Each linear-fed antenna array can achieve up to 8% radiation BW. As shown in Fig. 21(b), the antenna board and chip were glued on top of the platform FR-4 PCB, which also included the dc regulators and PLL input signal. To examine the operation of the proposed radar, three separate types of measurements were conducted: 1) stand-alone TX; 2) stand-alone RX; and 3) radar TRX measurements. In what follows, the specific measurements for each of these tests are provided and explained.

A. TX Measurements

The TX/PLL measurement setup is shown in Fig. 22. To measure the radiation pattern of the TX antennas, the chip was mounted on a rotational optical stage and the diagonal horn antenna was kept still (see Fig. 23). Both E-plane and H-plane measurements of the radiation pattern were conducted for both frequency bands using this technique and the results are provided in Fig. 24. Both antenna arrays achieve more than 6.5 dBi of measured realized gain.

Wireless testing was performed at distances exceeding 15 cm, beyond the Fraunhofer distance, to evaluate frequency and spectrum performance. The received signal was collected using a diagonal horn antenna, and the effective isotropic radiated power (EIRP) was measured with a power sensor and power meter. For PN and spectral measurements, the received signal was fed to a spectrum analyzer, with measurements taken in both free-running and phase-locked modes. In phase-locked mode, a 175 MHz external reference was injected into the mixing PLL, while a ramp input signal between 625–687.5 MHz was applied to the reference PLL.

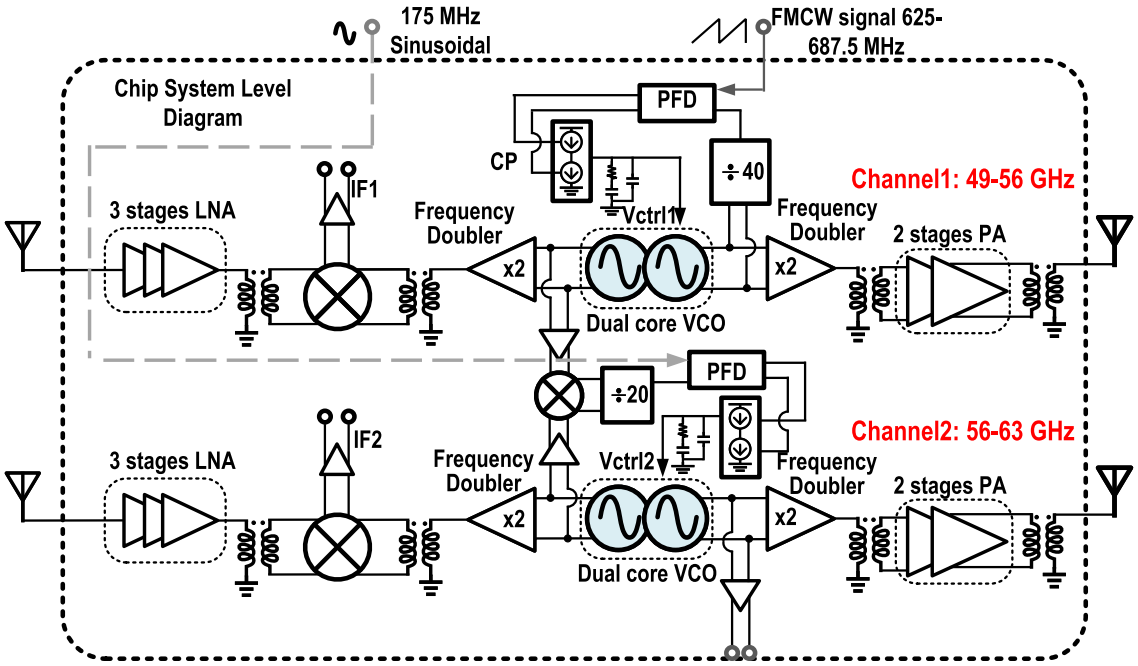

Fig. 19. Detailed TRX block diagram.

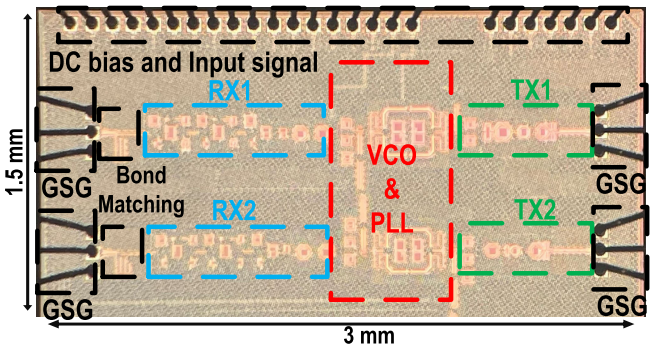

Fig. 20. Chip microphoto.

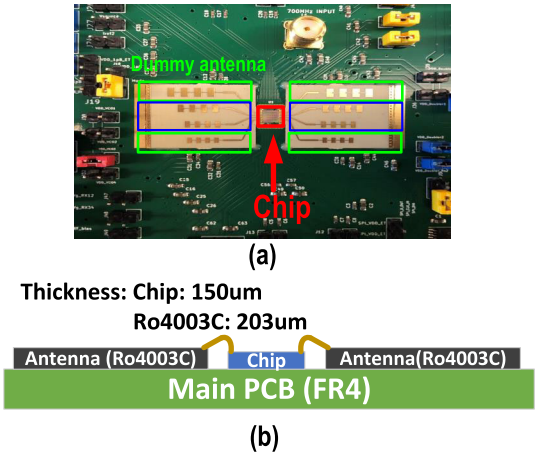

Fig. 21. Board design. (a) Top view and (b) cross section view.

The far-field EIRP measurements were repeated for various distances, and are shown in Fig. 25(a), where a close match between the received power with that estimated by the

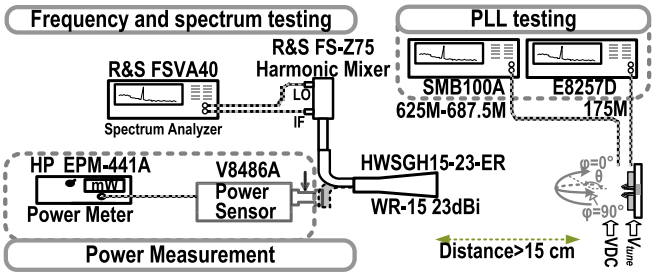

Fig. 22. TX and PLL measurement setup.

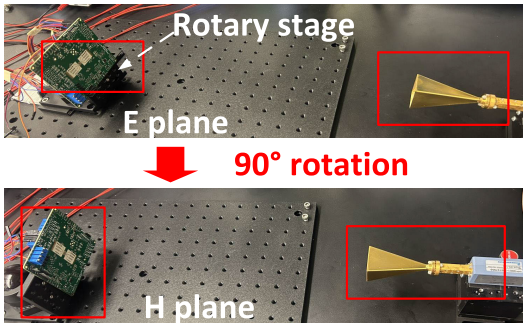

Fig. 23. Antenna pattern measurement for both E-plane and H-plane.

Friis equation [18] are observed. The peak EIRP is above 9 dBm for the low-frequency band and above 8 dBm for the high-frequency band. The power variations across the two sub-bands are attributed to the frequency-band mismatch between the antenna and PA as well as 3-dB loss for deviated PA output load impedance due to process variations and shifts in operation frequency.

For spectral measurements, two separate sets of measurements were conducted for the free-running and phase-locked

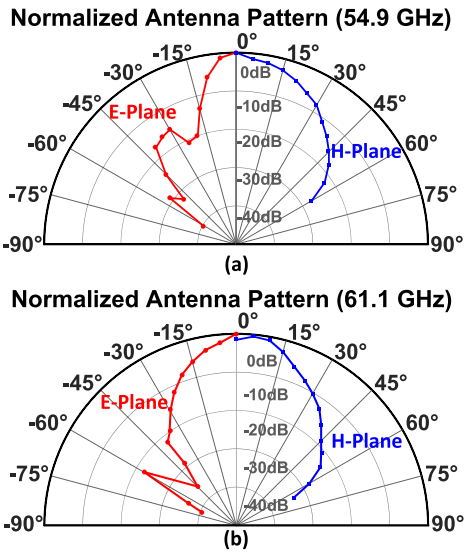

Fig. 24. Measured normalized antenna pattern at (a) 54.9 GHz (low-frequency band) and (b) 61.1 GHz (high-frequency band).

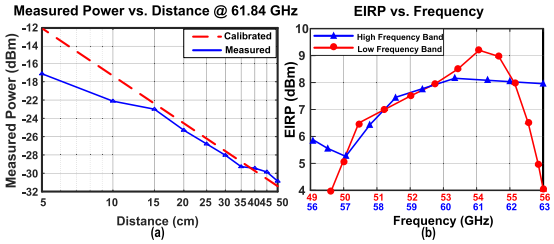

Fig. 25. (a) Close match of power profile with Friis formula at 61.84 GHz. (b) Measured EIRP from 49 to 63 GHz.

operations. On the TX side, the BW of free-running and phase-locked operation and the corresponding PN profiles were measured, as shown in Figs. 26–28, respectively. Each sub-band achieves close to 7 GHz of free-running BW in Fig. 26. However, the preferred mode of operation for this radar is the phase-locking mode, the frequency separation between the two sub-bands is precisely controlled. This is demonstrated in Fig. 27 where the external input to the mixing PLL sets Δf to 7.5 and 7 GHz for the respective scenarios shown in Fig. 27. The two pairs of spurs introduced by the input signals do not impair radar operation, since their spacing ($\Delta f/40$) exceeds the 20-MHz IF BW of this radar, with all the spurs occurring at multiples of $\Delta f/40$. According to the measurement results, the TX can achieve a phase-locked radiation BW of 10 GHz. The smaller BW of phase-locked mode compared to the free-running scenario is attributed to the PLL loop BW, which limits the frequency tuning for stable loop operations. PN measurements at different spot frequencies under phase-locked operation are shown in Fig. 28. The PN at 1-MHz offset is -96.39 and -101.7 at 52.16 and 56.01 GHz, respectively. The locked loop BW varies between 200 and 500 kHz across all these samples.

To demonstrate the simultaneous phase-locked operation of the radar for the two adjacent sub-bands, multiple dual-band measurements were conducted where the reference and mixing PLLs were enabled for variable BW associated with each sub-band. Three narrow-band operation scenarios (BW of each

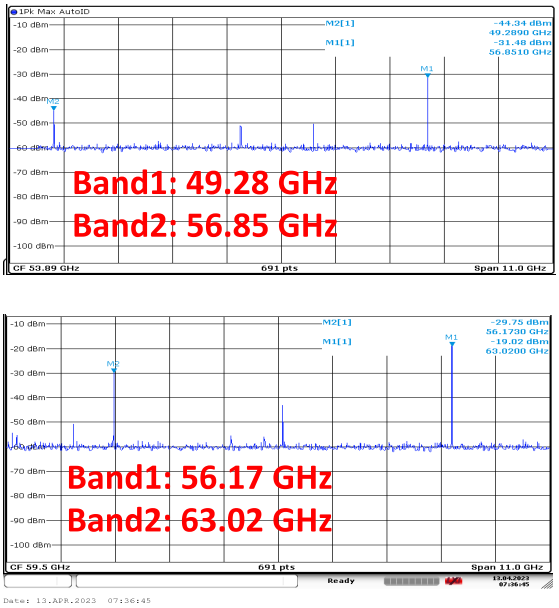

Fig. 26. Free running operation at minimum and maximum frequencies.

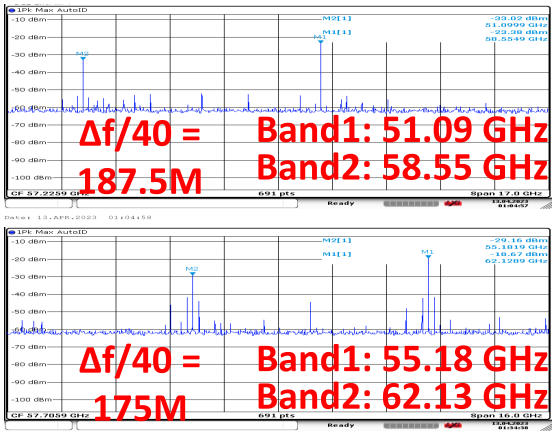

Fig. 27. Phase-locked operation at two distinct PLL reference frequencies.

band below 1.4 GHz), medium resolution (combined BW of 8.2 GHz), and high-resolution (combined BW of 10 GHz) were captured, and the corresponding spectrums are shown in Fig. 29. An important feature of this radar is the similar output power profiles of the two sub-bands under various BWs, enabling adjustable range resolution to suit different applications.

A chirp profile measurement was carried out using the measurement setup in Fig. 30(a), where the signal was down-converted using an R&S FS-Z75 and analyzed on an R&S RTP164B with VSA software. The setup block diagram is shown in Fig. 30(b). The measured dual-band chirp profiles under locking conditions are presented in Fig. 31(a) and (b) for modulation BWs of 200 MHz and 1 GHz per sub-band, respectively. The measured rms frequency errors for a 200 MHz modulation BW in the low and high-frequency sub-bands were 716 kHz and 1.844 MHz, respectively. At a 1-GHz modulation BW, the measured errors increased to 1.367 and 2.664 MHz in the low and high-frequency sub-bands, respectively.

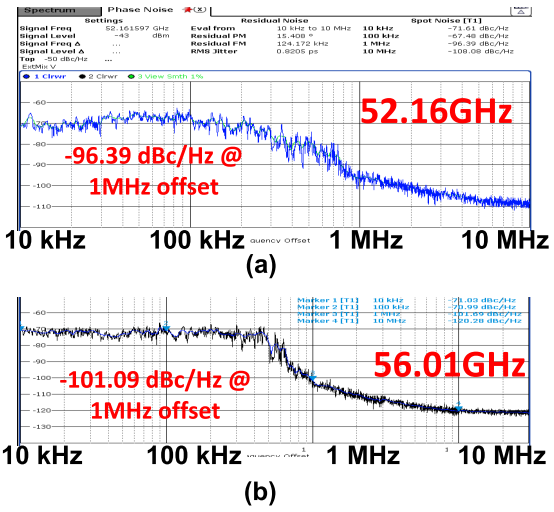

Fig. 28. Measured phase-locked PN profile at 52.16 and 56.01 GHz.

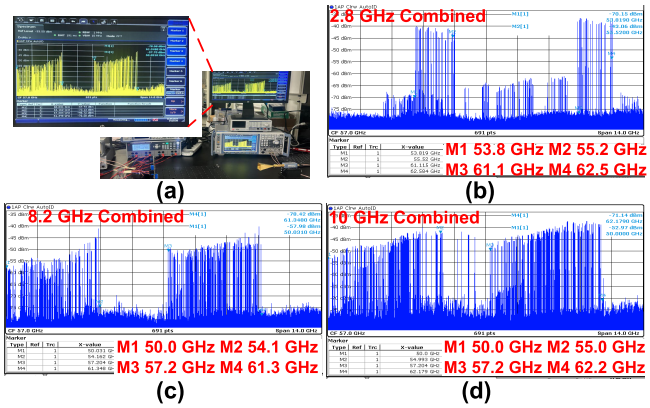

Fig. 29. (a) Dual band operation measurement setup, (b) 2.8-GHz BW, (c) 8.2-GHz BW, and (d) 10-GHz BW.

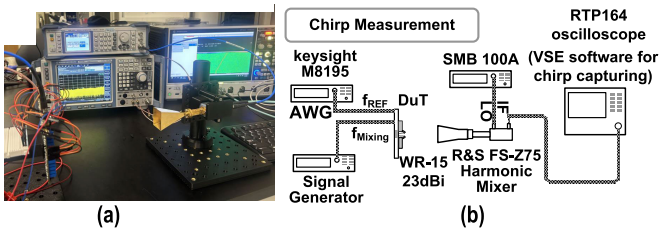

Fig. 30. (a) Chirp measurement setup using an oscilloscope. (b) Block diagram of the measurement setup.

B. RX Measurements

The RX measurement setup utilizing an external signal generator is shown in Fig. 32. The objective of this measurement is to evaluate the RX baseband signal by positioning the chip in the far-field of the diagonal horn antenna and receiving signals at different distances to induce shifts in the resultant IF signal. The IF spectrum associated with this measurement is shown in Fig. 33 where two peaks at 2 and 10 MHz were obtained by changing the distance between the horn antenna and chip. Both measurements indicate 30-dB SNR. The RX P1dB measurement was performed using a probe landing setup, with the input power adjusted through an attenuator, as illustrated in Fig. 32 (bottom). From the measured output power versus input power characteristics shown in Fig. 34, the RX 1-dB compression point (P1dB) is estimated to be approximately −33 dBm.

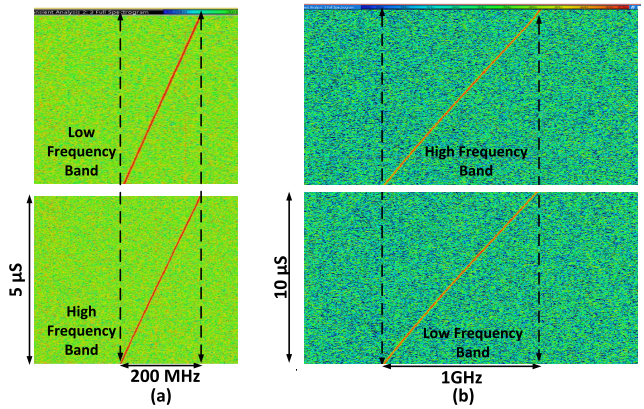

Fig. 31. Dual-band chirp operation for (a) 200-MHz BW and (b) 1-GHz BW per band.

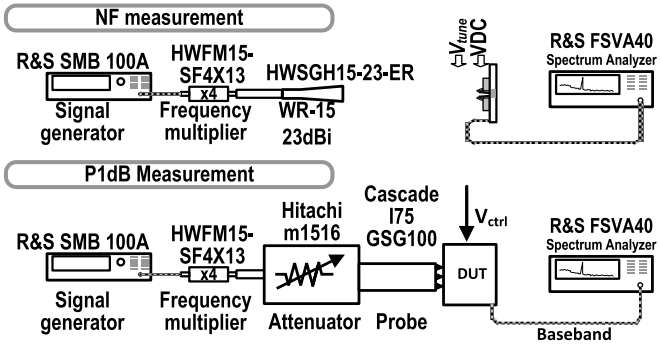

Fig. 32. Measurement setup of RX NF (top) and P1dB (bottom).

Fig. 33. RX baseband fft spectrum with a peak at 2 and 10 MHz.

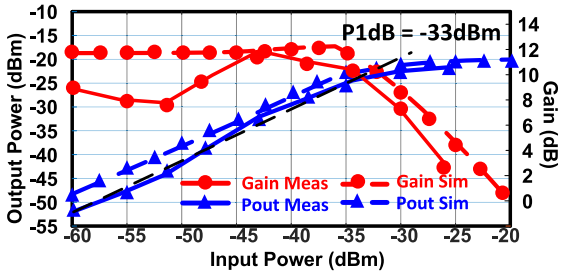

Fig. 34. Simulation and measurement results of RX Gain and P_{out} versus P_{in}.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS ARTS

	This work	[13]	[56]	[57]	[58]	[26]	[32]	[8]
Process	22nm FD-SOI	45nm CMOS	350nm SiGe	130nm SiGe	28nm CMOS	40nm CMOS	22nm FD-SOI	28nm CMOS
Phase Locked	Yes	Yes	No	No	No	Yes	Yes	Yes
N_{RX}/N_{TX}	2/2	4/3	4/2	1/1	3/2	2/2	2/2	1/1
Frequency [GHz]	49-63	57-64	57-64	58.3-63.9	57-64	54-69	57-66	57-66
Architecture	Coupled PLL	PLL	VCO	VCO	VCO	Cascaded-PLL	ADPLL	PLL
PN [dBc/Hz]@1MHz	-101.7	-93	-105	-	-99.4	-93.3	-73	-92.9
Bandwidth	14† 10†	4	-	5.6	9	7.2	9	7.2
TX P_{out} [dBm]	6	12.1	4(P_{sat})	6.4	10(P_{sat})	12.8(P_{sat})	1	8.1
Antenna gain [dB]	7‡	-	-	-	-	-	-	-
RX NF [dB]	10	12.5	9.5	-	12	10	30	10.5
RX Gain [dB]	20	-	19	-	77	20-87^	6	46
RX P1dB [dBm]	-33	-10/-14	-8.5	-8.1	-12	-11	-	-43 to -33
P_{dc} [mW]	400	3500	990	520	920	695	68◊	62
Area [mm^2]	4.5	-	20.25	1.03*	7.45	9.9	1.25	4.13

† 14 GHz free running bandwidth and 10GHz phase locked bandwidth
‡ Realized gain including matching structure
* TX and RX share same antenna
^ including basedband amplifier
◊ not including basedband amplifier and digital loop filter

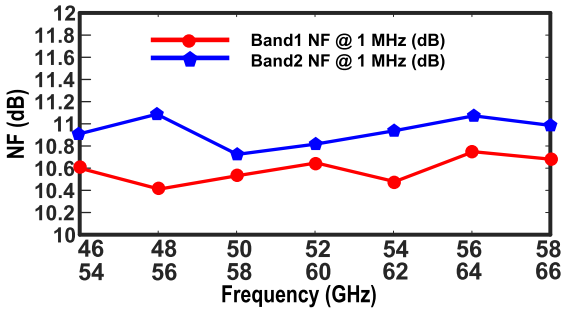

Fig. 35. Estimated NF measurement from radiation-based setup.

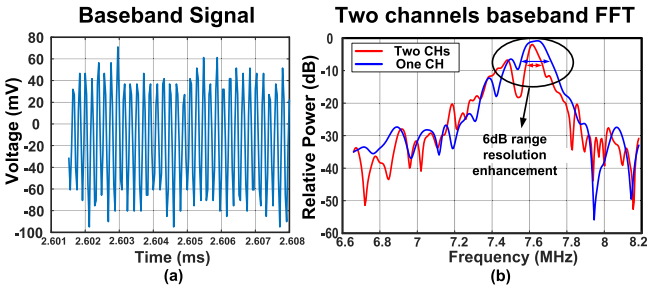

Fig. 36. Enhancement of range resolution by applying FFT on the combined IF signal of the two sub-bands. (a) Baseband time-domain signal from radar field measurement. (b) Enhanced range resolution achieved by applying FFT on the combined IF signal from the two subbands.

The key advantage of the phase-locked stepped chirp architecture lies in its ability to enhance resolution by integrating multiple sub-bands. To demonstrate this feature, a radar field measurement was performed at a distance of 50 cm, and the IF signals from both sub-bands were extracted separately. The time-domain IF signals were then combined, as shown in Fig. 36(a). The FFT of the combined signal, shown in Fig. 36(b), reveals a significant enhancement of range resolution where closely spaced peaks become clearly distinguishable. For this measurement, the range resolution of each sub-band was 28 mm, and for the combined signals, the range resolution was enhanced to the finer value of 14 mm.

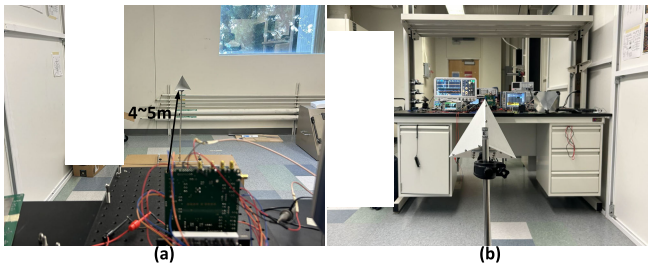

Fig. 37. Radar field measurement with corner reflector object. (a) Radar field measurement taken from the chip side. (b) Radar field measurement taken from the object side.

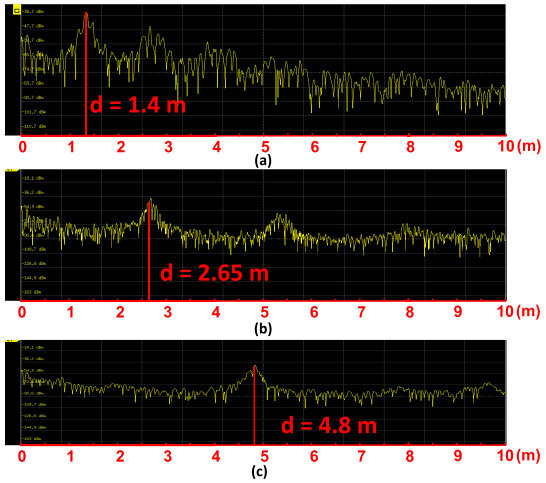

Fig. 38. Radar field measurement at (a) 1.4, (b) 2.65, and (c) 4.8 m.

C. Radar Field Measurements

Various field measurements of the radar are conducted at multiple distances between the radar TRX and a reflector

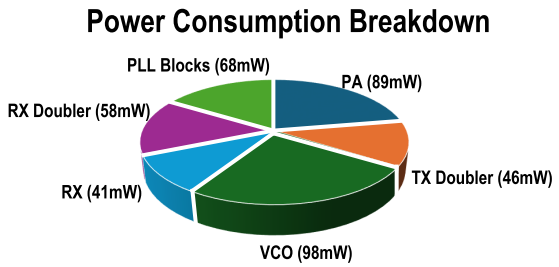

Fig. 39. Measured power consumption breakdown.

object. As shown in Fig. 37, a corner reflector object is placed at incremental distances ranging from 0.5 to 5 m.

The range measurements of the radar for these different range scenarios are shown in Fig. 38. It is observed that for all the measurements, the radar maintains an IF SNR above 16 dB translating to 10 dB of NF_{SSB} for the RX chain. These measurements were conducted at room temperature and with no aid from culminating Teflon lenses or silicon lenses to improve the EIRP of the TX.

Fig. 39 summarizes the measured power breakdown of the circuit blocks in the TX and RX. The total power consumption of this two-band phase-locked radar TRX is 400 mW, significantly lower compared to the prior art. Table I compares the measurement results with the prior art. This work outperforms the radars in the same frequency range in terms of PN, phase-locked BW, and power consumption. This design demonstrates the first phase-locked stepped chirp radar with more than 10-GHz synthetic BW, and a few meters detectable range.

V. Conclusion

In this article, a fully integrated CMOS-based phase-locked stepped chirp radar TRX at 49–63 GHz was presented. The TX side employed a novel PLL scheme which reduced the power consumption and the necessary division ratio compared to conventional type-II PLLs. The RX side incorporated frequency-segmented narrow-band RXs which are combined in the IF domain to enhance the range resolution. The phase-locked BW of this radar was more than 10 GHz and achieved a peak EIRP of 9 dBm. Due to the selected frequency of operation and the total synthetic BW of operation, this radar achieved a meter-scale range of coverage and centimeter-scale (1.4 cm) range resolution simultaneously. This radar TRX with a low power consumption of 400 mW offers a potential candidate for future mm-wave radars for automotive, crack detection, and surface monitoring applications.

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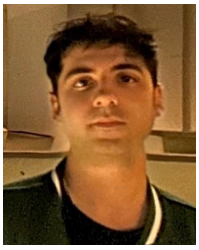

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