

Two-dimensional-materials-based transistors using hexagonal boron nitride dielectrics and metal gate electrodes with high cohesive energy

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Two-dimensional (2D) semiconductors could potentially be used as channel materials in commercial field-effect transistors. However, the interface between 2D semiconductors and most gate dielectrics contains traps that degrade performance. Layered hexagonal boron nitride (h-BN) can form a defect-free interface with 2D semiconductors, but when prepared by industry-compatible methods—such as chemical vapour deposition (CVD)—the presence of native defects increases leakage current and reduces dielectric strength. Here we show that metal gate electrodes with a high cohesive energy—platinum and tungsten—can allow CVD-grown layered h-BN to be used as a gate dielectric in transistors. The electrodes can reduce the current across CVD-grown h-BN by a factor of around 500 compared to similar devices with gold electrodes and can provide a high dielectric strength of at least 25 MV cm⁻¹. We examine the behaviour statistically across 867 devices, which includes a microchip based on complementary metal–oxide–semiconductor technology.

The first commercial transistors had a top-down structure made entirely of silicon: specifically, a polysilicon gate electrode, a thin (~20 nm) SiO₂ dielectric and a silicon bulk channel^{1,2}. In the early 2000s, the size of transistors had been reduced to the point where the leakage current across the SiO₂ (which was only about 2 nm thick) could be more than 10 A cm⁻² at 0.6 V, which led to increased power consumption and premature dielectric breakdown (that is, device failure)³. In 2004, Intel introduced a solution to this problem by replacing SiO₂ with HfO₂, which has a higher dielectric constant (*k*) and can produce the same capacitance effect (necessary to form the channel) using a greater thickness (which reduces the leakage current and slows down

the dielectric breakdown)⁴. Intel started to commercialize this technology in 2008, and all scaled transistors are now based on the high-*k*/metal gate technology⁵.

Two-dimensional (2D) semiconducting materials—such as molybdenum disulfide (MoS₂) and tungsten diselenide (WSe₂)—have been proposed as a candidate to replace silicon in future commercial transistors. The low and accurate thickness (a few angstroms) of these materials could provide excellent electrostatic control over the channel, which should result in negligible current towards the substrate, very low phonon scattering and reduced short-channel effects^{6–8}. However, the interface between 2D semiconductors and most dielectric

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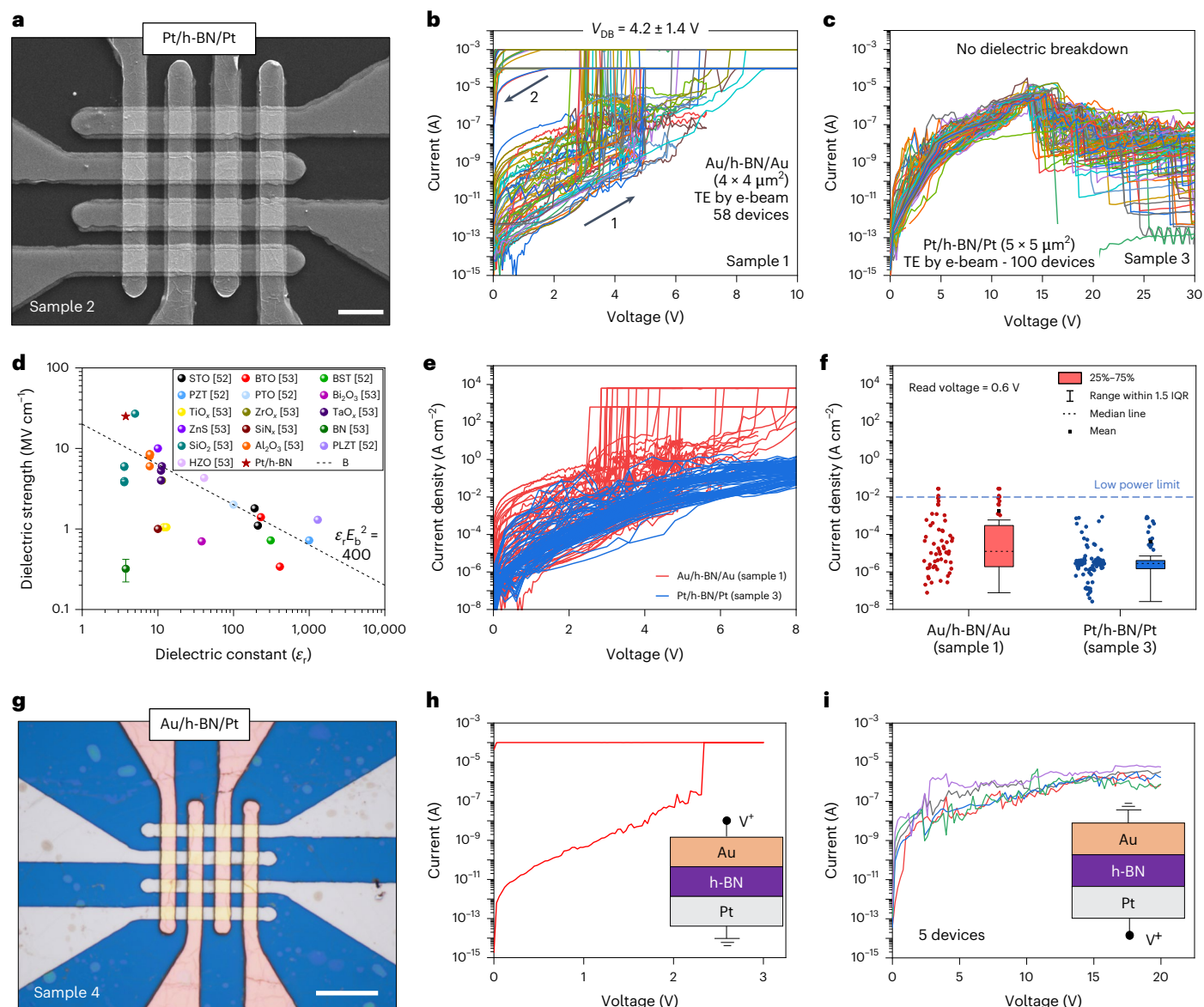


Fig. 1 | Dielectric breakdown and leakage current in Pt/h-BN/Pt and Au/h-BN/Au devices. **a**, SEM image of a 4×4 crossbar array of Pt/multilayer h-BN/Pt (device size $4 \times 4 \mu\text{m}^2$). Scale bar, $10 \mu\text{m}$. **b**, Forming I - V curve measured in Au/multilayer h-BN/Au device. **c**, I - V curve measured in Pt/multilayer h-BN/Pt device; the leakage current is very small, and none of the devices broke down, even at excessively high voltages (up to 30 V). **d**, Dielectric strength (E_b) as a function of dielectric constants (ϵ_r). Plot B is an equation used to describe the relationship between ϵ_r and E_b . The data originate from literature published in the past^{52,53}. Data points represent mean values, with error bars indicating the standard error of the mean. Reproduced from ref. 52 with permission from MDPI. **e**, Current density versus voltage characteristics

measured in Au/multilayer h-BN/Au and Pt/multilayer h-BN/Pt device. **f**, Box line distribution of current density of Au/multilayer h-BN/Au and Pt/multilayer h-BN/Pt device. Each plot displays the median value (central line) and the 25th to 75th percentiles (box boundaries). The whiskers extend to a range of 1.5 times the interquartile range (IQR), beyond which outliers are marked as individual points. **g**, Optical microscopic image of a 4×4 crossbar array of Au/multilayer h-BN/Pt devices (device size $4 \times 4 \mu\text{m}^2$). Scale bar, $20 \mu\text{m}$. **h**, Forming I - V curve measured in Au/multilayer h-BN/Pt device with Au as anode. **i**, I - V plot of different devices that show low leakage currents in Au/multilayer h-BN/Pt device with Pt as anode. Note the considerably larger voltage as compared to **h**.

materials—including hafnium oxide (HfO_2), aluminium oxide (Al_2O_3) and tantalum oxide (Ta_2O_5)—is problematic. In particular, the absence of dangling bonds on the surface of the 2D material impedes conformal coating and generates multiple atomic defects at the interface^{9,10}. At the device level, that is catastrophic because it increases the gate leakage current, hysteresis, subthreshold swing and threshold voltage instability in the transistors¹⁰.

One solution to the problem is to employ 2D hexagonal boron nitride (h-BN) as a gate dielectric, as it forms a defect-free van der Waals interface that results in enhanced performance (such as higher channel mobilities)¹¹. Moreover, h-BN can provide low leakage currents ($<10 \text{ A cm}^{-2}$ at 0.6 V for 1.3-nm-thick stacks)^{3,12} and high dielectric

strength ($\sim 21 \text{ MV cm}^{-1}$)¹³. However, so far this only works when using mechanically exfoliated 2D materials. When using 2D materials synthesized by chemical vapour deposition (CVD), the performance is worse¹⁴ due to the presence of native defects in the h-BN (that is, atomic vacancies, strained bonds, impurities and few-atoms-wide amorphous regions embedded in the 2D layered h-BN)^{15,16}. Various strategies to mitigate this problem have been explored, including the use of a monolayer molecular crystal (such as 10-*perylene-tetracarboxylic dianhydride*) as a seeding layer¹⁷, the use of 2D semiconductors that can be oxidized to form a high-*k* dielectric (such as $\text{Bi}_2\text{O}_3\text{Se}$ to Bi_2SeO_3)¹⁸ and the use of ionic crystals (such as CaF_2) as the gate dielectric¹⁹. However, these methods face integration challenges, and so far industry has not adopted them.

In this Article, we show that metal gate electrodes with a high cohesive energy can be used to mitigate leakage currents and premature dielectric breakdown across CVD-grown multilayer h-BN. Unlike metal oxides (such as HfO_2), in which breakdown can be triggered at low electrical fields by moving oxygen ions, h-BN does not contain conductive atoms and so metal penetration is imperative to trigger the breakdown. As a result, we show that the use of metallic electrodes with a high cohesive energy—platinum and tungsten—can provide gate leakage current that is around 500 times lower and dielectric strength that is around five times higher compared to similar devices with gold electrodes. We illustrate this behaviour statistically in 867 devices from 23 samples, which includes a microchip based on complementary metal–oxide–semiconductor (CMOS) technology at the 180 nm node.

Dielectric breakdown and leakage current in devices

We fabricated 23 different samples to test the magnitude of the electrical current across 8-nm-thick (~24 layers) CVD-grown h-BN. A description of all the samples is provided in Supplementary Table 1. Samples 1–14 correspond to vertical metal/h-BN/metal devices fabricated using different protocols: photolithography or electron-beam lithography (EBL; sizes of $16\text{--}25\ \mu\text{m}^2$ and $0.0759\text{--}0.3685\ \mu\text{m}^2$, respectively); different electrode materials (Pt, Au, Ti, Ag); and different metal evaporation methods (electron-beam evaporation and magnetron sputtering). Sample 15 corresponds to a silicon microchip containing vertical W vias coming from the front-end-of-line transistors and going up to the surface (at the fourth metallization layer). The exposed via is used as the bottom electrode on which the CVD-grown multilayer h-BN is transferred and the top electrode is deposited, resulting in a Pt/h-BN/W device with a lateral size of $\sim 0.053\ \mu\text{m}^2$. Samples 16–23 are field-effect transistors with an MoS_2 channel and CVD-grown multilayer h-BN as gate dielectric. In samples 16–22, the MoS_2 is produced by mechanical exfoliation, and in sample 23 it is produced via CVD.

We first compare the electrical properties of Au/h-BN/Au devices as a reference (sample 1) and Pt/h-BN/Pt devices (samples 2 and 3; Fig. 1) fabricated via photolithography and electron-beam evaporation. We apply positive ramped voltage stresses (RVS) to the devices at the top electrode (keeping the bottom electrode grounded) until dielectric breakdown is triggered, using a current limitation of 10^{-4} or $10^{-3}\ \text{A}$ —that is, a few orders of magnitude above the breakdown current. We measured 94 Au/h-BN/Au devices (sample 1) and 200 Pt/h-BN/Pt devices (sample 3), and the yield (that is, the percentage of devices that was not shorted over the total) was relatively high: 61.7% and 81%, respectively. This yield is much higher than that observed in similar devices made of monolayer h-BN¹⁵ and is related to the higher mechanical strength of ~24-layers-thick CVD-grown h-BN, which avoids pinholes and microcracks during transfer.

Statistically, the Au/h-BN/Au devices show initial currents of ~100 fA at 0.05 V, and these currents increase progressively up to a point at which they suddenly increase by several orders of magnitude until reaching the current limitation (Fig. 1b). When the voltage is then ramped down, the currents stay at the current limitation until the voltage is <0.1 V. The gap between forward and backward sweeps and the high currents ($>10^{-5}\ \text{A}$) registered in the backward sweep at very low voltages (<0.1 V) indicate that the dielectric breakdown has been triggered. The dielectric breakdown voltage (V_{DB}) was found to be $4.2 \pm 1.4\ \text{V}$, and we quantify its variability by calculating the coefficient of variance as the standard deviation divided by the mean value, which gives 49.09%. When the same experiments are repeated using Pt/h-BN/Pt devices, the initial currents are also low (~100 fA at 0.05 V); however, the resistance of the devices remains unaltered even if voltages of ~15 V are applied (Fig. 1c). In some devices the resistance is preserved even when voltages up to ~20 V are applied (Supplementary Fig. 1), probably due to the h-BN stack in those specific devices having a lower number of defects.

These observations indicate that when gold electrodes are used, the dielectric strength (also referred to as the breakdown field) of our ~8-nm-thick CVD h-BN stack is $5.2\ \text{MV cm}^{-1}$. When platinum electrodes are used, this value is over $25\ \text{MV cm}^{-1}$ (Fig. 1d), which is even higher than the $21\ \text{MV cm}^{-1}$ measured in mechanically exfoliated h-BN¹³. At higher voltages, the currents across the Pt/h-BN/Pt progressively reduce due to the degradation and melting of the metallic electrodes (Fig. 1c and Supplementary Fig. 2). Statistical analyses indicate that the leakage current across the CVD-grown h-BN stack (read at 0.6 V) is reduced by a factor of ~10 when using platinum electrodes compared to gold electrodes, and it also shows lower device-to-device variability (Fig. 1e,f). We also note that all the Pt electrode devices fulfil the current density requirements ($<10^{-2}\ \text{A cm}^{-2}$; the horizontal dashed line in Fig. 1f) of the International Roadmap of Devices and Systems for use as gate dielectrics⁶. When the devices are exposed to accelerated constant voltage stresses, a typical reliability figure-of-merit for dielectrics, the use of platinum electrodes results in an average ~40-times-longer lifetime (Supplementary Fig. 3) compared to gold electrodes.

Initially, we thought that the platinum electrodes might be interacting with the polymers used during the fabrication process (that is, the photoresist during photolithography or polymethyl methacrylate during transfer), impeding their complete removal and increasing the electrical resistance of the Pt/h-BN/Pt devices. However, the following measurement showed that this is not the case. First, we fabricated and stressed asymmetric devices consisting of (from top to bottom) Au/h-BN/Pt (sample 4; Fig. 1g). When positive RVS is applied to the top gold electrode, the currents driven (Fig. 1h) are very similar to those driven by the Au/h-BN/Au devices (Fig. 1b) with initial currents of ~100 fA at 0.05 V and a V_{DB} of ~2.4 V. This confirms that the device is correctly fabricated and free of any insulating contaminants. However, when positive RVS is applied to the bottom Pt electrode, the currents registered (Fig. 1i) are very similar to those driven by the Pt/h-BN/Pt devices (Fig. 1c). A similar result occurs in the Ti/h-BN/Pt devices (sample 5; Supplementary Fig. 4). As well as confirming the observations in Fig. 1b,c, this result indicates that the dielectric breakdown process in the CVD-grown h-BN is related to the penetration of metallic ions from the electrodes under an electrical field.

Second, we analysed the Pt/h-BN/Pt and Au/h-BN/Au devices via cross-sectional transmission electron microscopy (TEM) coupled with energy dispersive X-ray spectroscopy (EDX) and electron energy loss spectroscopy (EELS). The fresh devices show the layered structure of h-BN, although with several orientations and lattice defects, as expected^{15,16} (Fig. 2a,d). The chemical characterization shows the expected symmetric boron and nitrogen profiles sandwiched by the platinum electrodes (Supplementary Fig. 5). Therefore, the structure of the Pt/h-BN/Pt and Au/h-BN/Au devices is correct. We note that the focused ion beam process used to prepare the devices for TEM did not produce the defects observed in the TEM images because when we cut h-BN devices produced by mechanical exfoliation, no defects are observed (Supplementary Fig. 6). When the devices are stressed, the Pt/h-BN/Pt devices show no notable changes in morphology and chemical composition (Fig. 2b,c), consistent with the absence of a resistance increase at low voltages below V_{DB} (Supplementary Fig. 1). However, the stressed Au/h-BN/Au devices show traces of Au penetration into the h-BN both in the cross-sectional TEM images and in the EDX and EELS maps (Fig. 2e,f and Supplementary Fig. 7). Third, we fabricated another cross-point Pt/h-BN/Pt device using magnetron sputtering (instead of electron-beam evaporation) to deposit the platinum electrodes and rule out any kind of interaction or contamination related to the metal deposition technique. The electrical characteristics look similar independent of the method used to deposit the electrodes (Supplementary Fig. 8).

Next, we fabricated smaller Pt/h-BN/Pt devices and Au/h-BN/Au devices with lateral sizes below $600 \times 600\ \text{nm}^2$ (Fig. 3a) using EBL and depositing the electrodes using electron-beam evaporation or

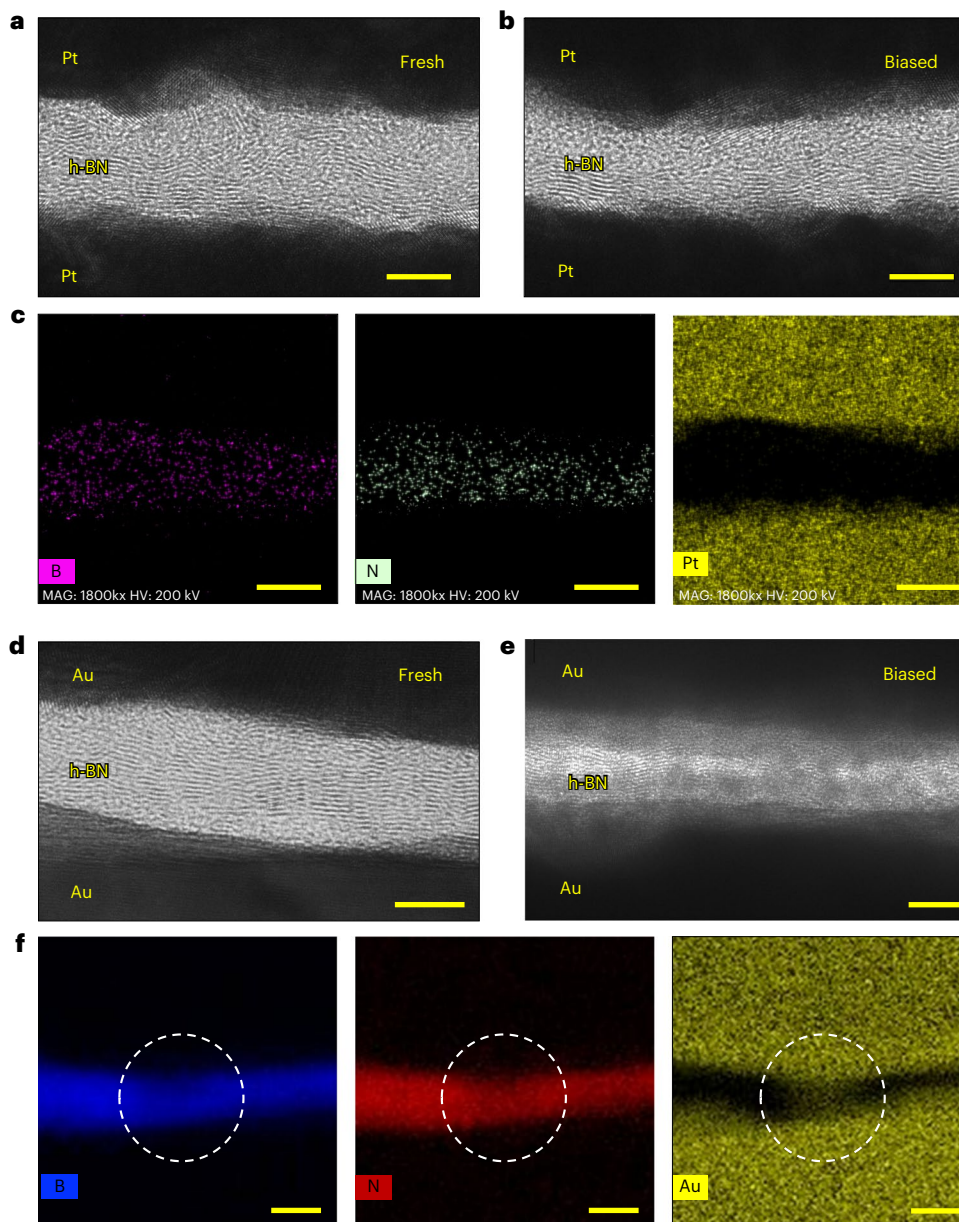


Fig. 2 | Morphological and chemical characterization of fresh and biased Pt/h-BN/Pt and Au/h-BN/Au devices. a, b, Cross-sectional TEM images of a fresh Pt/h-BN/Pt device (a) and a stressed Pt/h-BN/Pt device (b). **c,** EDX maps of B, N and Pt signals of a stressed Pt/h-BN/Pt device. EDX mapping images acquired at 1.8 million magnification (MAG 1800kx) using 200 kV high voltage (HV).

d, e, Cross-sectional TEM images of a fresh Au/h-BN/Au device (d) and a stressed Au/h-BN/Au device (e). **f,** EELS maps of B, N and Au signals of a stressed Au/h-BN/Au device at a location where severe metal penetration has taken place (inside the dashed circle). Scale bars: 5 nm for a, b, d and e; 10 nm for c and f.

magnetron sputtering (samples 7–11; Supplementary Table 1). Again, the Au/h-BN/Au devices exhibit premature breakdown ($V_{DB} < 4$ V) and the Pt/h-BN/Pt devices never reach dielectric breakdown (Fig. 3b,c)—most (~91.8%) Pt/h-BN/Pt devices show a sudden current decrease when the voltage reaches values of ~12 V due to the melting of the metallic wires (Supplementary Fig. 9). In this case, the use of platinum electrodes reduces the gate leakage current by a factor of up to ~500 compared to gold electrodes (Fig. 3d,e). The devices with electrodes deposited via electron-beam evaporation and magnetron sputtering show similar behaviours (Fig. 3f and Supplementary Fig. 8), which eliminates experimental factors related to the deposition technique. These observations confirm that the platinum electrodes are the main factor for the high V_{DB} and low leakage currents. In total, we fabricated 14 samples in 7 months using different electrode materials, device sizes, lithography techniques and metal evaporation tools (Supplementary

Table 1) and characterized 799 metal/h-BN/metal devices, and in all cases the application of positive RVS to the platinum electrode results in a much lower leakage current and much higher V_{DB} .

Previous studies in metal oxides showed that the leakage current and V_{DB} depend on the conductivity and diffusivity of the metallic electrodes used^{20,21}. However, the high dielectric strength observed in Pt/h-BN/Pt devices is not observed in metal oxides sandwiched by platinum electrodes. For example, it was reported that the V_{DB} in Pt/10-nm-HfO₂/Pt devices is 4.3 ± 0.6 V (ref. 22), and the V_{DB} Pt/50-nm-TiO₂/Pt is up to 20 V (ref. 23). This gives dielectric strengths of 4.3 and 4.0 MV cm⁻¹, respectively. The reason for this difference is that metal oxides can trigger dielectric breakdown in two different ways: (1) when metal-oxide devices with active electrodes (Ag, Cu) are exposed to an electrical field, positive metallic ions from the electrodes can penetrate into the metal oxide until a conductive filament forms and triggers

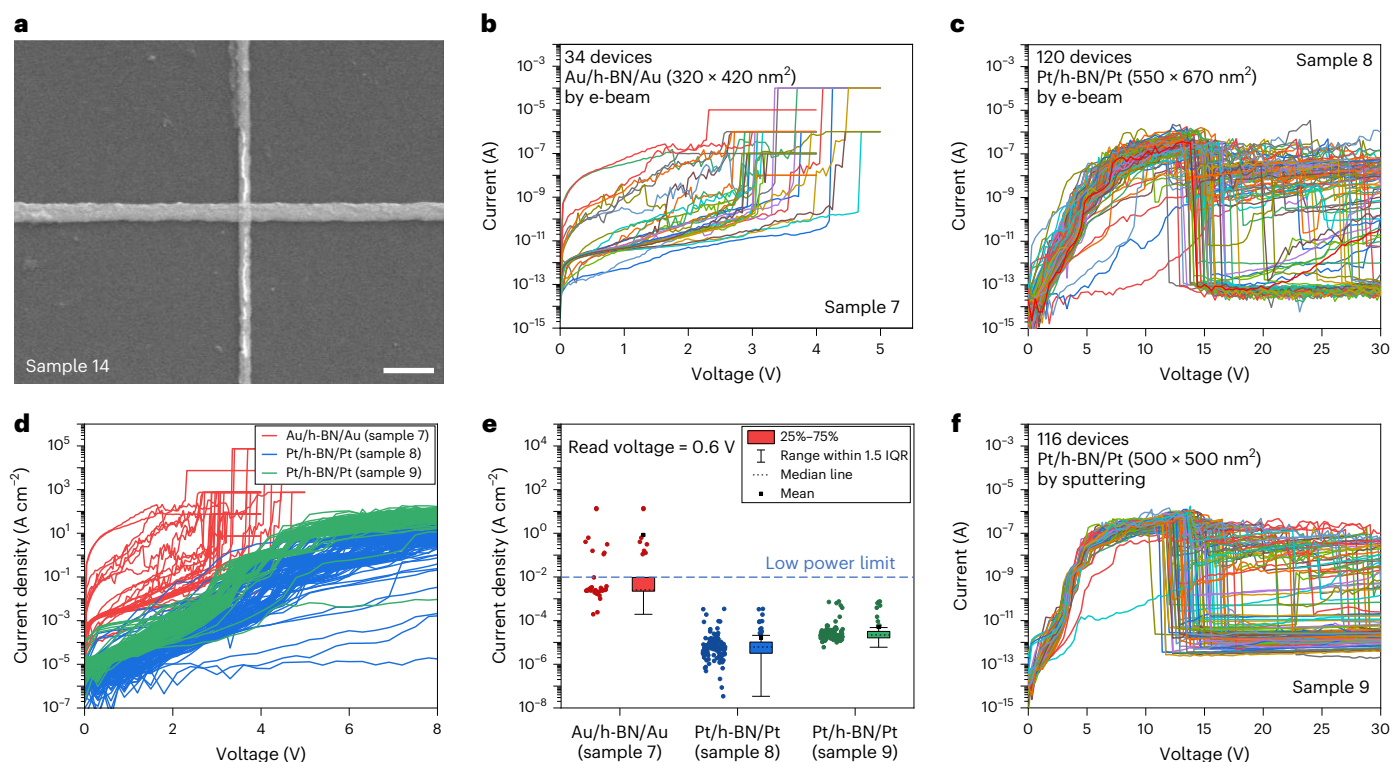


Fig. 3 | Dielectric breakdown and leakage current in small Pt/h-BN/Pt and Au/h-BN/Au devices. **a**, SEM image of a cross-point Pt/h-BN/Pt device (device size $370 \times 250 \text{ nm}^2$). Scale bar, $1 \mu\text{m}$. **b**, Current versus voltage characteristics measured in Au/multilayer h-BN/Au devices with lateral size of $320 \times 420 \text{ nm}^2$. Au electrodes were deposited by electron-beam evaporation. **c**, Current versus voltage characteristics measured in Pt/multilayer h-BN/Pt devices with lateral size of $500 \times 500 \text{ nm}^2$. Pt electrodes were deposited by electron-beam evaporation. **d**, Current density versus voltage characteristics measured in Au/

multilayer h-BN/Au and Pt/multilayer h-BN/Pt devices. **e**, Box line distribution of current density of Au/multilayer h-BN/Au and Pt/multilayer h-BN/Pt devices. Each plot displays the median value (central line) and the 25th to 75th percentiles (box boundaries). The whiskers extend to a range of 1.5 times the interquartile range, beyond which outliers are marked as individual points. **f**, I - V curve measured in Pt/h-BN/Pt devices with lateral size of $500 \times 500 \text{ nm}^2$ with Pt electrodes deposited by magnetron sputtering. Thickness of h-BN is $\sim 8 \text{ nm}$. IQR, interquartile range.

dielectric breakdown^{22,23}; and (2) when very stable electrodes (like Pt) are used, oxygen ions within the metal oxide can migrate, leaving behind a metallic path (that is, Hf in HfO_2 , Al in Al_2O_3), which also triggers dielectric breakdown^{24,25}. However, multilayer h-BN does not contain metallic ions, and therefore metal penetration is always necessary to trigger dielectric breakdown^{26,27}. Hence, the use of highly stable metals with a high cohesion energy like platinum²¹ results in a high dielectric strength.

DFT simulations of h-BN breakdown and stability analysis

We further study the dielectric breakdown of h-BN films using atomistic simulations based on density functional theory (DFT). We start by analysing the electronic structure of both h-BN and amorphous BN (a-BN). Here, a-BN serves as a model system to understand the impact of amorphous defects a few atoms wide embedded in otherwise crystalline h-BN. Figure 4a,b shows the density of states (top) for h-BN and a-BN, respectively. In the case of h-BN, we obtain a bandgap of 5.8 eV , in good agreement with experimental values (5.95 eV)²⁸. Upon amorphization, the electronic bandgap reduces to 3.2 eV . However, by analysing the inverse participation ratio (IPR)²⁹ of the electronic states (bottom panels in Fig. 4a,b), we show that the introduced states close to the newly formed band edges are mostly (semi)localized. Although these states could act as charge trapping sites, potentially leading to reliability issues (like bias temperature instability and increased leakage current via trap-assisted tunnelling), they are not conductive in themselves and thus are not likely to play a role in dielectric breakdown. To better understand the microscopic breakdown mechanism, we studied the

formation of defects in both BN phases. As shown in Fig. 4c, we find that the formation energy for boron vacancies is substantially reduced in a-BN ($4.00 \pm 1.05 \text{ eV}$) compared to h-BN (9.80 eV), suggesting a much larger defect concentration in a-BN. Although in this work we primarily focused on boron vacancy as a prototypical defect in BN, we expect a similar trend for other defect types as well.

Because conductive filaments can be formed in h-BN under applied bias¹⁶, we study the initial stages of dielectric breakdown by investigating the penetration of platinum and gold atoms into a-BN and incorporation at boron vacancy sites. We find that the estimated penetration barrier from the electrode into the dielectric (E_b) is substantially lower for gold ($2.64 \pm 0.34 \text{ eV}$) than for platinum ($4.65 \pm 0.27 \text{ eV}$), thus providing an explanation for the increased dielectric breakdown field when using platinum (Fig. 4d,e). The large difference in E_b can be attributed to the electron configuration of platinum leading to a much larger cohesive energy. Indeed, we find that there is a strong correlation between the observed breakdown field and the cohesive energy of the electrode metal (Fig. 4f), making the cohesive energy a key parameter for the electrical stability of the dielectric. Figure 4f also suggests that the use of metals with higher cohesive energy may result in even better performance. We conclude that the dielectric breakdown in h-BN films occurs primarily via metal atoms from the electrode penetrating into the dielectric and being incorporated at vacancy sites. Because the density of vacancies is much larger in a-BN, based on our formation energy calculations, we expect this process to be primarily initiated at disordered defects a few atoms wide embedded in the crystalline 2D layered h-BN.

We also analyse the stability of the currents across Pt/h-BN/Pt devices (fabricated via photolithography and electron-beam

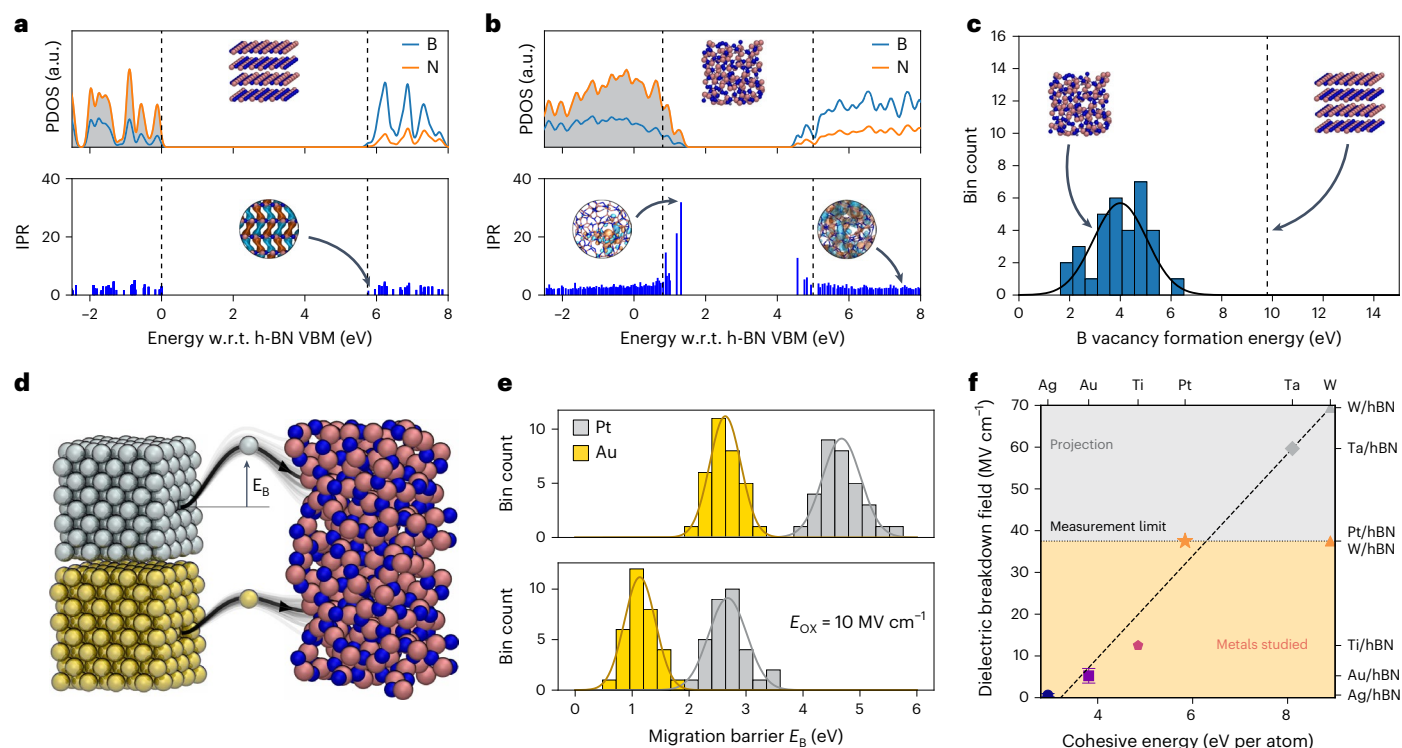


Fig. 4 | Atomistic simulation of dielectric breakdown in Pt/h-BN/Pt and Au/h-BN/Au devices. **a**, Projected density of states and IPR analysis for bulk h-BN. The small IPR values throughout the spectrum indicate that all states are delocalized. The inset shows the states close to the bottom of the conduction band. **b**, Analogous analysis for amorphous boron nitride (a-BN). A drop in the bandgap is observed compared to h-BN. The states close to the band edges are strongly localized, as indicated by large IPR values. These states could act as charge trapping sites and do not contribute to transport. The states within the conduction band are more delocalized (inset). The dashed lines mark the mobility edges: that is, the boundaries between localized and delocalized states. **c**, Formation energies of B vacancies in h-BN and a-BN. The formation of these defects is much easier in a-BN, suggesting a high concentration of vacancies in

disordered embedded defects a few atoms wide. **d**, Schematic representation of metal atoms penetrating a-BN. For Pt, the penetration barrier is much larger than for Au, explaining the large increase in breakdown field for stacks with Pt electrodes. **e**, Histograms of the penetration barriers obtained from DFT (upper panel) and corrected by a positive applied bias (bottom panel). Even at moderately high fields of 10 MV cm^{-1} , the Au electrode shows barriers below 1 eV, thus making penetration into the dielectric likely at room temperature. **f**, Dielectric breakdown field of CVD-grown h-BN sandwiched by a metal versus the cohesive energy of that metal, showing a strong correlation between the two properties. Data points represent mean values, with error bars indicating the standard error of the mean. The dielectric breakdown in Ag/h-BN/Ag devices (sample 6) is shown in Supplementary Fig. 18. a.u., arbitrary units; w.r.t., with respect to.

evaporation; sample 12) by measuring the electrical characteristics at different temperatures (Supplementary Figs. 10 and 11). These indicate that all the devices are stable at high temperatures up to -175°C and some of them even up to 225°C (Supplementary Fig. 12). Devices fabricated using the same methods but using gold electrodes (sample 13) and titanium electrodes (sample 14) show an increase in leakage current by a factor of ~ 100 when they are exposed to temperatures of 150°C (Supplementary Figs. 13 and 14), and at 275°C the devices are severely damaged. This observation again points to the platinum electrode as the main factor governing the currents flowing across Pt/h-BN/Pt devices.

Microchip and 2D transistor applications

Next, we integrate the multilayer h-BN on a microchip (sample 15) containing circuitry from the 180 nm CMOS technology node to form Au/Ti/h-BN/W capacitors with sizes of $\sim 0.053 \mu\text{m}^2$ (Methods and Fig. 5a–d). We use the W vias coming up from the fourth metallization layer as the bottom electrode. First, we etch a small amount of the SiO_2 surface of the microchip ($\sim 10 \text{ nm}$) to expose the vias, then we transfer the h-BN sheet following a standard wet transfer process, and finally we pattern the top electrode via photolithography. Cross-sectional TEM images confirm the correct structure of the devices, and topographic atomic force microscopy (AFM) maps show that no wrinkles are formed on the vias, as they are acting as subsection points. When the devices are stressed by applying positive RVS to the top Au/Ti electrode, we observe $V_{\text{DB}} < 3 \text{ V}$ (Fig. 5e); however, when a negative RVS is applied to the top

Au/Ti electrode (that is, the tungsten electrode serves as anode), we never observe dielectric breakdown even if voltages up to 30 V are applied, and the leakage current never exceeds the noise level of the instrumentation for voltages up to 20 V (Fig. 5f, left). Surprisingly, if a second RVS is applied to the Au/Ti electrode, this time with positive polarity, V_{DB} increases to $\sim 5 \text{ V}$ and the currents never surpass $5 \mu\text{A}$ (Fig. 5f, right), indicating that the first RVS modified the structure of the Au/Ti/h-BN/Au device and made it more resistive. These behaviours have been observed in six different microchip devices (all measured), as indicated in Supplementary Table 1. Compared to platinum, the use of tungsten is also more beneficial because it is being already employed by the industry in multiple parts of microchips (Fig. 5c).

To further confirm the applicability of Pt/h-BN as a gate stack in transistors with 2D semiconducting channels, we fabricate field-effect transistors with mechanically exfoliated MoS_2 as the channel, $\sim 8 \text{ nm}$ -thick CVD-grown multilayer h-BN as the dielectric and platinum as the gate electrode (samples 20–26). The detailed fabrication process is shown in Supplementary Fig. 15. The source and drain electrodes were made of gold, and the gate length is $\sim 0.5 \mu\text{m}$. Figure 6a shows the scanning electron microscope (SEM) image of one of the transistors. The typical drain-to-source current (I_{DS}) versus drain-to-source voltage (V_{DS}) characteristic for different gate voltages (V_{G}) and the typical I_{DS} versus V_{G} characteristic for $V_{\text{DS}} = 2 \text{ V}$, referred to as output and transfer characteristics, respectively, are shown in Fig. 6b–c (data from more devices are shown in Supplementary Fig. 16). The drain current can

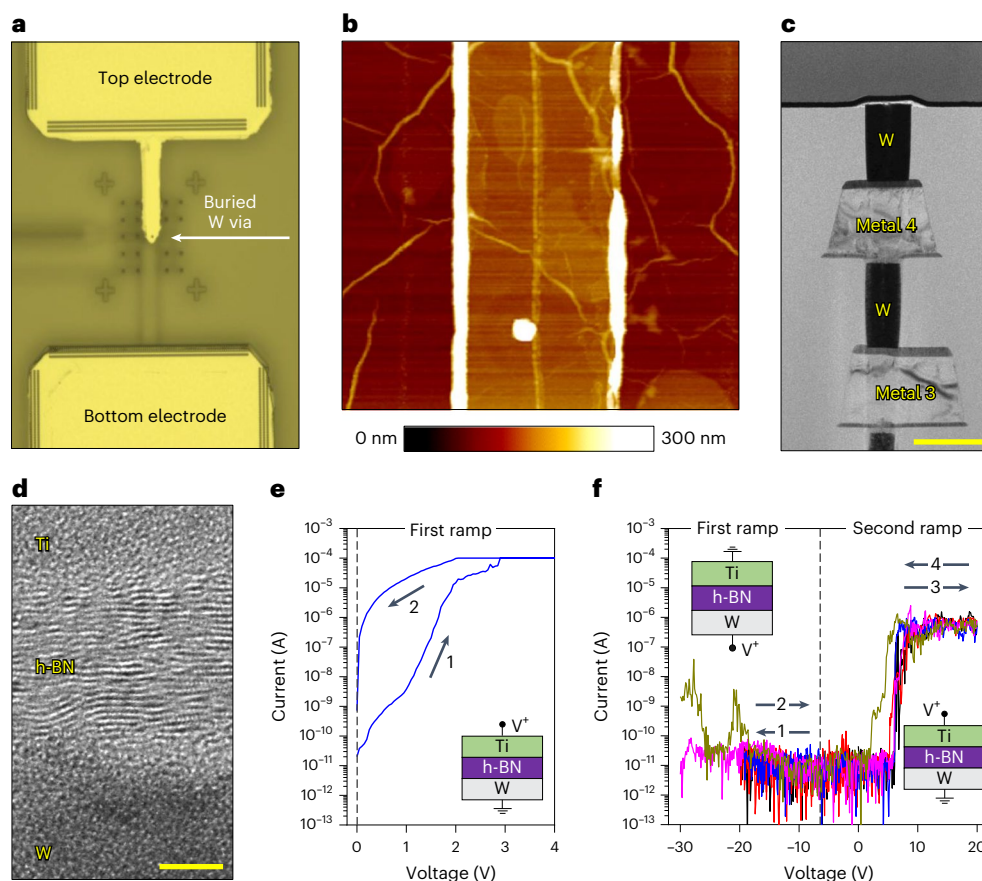


Fig. 5 | Characterization of Au/Ti/h-BN/W structures embedded in a microchip. **a**, Optical microscope image of the Au/Ti/h-BN capacitor with the top electrode up and the bottom electrode down. **b**, Topographic AFM map in which the top electrode, W via and wrinkles of the h-BN can be observed. Image size $7 \times 6 \mu\text{m}^2$. No wrinkles are formed on the W via because it is slightly elevated and acts as support. **c**, Cross-sectional TEM image of an Au/Ti/h-BN/W capacitor formed by integrating the h-BN on the W via. The diameter of the W via is 260 nm, and hence the area of the Au/Ti/h-BN/W device is $0.053 \mu\text{m}^2$. Scale bar, 500 nm.

d, Enlarged cross-sectional TEM image of a region of the chip next to the W via, showing the correct layered structure of the h-BN. Scale bar, 5 nm. **e**, Positive I - V curves applied to the top Ti electrode, showing that $V_{\text{DB}} < 3 \text{ V}$ and post-breakdown currents easily reach $100 \mu\text{A}$. **f**, Positive I - V curves applied to the bottom W electrode of five different devices, showing that they can resist 30 V and the currents never exceed the noise level for voltages up to 20 V. The second ramp shows that after such a stress cycle, the devices become more insulating: that is, $V_{\text{DB}} \sim 5 \text{ V}$, and the currents never surpass $5 \mu\text{A}$.

be modulated by adjusting either V_{DS} or V_{G} (Fig. 6b–c), reaching high current on/off ratios up to $\sim 10^6$ and a low subthreshold swing down to 68 mV per decade (Supplementary Fig. 16c). Note that the value of subthreshold swing measured at a specific V_{G} does not depend on the value of V_{D} , indicating there is no drain-induced barrier lowering, which is a common reliability problem in beyond-silicon transistors^{30–32}. More importantly, the gate leakage current density is always lower than $10^{-4} \text{ A cm}^{-2}$ (Fig. 6e), which is two orders of magnitude below the low power limit acceptable for ultrascaled transistor nodes.

It should be noted that the maximum drain current per unit width driven by the MoS_2 transistors is $\sim 1 \mu\text{A } \mu\text{m}^{-1}$. The reasons are: (1) the formation of a Schottky contact between the gold source/drain electrodes and the MoS_2 channel, as indicated by the nonlinear and asymmetric output characteristics in the triode region (Supplementary Fig. 17a) and the increased subthreshold swing at higher currents (up to 200 mV dec^{-1} ; Supplementary Fig. 16c,f); and (2) the presence of a $\sim 300 \text{ nm}$ gap between the edge of the gate electrode and the source/drain electrodes, resulting in an ungated region of the MoS_2 channel and additional series resistance. Articles that have reported record drain currents per unit width use gate electrodes that fully cover the MoS_2 channel and slightly overlap with the source/drain³³. The maximum current density per unit width is similar to that reported in other studies using a similar fabrication method (Supplementary Fig. 17c,d and Supplementary Table 2), and it could be enhanced using other metals

(Bi, Sn, S), using ultra-high vacuum ($< 10^{-7}$ torr) evaporation, avoiding ungated regions in the MoS_2 channel and making shorter devices with channel lengths below 500 nm. Nevertheless, the aim of this study is to reduce the leakage current and increase the lifetime of devices with CVD-grown multilayer h-BN by slowing the dielectric breakdown process, not to report record on-state currents. Our approach of using gate electrodes with a high cohesive energy (W, Pt) achieves this and is independent of the type of source/drain contacts used.

Finally, we fabricated all-CVD transistors with Pt/h-BN/ MoS_2 gate structure (Fig. 6d; sample 27)^{6,34} using CVD for the synthesis of all the 2D materials and photolithography and metal evaporation for the patterning of the electrodes. We characterize the all-CVD transistors in the dark and when exposed to white light illumination intensity of 10 W m^{-2} . The electrical transfer characteristics of the devices (Fig. 6e) demonstrate that they can be employed as photodetectors with current on/off ratios up to $\sim 1,000$ and gate current density well below $10^{-4} \text{ A cm}^{-2}$, which is more than two orders of magnitude below the low power limit. For this photodetector application, as well as others such as MoS_2 synaptic transistors^{35,36}, keeping a low drain current per unit width is beneficial to reduce power consumption.

Conclusions

We have shown that metal electrodes with a high cohesive energy can allow commercial CVD-grown 2D layered h-BN to be used as gate

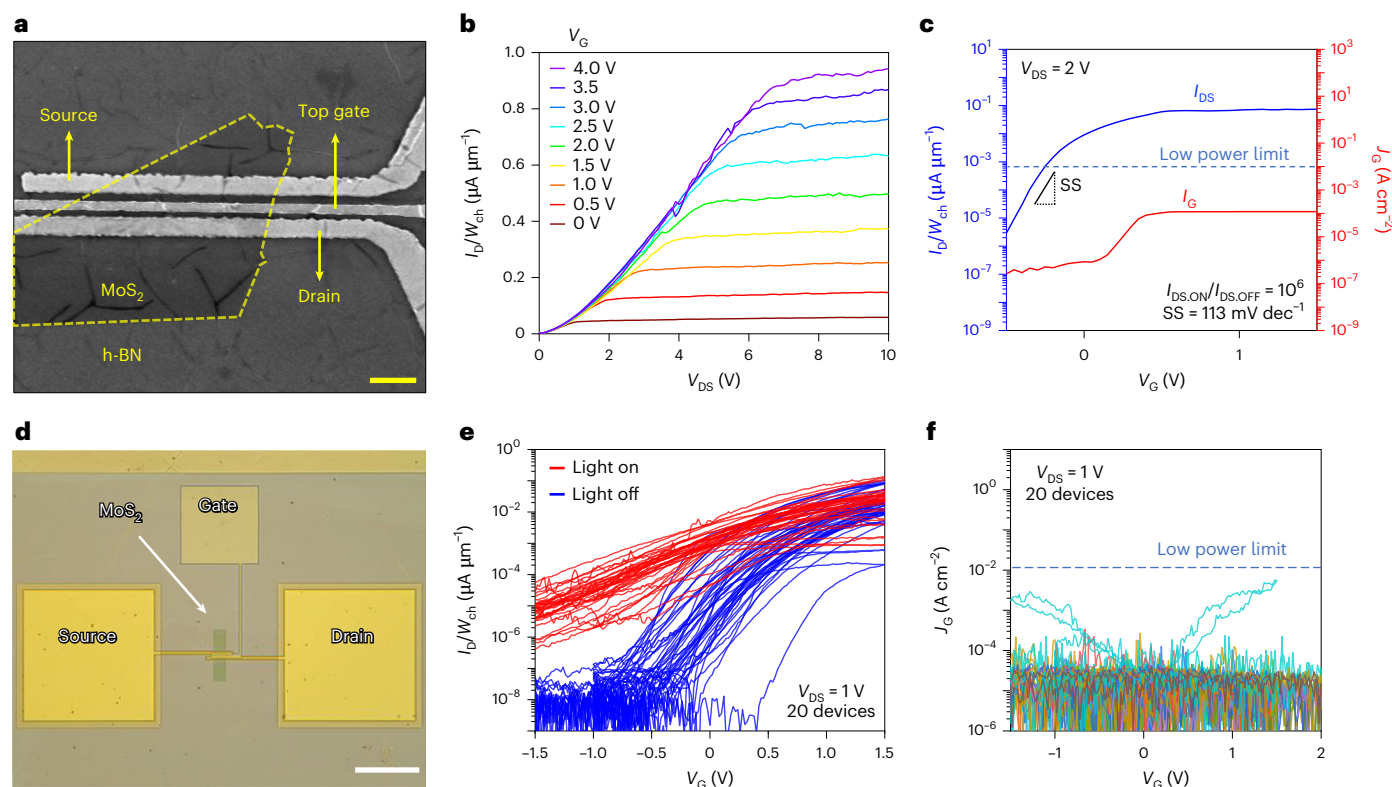


Fig. 6 | Morphology and electrical characteristics of MoS₂ transistors with Pt/h-BN gate stack. **a**, SEM image of a transistor with Pt/h-BN/MoS₂ structure in which the h-BN is grown by CVD and the MoS₂ is mechanically exfoliated. The gate length and width are $0.5 \times 9 \mu\text{m}^2$. Scale bar, $2 \mu\text{m}$. The thickness of h-BN in this sample is ~ 8 nm. Source and drain electrodes are made of gold by magnetron sputtering. **b, c**, Output characteristics (**b**) and transfer characteristics (**c**) of the transistor device. **d**, Optical microscope image of an all-CVD transistor with Pt/h-

BN/MoS₂ gate stack. Scale bar, $25 \mu\text{m}$. **e**, Transfer characteristic for 20 devices like those in **d** in the dark and under illumination, confirming their correct use as photodetector. The low currents (provoked by non-optimized Schottky contacts between MoS₂ channel and Au source/drain electrodes) are even beneficial in this application to reduce power consumption. **f**, Gate current density versus gate voltage for the same 20 devices measured in **e**, showing no detectable gate leakage current. SS, subthreshold swing.

dielectric in transistors, despite the fact that the h-BN contains numerous native defects. The use of platinum electrodes reduces the leakage current across around 8-nm-thick CVD-grown h-BN by a factor of around 500 compared to gold electrodes, and the use of tungsten electrodes results in undetectable leakage current at voltages up to 20 V. In both cases, the electrodes provide a dielectric strength of more than 25 MV cm^{-1} . Further optimization of our Pt/h-BN and W/h-BN stacks, as well as the use of other industry-friendly high-cohesive-energy metals (such as TaN or TiN), could allow them to fulfil the requirements of CMOS technologies. Our approach could ultimately help accelerate the introduction of 2D materials in solid-state microelectronic devices and circuits.

Methods

Fabrication of metal/h-BN/metal devices (samples 1–14)

The 14 samples fabricated can be divided into two groups based on device structure. One group is crossbar arrays of metal/h-BN/metal devices with array size 4×4 and device size $4 \times 4 \mu\text{m}^2$ (made via photolithography), and the second group is isolated metal/h-BN/metal cross-point devices with lateral sizes below $600 \times 600 \text{ nm}^2$ (made via EBL). In both cases, the process starts by cleaning a $300 \text{ nm SiO}_2/\text{Si}$ substrate ($1.5 \times 1.5 \text{ cm}^2$) in acetone, alcohol and deionized water for 20 min (each step) under ultrasonication (model KQ-100KDB, power 99 W). Then the bottom electrodes were patterned. For the large crossbar arrays, we used a mask aligner (model SUSS MJB4, photoresist AR-P 5350, developer ZX-238 diluted in pure water (1:5)); and for the small isolated cross-point devices, we used EBL (model Raith ELPHY VI, resist 950 polymethyl methacrylate (PMMA) A4, developer methyl isobutyl ketone (MIBK) diluted in isopropyl alcohol (IPA; 1:3)) integrated in a

SEM (model Quanta 200). The bottom electrode was made of 5 nm titanium with 45 nm gold, platinum, titanium or silver on top, and it was deposited at a rate of 0.04 nm s^{-1} with an electron-beam evaporator (Kurt J. Lesker PVD75 Deposition System) or at a higher rate using magnetron sputtering (Kurt J. Lesker PVD75 Deposition System). Then a 2D layered h-BN stack (~ 8 nm multilayer h-BN, bought from Graphene Supermarket) was transferred on the bottom electrode using a PMMA scaffold (see below). Then the PMMA scaffold was removed by soaking in acetone (>12 h) after transfer. Finally, top electrodes (gold, platinum, titanium or silver) were deposited using a process similar to that used for the bottom electrodes. Finally, a third lithography step was performed to etch the h-BN on the bottom electrodes, using Ar/O_2 plasma, and the resulting Au/h-BN/Au, Pt/h-BN/Pt, Au/h-BN/Pt, Ti/h-BN/Pt and Ag/h-BN/Ag devices (with different sizes) were ready to be tested.

Transfer of h-BN sheets

Liquid PMMA solution (5 wt% PMMA/anisole solution, number-average molecular weight of PMMA 996000) was spin-coated (at 800 rpm for 5 s and 3,000 rpm for 30 s) on a piece of $0.5 \times 0.5 \text{ cm}^2$ h-BN/Cu foil. The PMMA solution was turned into polymer scaffolds on the surface of the h-BN sheet by soft baking at 100°C for 3 min, which formed a solid PMMA film with a thickness of ~ 200 nm. Then the PMMA/h-BN/Cu foil was put in 2 wt% FeCl_3 liquid solution for several hours until the Cu foil is etched away. After that, the PMMA/h-BN sheet was cleaned in 0.1 mol l^{-1} HCl liquid solution for 2 min and then in deionized water for 1 h. The PMMA/h-BN stack was picked up by the target substrate ($300 \text{ nm SiO}_2/\text{Si}$ substrate with deposited bottom electrodes, in this case). The whole sample was heated at 50°C for 5 min to evaporate the water between

h-BN and the target substrate. Then the sample was soaked in acetone for over 12 h to help remove the PMMA film on the surface of the h-BN.

Some experts consider this approach not realistic for wafer-scale nano/microelectronics due to the generation of residues, cracks and pinholes in the transferred 2D material. However, substantial progress has been achieved in the past few years using wafer-to-wafer bonding³⁷ and roll-to-roll techniques³⁸. Multiple groups have also demonstrated large arrays of 2D-materials-based electronic devices with a high yield^{39–42}, and there are companies offering multiproject wafer tape-outs involving the transfer of 2D materials⁴³. We note that those studies used monolayer 2D materials, and transfer of multilayer 2D materials (like the h-BN used in this study) is much easier due to its higher mechanical stability¹⁵. In general, the feasibility of the transfer strongly depends on the type of material to transfer and its thickness¹⁵, the type of device and its resiliency to defects²⁶, the device size³⁸ and the technical specifications of the application. Hence, the transfer of 2D materials may be suitable for some technologies and challenging for others.

Microchip fabrication (sample 15)

The microchips were fabricated in a commercial foundry using 180 nm CMOS technology. The wafers were finished in the fourth metallization layer and sent to the King Abdullah University of Science and Technology. The $2 \times 2 \text{ cm}^2$ microchips were separated, and the native oxide that formed during shipping was etched away using a diluted hydrofluoric acid (10:1) bath for 1 min. This exposed the 260-nm-wide circular tungsten vias that served as bottom electrodes. Then we transferred a sheet of 8-nm-thick multilayer h-BN on the microchip following the above process. Finally, we deposit the top 40-nm-thick Au on 20-nm-thick Ti electrodes using photolithography, electron-beam evaporation and lift-off.

Fabrication of Pt/h-BN/MoS₂ transistors with exfoliated channel (samples 16–22)

A 300 nm SiO₂/Si substrate ($1.0 \times 1.0 \text{ cm}^2$) was cleaned in acetone, ethanol and deionized water for 20 min (each step) under ultrasonication (model KQ-100KDB, power 99 W). Then we patterned the source and drain electrodes (5 nm titanium and 45 nm gold) by EBL (model Raith ELPHY VI, resist 950 PMMA A4, developer MIBK diluted in IPA (1:3)), electron-beam evaporation (Kurt J. Lesker PVD75 Deposition System) and lift-off. Then we exfoliated MoS₂ from a natural MoS₂ crystal (from Moly Hill mine) using tape (Nitto SPV-224Pr) and placed it on the source and drain electrodes using a transfer stage (model OWTS-01 from Shanghai ONWAY Technology Co., Ltd) equipped with an optical microscope. Then we transferred a -8-nm-thick CVD-grown h-BN film to cover the whole structure following the above transfer method. Finally, the top-gate electrode was patterned by EBL, electron-beam evaporation of platinum and lift-off. The channel length and width of the transistors are around $0.5 \times 9 \text{ }\mu\text{m}^2$.

Fabrication of all-CVD Pt/h-BN/MoS₂ transistors (sample 23)

The all-CVD h-BN/MoS₂ transistors were fabricated at Penn State University. Monolayer MoS₂ was deposited on an epi-ready 2-inch sapphire substrate by MOCVD. An inductively heated graphite susceptor equipped with wafer rotation in a cold-wall horizontal reactor was used to achieve uniform monolayer deposition. Molybdenum hexacarbonyl (Mo(CO)₆) and hydrogen sulfide (H₂S) were used as precursors. Mo(CO)₆ maintained at 25 °C and 375 torr in a stainless-steel bubbler was used to deliver 2.0×10^{-2} sccm of the metal precursor for the growth, whereas 400 sccm of H₂S was used for the process. MoS₂ deposition was carried out at 950 °C and 50 torr in H₂ ambient, with monolayer growth being achieved in 18 min. Before growth, the substrate was baked at 1,000 °C in H₂ for 10 min. Following growth, the substrate was cooled in H₂S to 300 °C to inhibit the decomposition of the MoS₂ film. Electron-beam evaporation (Temescal FC2000 Bell

Jar Deposition System) was used to prepare 20/50 nm Ti/Pt back-gate electrodes on a commercially purchased substrate (thermally grown 285 nm SiO₂ on p⁺-Si). An atomic layer deposition process was then implemented to grow the back-gate dielectric (50 nm Al₂O₃). Access to the individual Pt back-gate electrodes was achieved via a BCL₃ reactive ion etching (RIE) process (Plasma-Therm Versalock 700). The as-grown MoS₂ film was then transferred to the application substrate using a PMMA-assisted wet transfer process.

To define the channel regions, the substrate was spin-coated with PMMA A6 (4,000 rpm for 45 s) and baked at 180 °C for 90 s. The resist was then exposed using a Raith EBP5200 EBL tool and developed using a 1:1 mixture of MIBK and IPA (60 s) and then rinsed using IPA (45 s). The exposed monolayer MoS₂ film was subsequently etched using a sulfur hexafluoride (SF₆) RIE process at 5 °C for 30 s. Next, the sample was rinsed in acetone and IPA to remove the electron-beam resist. A subsequent lithography step was conducted to form source/drain electrodes. The substrate was spin-coated at 4,000 rpm for 45 s with methyl methacrylate EL6 and PMMA A3; following application, these resists were baked at 150 °C for 90 s and 180 °C for 90 s, respectively. EBL was again used to pattern the source and drain, and development was again performed using a 1:1 mixture of MIBK/IPA and an IPA rinse for the same times as previously. Then 40 nm of Ni and 30 nm of Au were deposited using electron-beam evaporation to form the electrodes. A lift-off process was then performed to remove the excess Ni/Au by immersing the sample in acetone for 1 h, followed by IPA for another 30 min to clean the substrate.

To fabricate the top gates, a -8-nm-thick CVD-grown h-BN on Cu foil was transferred to the application substrate using a process similar to that detailed above. EBL was used to define the top-gate electrodes, and electron-beam evaporation was used to deposit Pt to serve as the electrode metal. Finally, the underlying source, drain and back-gate pads were opened using an SF₆ RIE process. The channel length and width of the transistors are $1 \times 5 \text{ }\mu\text{m}^2$.

Device characterization

Surface morphologies and vertical structures of the h-BN-based memristors were characterized by optical microscopy (model DM400, from Leica), SEM (model Supra55/G500, from ZEISS) and cross-sectional TEM (model JEM-2100, from JEOL) with a working voltage of 200 kV and AFM (model Cypher S, from Asylum Research) provided with Olympus tips (model AC240TS-R3) and operated in tapping mode. The cross-sectional TEM sample was prepared by using a focused ion beam (model Helios NANOLAB 450S, from FEI), which can cut ~40 nm thick in the metal/h-BN/metal device, and then these thin lamellas were placed on a copper grid for TEM investigation. The electrical characterization of the devices was carried out using a probe station (model EPS150, from Cascade) connected with a semiconductor parameter analyser (models SCS4200, from Keithley, and B1500A, from Keysight). The light source is a standard lightguide connected white 640 lm LED source (Photonic F3000 from 4H-JENA, colour temperature 5,800 K) at 100% intensity during measurements under the 'light ON' conditions.

First-principles calculations

The atomistic simulations employed DFT within the Gaussian plane-wave method as implemented in CP2K⁴⁴. The electronic exchange-correlation functional was treated within the Perdew–Burke–Ernzerhof⁴⁵ approximation. We additionally employed the semi-empirical DFT-D3 dispersion correction⁴⁶ to include the long-range van der Waals interaction. The double- ζ Goedecker–Teter–Hutter basis set⁴⁷ was used to expand the electronic wavefunctions, with the auxiliary plane-wave basis having a cut-off energy of 600 Ry. The electronic structure was determined self-consistently with a tolerance of 2.7×10^{-5} eV, whereas structure relaxations were carried out with tolerances of 0.25 eV nm⁻¹ and 0.05 GPa for the residual forces and stresses, respectively.

All calculations for h-BN were performed in a hexagonal $6 \times 6 \times 3$ supercell of the bulk unit cell with 432 atoms in total. To model the defects a few atoms wide embedded in the 2D multilayer h-BN, which are suspected to be the initial sites for dielectric breakdown, we created a-BN samples containing 216 atoms from a $3 \times 3 \times 3$ supercell of cubic BN following the melt-and-quench procedure within classical molecular dynamics. The initially crystalline BN was melted and equilibrated at 5,000 K and subsequently quenched with a cooling rate of 5 K ps⁻¹ with time steps of 0.25 fs, the atomic interactions with a suitably parametrized classical potential⁴⁸. At the beginning of the procedure, the cell volume was adjusted to match the experimental density of 2.28 g cm⁻³ of the a-BN films. The resulting structure of a-BN is shown in Fig. 4b.

For calculating accurate electronic structures of h-BN and a-BN, as presented in Fig. 4a,b, we additionally performed single-point calculations with the nonlocal PBE0_TC_LRC hybrid-functional⁴⁹ for the Perdew–Burke–Ernzerhof-relaxed structure. We utilized the auxiliary density matrix method⁵⁰ to efficiently calculate the exact Hartree–Fock exchange on a reduced auxiliary basis set. To characterize and quantify the degree of localization of the electronic states near the band edges, we calculated the IPR based on a decomposition of the resulting molecular orbitals into contributions from each atom. The IPR is a measure for the number of atoms that a particular wavefunction is spreading across. Small IPR values indicate spreading over many atoms. Because we used differently sized cells for h-BN and a-BN, we normalized the IPR (bottom panels of Fig. 4a,b) in such a way that the smallest possible value is 1.

The formation energies of neutral B vacancies in Fig. 4c are obtained as $E^f = E_{\text{defective}}^{\text{tot}} - E_{\text{pristine}}^{\text{tot}} + \mu_{\text{B}}$, where $E_{\text{defective}}^{\text{tot}}$ is the corresponding energy of the pristine relaxed supercell and μ_{B} is the corresponding chemical potential of B. To obtain statistics in the case of a-BN, we removed a B atom at 50 randomly chosen sites to create a vacancy. We used the total energy per atom in the rhombohedral α -allotrope of B for μ_{B} , and hence the obtained formation energies are valid for boron-rich conditions. Note that μ_{B} depends on the conditions (temperature, pressure, and so on) during deposition and thus may vary. However, this variation of μ_{B} affects the formation of B vacancies equally in a-BN and h-BN and thus does not influence our conclusions concerning the large difference in formation energies between both forms of BN.

The process of metal penetration is expected to be complex, with ions moving across an interface that is not experimentally well characterized (see also Fig. 2b). Because this is difficult to describe within DFT, applying the common nudged-elastic band⁵¹ methodology to obtain migration barriers is not promising. Hence, we estimated the penetration barriers based on energetical considerations and by invoking the Bell–Evans–Polanyi principle⁵¹. We therefore calculated the formation energy of a vacancy in the bulk metal as well as the energy required to incorporate the metal atoms in a-BN dielectric. The penetration barrier then was inferred from the reaction enthalpy between the initial (intact metal) and final (metal with vacancy plus metal atom incorporated in a-BN) states of the system.

The vacancy formation energy was calculated in a $4 \times 4 \times 4$ supercell of the respective metal by removing one atom followed by structure relaxation. Due to the relatively large sizes of the Au and Pt atoms, it was assumed that these atoms are primarily incorporated at vacancy sites in a-BN. Hence we calculated the formation energy of a metal atom occupying a boron vacancy. Due to the amorphous nature of a-BN, this was performed for 50 randomly chosen sites, resulting in the barrier statistics presented in Fig. 4e.

Because Au and Pt occur in their +1/+3 and +2/+4 oxidation states, respectively, for most chemical environments, a positive applied bias acting on these positively charged ions will greatly lower the penetration barrier. In Fig. 4e, we conservatively estimated this barrier lowering for a field of 10 MV cm⁻¹ acting on Au³⁺ and Pt⁴⁺ ions across an interface of 0.5 nm assumed thickness.

Data availability

The data that support the plots within this article and other findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

M.L. conceived the idea, designed the experiments and supervised the entire investigation. Y.S. fabricated and characterized most of the devices. K.Z. fabricated and characterized the devices with W electrodes. Y.X. and X.L. fabricated and characterized the devices at high temperature. W.Z. and Y.Y. sporadically helped Y.S., K.Z. and Y.X. with the fabrication and electrical characterization tasks. T.F.S. fabricated the all-CVD devices with supervision from S.D. The MOCVD MoS₂ used in these devices was grown by N.T. with supervision from J.M.R. D.W. and A.H.B. performed the atomistic calculations, and T.K., T.G. and U.S. supervised them. J.B.R., H.T. and S.P. gave comments on the strengths and weaknesses of previous versions of the manuscript. H.W. provided the wafers containing CMOS circuitry. M.L. and Y.S. wrote the manuscript. All the authors read the manuscript and provided comments.

Competing interests

The authors declare no competing interests.

Additional information

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