R(t)-based Spike-Timing-Dependent Plasticity in Memristive Neural Networks

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***Abstract*—Inspired by the human brain, neuromorphic computation should be extremely efficient at very large scales due to inherent parallelism, scalability, and fault and failure tolerance. Spike-Timing-Dependent Plasticity (STDP) is one of the most biologically plausible synaptic learning behaviors. The proposed generic model of time-varying resistance, or R(t) elements in this work can produce STDP in electronic spiking neural networks with memristive synapses that is very similar to that observed in biology. Both pair-based and triplet-based STDP is verified with the proposed generic R(t) model.**

Keywords—Spike-Timing-Dependent Plasticity, R(t) element, memristor, Spiking Neural Network, spike triplet learning.

I. Introduction

Memristive Spiking Neural Networks (SNNs) capable of emulating the Spike-Timing-Dependent Plasticity (STDP) learning rule are promising candidates for brain-inspired low-power energy-efficient neuromorphic architectures [1,2]. However, multiple studies reveal that calcium-based plasticity in hippocampal culture and the visual cortex regions in the brain depend on both spike rate and timing [3,4,5,6]. Pair-based STDP takes into account only the timing of a pre-post pair to explain synaptic weight change, thus failing to produce third-order correlations of input spike trains [7]. Therefore, rate-dependent STDP is required to fully process Spatio-Temporal Patterns (STPs). Triplet-based STDP, which introduces the third spike in either the pre-or post-synaptic neuron is useful to validate rate-dependent STDP [8,9,10]. Moreover, triplet-STDP increases the training stability of neurons in learning STPs for highly fired input spikes [11]. In order to develop a highly realistic neuromorphic system with unsupervised and continuous learning capability, it is important to investigate and modify the learning behavior beyond pair-based STDP. R. Yang et. al physically implemented triplet-STDP with a second-order memristor which requires a complicated digital circuit [12]. It is difficult to design a single device that has the proper first and second-order responses. Other research has demonstrated a floating-gate synaptic implementation along with a mathematical procedure to control gate voltage to generate triplet-STDP [13]. This requires additional logic gate components and a guideline for plausible neuromorphic architecture is missing. Overall, it is much more difficult to design a single memristive device with drift/diffusion than it is to build an external circuit that captures those behaviors and that can be tuned to provide the right response based on whatever memristive device is attached. Therefore, further investigation for alternative approaches to establishing triplet-STDP with minimum circuit elements and commercially available memristor model incorporative SNNs is required. An R(t) element is any time-varying resistance that can be used in conjunction with memristors to vary the resistance change with respect to time for implementing frequency-dependent STDP [14]. The advantage of including this element is a dramatic reduction in complexity compared to pulse-shaping circuits. A generic model explaining the time-dependent change in effective resistance of R(t) elements is required as a reference for understanding the controlling circuit parameter and establishing different synaptic learning behavior in SNNs. Although at this moment, it cannot be guaranteed that the model can always be implemented with standard CMOS circuitry, the model serves as a behavioral guideline for physical implementations. There's room for analyzing the downsides of inclusion R(t) elements in neuromorphic architecture in future.

In this work, both pair- and triplet-based STDP learning behavior from R(t)-based neural networks have been explored in TSMC 180 nm technology. Furthermore, a generic model of R(t) elements is presented and pair-based STDP is generated using the same technology. Results reveal that an ideal R(t) element attached to pre-and post-synaptic learning circuits, along with a memristor device can produce perfect symmetric STDP in neural circuits. The analysis presented in this work can be an aid to realize the dependency of the learning behavior of SNNs on different neuronal variables and thereby help design faster and more efficient brain-emulating electronic circuits.

II. Methodology

A. Neural network design

All SNNs consist of neurons connected together through synapses. This work analyzes a single memristive synapse connecting pre- and post-synaptic neurons via two R(t) elements on both sides of the synapse. Fig. 1. Shows a pseudo-schematic diagram of the SNN network building block used for this work. The memristor and the R(t) elements are modeled in Verilog-A. Memory storage and processing happen inside the memristor without the necessity of a pulse-shaping network. The conductance of the memristor defines the state of the device. The state (W/D) is defined as the normalized conductance swing between 0 to 1.

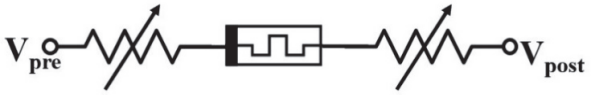

Fig. 1: Pseudo-schematic of a neural circuit with time-dependent resistance, or R(t) elements to control modification and learning in a memristive synapse.

B. Memristor model

In this work, a non-linear drift model of a TiO_2-based memristor is used [2-3]. The memristor current is determined by an auxiliary circuit with a dependent current source and a 1 F capacitor. The voltage across the auxiliary capacitor controls the memristor voltage and state variables of the device. The I-V characteristics of this memristor model and a more detailed description of parameters are provided in ref. [3].

C. R(t) element

Previous work has demonstrated learning in SNNs in which the R(t) element was either a short-term charge-trapping memory or a circuit consisting of MOSFETs and resistors in which the effective resistance changes from a maximum to a minimum value [11,12]. To establish a standard asymmetric-Hebbian STDP learning behavior in the SNN, we need to modify the R(t) circuit. The process starts with a simplified model of the circuit replacing the MOSFET-based current mirror circuit with a voltage-controlled current source (Fig. 2).

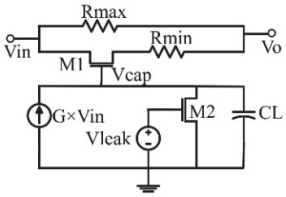

Fig. 2: (a) Simplified model of R(t) element with a voltage-controlled current source.

The current of the source is dependent on the input voltage by scaling of G. Resistors R1 and R2 from the original circuit are regarded as R_{max} and R_{min} in the simplified model.
In the simplified model, the voltage across the capacitor C_L (V_{cap}) controls changes in the resistance of the element over time. V_{cap} is dependent on scaling parameter G and the leakage voltage V_{leak}.

Before further simplification, we analyzed how the charging of the capacitor is affected by the variation of these parameters. The leakage time constant of the capacitor is referred as τ_{leak}. The value of the parameters used for this analysis are presented in Table I.

TABLE 1. LIST OF PARAMETERS OF THE R(T) CIRCUIT

Parameters	Value
G ($\mu\Omega^{-1}$)	1
Δ t (ms)	5
C_L(pF)	1
R_{max}(kΩ)	100
R_{min}(kΩ)	1
V_{leak} (mV)	40
V_{th} (mV)	700
Vdd(V)	2

In Fig. 3(a), τ_{leak} is plotted against V_{leak} keeping the voltage in mV range as V_{leak} is described as a very small voltage in the original circuit. The decrease of τ_{leak} with the increasing V_{leak} verifies the assumption. Again, the voltage V_{cap} is plotted with respect to the scaling parameter, G (Fig. 3(b)). These results are helpful to determine the ideal values of the parameters while designing the R(t) circuits.

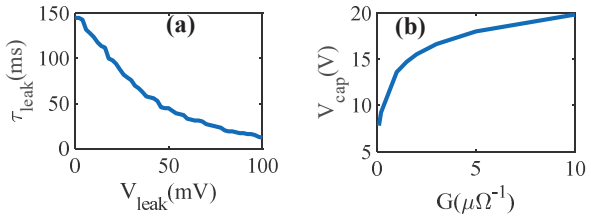

Fig. 3: (a) Effect of changing leakage time constant on synaptic weight, (b) Effect of changing current injection of synaptic weight.

The generic model of the R(t) element shown in Fig. 4 is designed in a way that the effective resistance is dependent on the input voltage and swings between a high resistance $R_{max}(1/\sigma_{min})$ and minimum resistance $R_{min}(1/\sigma_{max})$. The effective resistance of the element can be equated as,

$$R(t) = \frac{1}{\sigma(t)} \quad (1)$$

$$\sigma(t) = \sigma_{min} + \gamma \times \sigma_{max} \quad (2)$$

Here, γ is a time-dependent parameter that can be expressed as,

$$\gamma = \frac{V_{cap}(t)}{V_{cap}(max)} \quad (3)$$

V_{cap}(max) is the maximum capacitor voltage gained after charging for a duration of t_{charge}. This can be expressed as,

$$V_{cap}(max) = \frac{(G \times Vdd \times t_{charge})}{C_L} \quad (4)$$

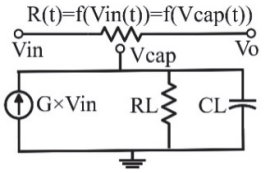

Fig. 4: Schematic of the generic model of R(t) element.

From the final generic model of the R(t) (Fig. 4), as the input to the circuit changes, the voltage across the capacitor changes, and the conductance of the R(t) element changes based on equation (4). To physically implement an R(t) element following the generic model, a nanoscale transistor having low threshold and a linear current-gate voltage relationship in compatible technology is required in place of MOSFET M1 in Fig. 2. Further consideration is required to implement all the resistances with transistors.

III. RESULTS & DISCUSSIONS

Both pair-based and triplet-based STDP are simulated using the SNN building block shown in Fig. 1. The details results are presented in the following subsections.

A. Pair-based STDP

Initially, we tested the network with the compound R(t) element [14] in TSMC 180nm technology. The effective resistance of the circuit with a single pulse is generated in TSMC 180 nm technology as shown in Fig. 5. The values used for constant parameters are given in TABLE I.

The neural network is analyzed with a generic R(t) element and the results are shown in Fig. 5. A single pulse is applied as both the pre-and post-synaptic neural signals. For an initial normalized weight of 0.44, the voltage across the memristor

changes during a 5 ms timing difference between pre-and post-synaptic signals. The state variable W/D changes accordingly within this time interval.

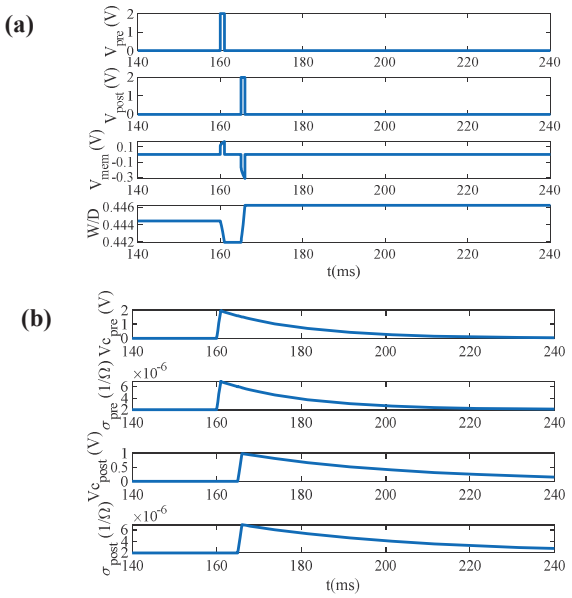

Fig. 5: (a) Pre-Post spike input pair, memristor voltage, memristor weight change, (b) Capacitor voltages, and the conductance of pre-and post-synaptic R(t) circuits.

In Fig. 5(b), The effective conductance for both the pre-and post-synaptic neural circuits is plotted following the capacitor voltage. As the capacitor voltage changes exponentially with time after a pre-post pair, the conductance exponentially changes from a maximum to a minimum value. To verify STDP, the weight change (ΔW/D) across the memristor is plotted with respect to the timing difference (Δt) in Fig. 6 for both the compound and generic R(t) elements.

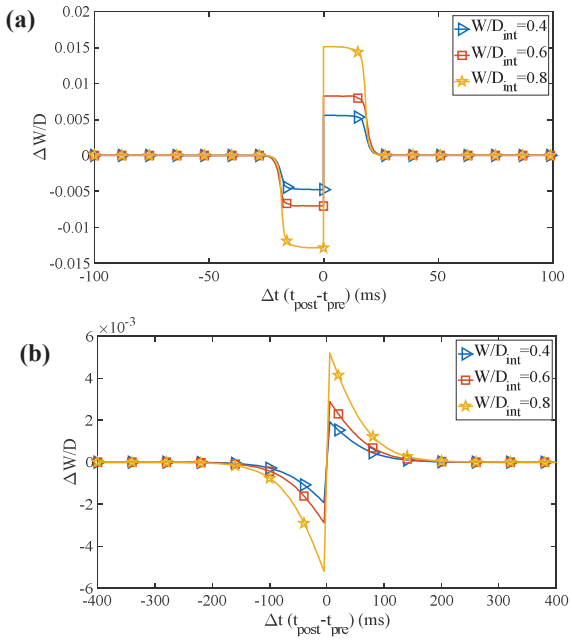

Fig. 6: Pair-based STDP (a) With MOSFET-based compound R(t), (b) With generic R(t) model with R_{min}=200kΩ and R_{max}=500kΩ.

From Fig. 6, it is clear that STDP using the generic R(t) element better resembles biological STDP behavior. It is possible to get different types of symmetric and asymmetric STDP behavior from this R(t) model by tuning the maximum and minimum resistances as well as the conductance function.

B. Triplet-based STDP

To generate triplet-based STDP, researchers from different groups modeled the timing differences differently, using either one timing or two timings [8,9,10,11,16]. In this work, two timing differences between pre- and post-synaptic neurons are considered and based on the position of the third spike, the triplet signals are categorized into six patterns to test our network. For all the patterns, the first timing difference, Δt_1 is the timing difference between the arrival time of the first and second spikes, and the second timing difference, Δt_2 is the timing difference of the arrival time of the second and third spikes. In Fig. 7, the weight change across the memristor due to a triplet input; in this case a Pre-Post-Pre triplet is plotted. Similar to Pre-post input, the effective conductance for both the pre-and post-synaptic neural circuits is plotted following the capacitor voltage (Fig. 7(b)).

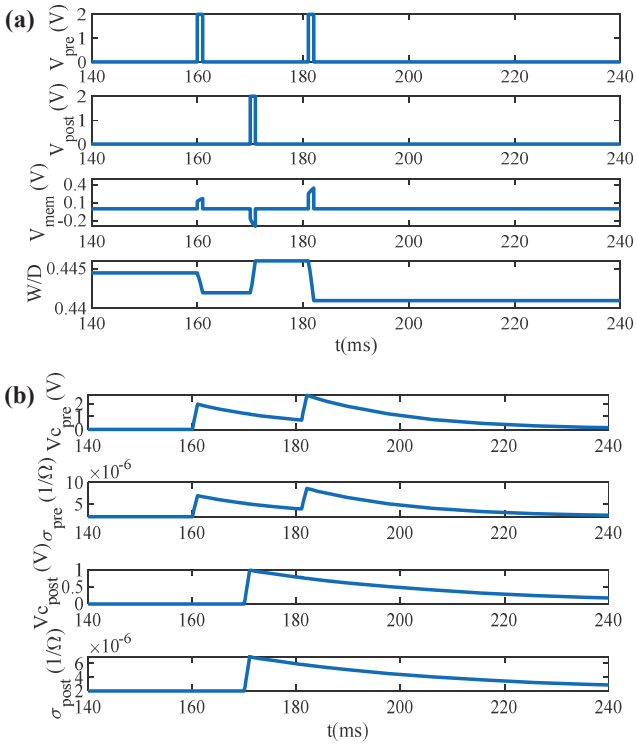

Fig. 7: (a) Pre-Post-Pre triplet input spikes, memristor voltage, memristor weight change, (b) Capacitor voltages, and the conductance of pre-and post-synaptic R(t) circuits.

The weight change across the memristor is now dependent on the arrival of all three spikes. To demonstrate the triplet-based STDP learning behavior, the weight change across the memristor was plotted with respect to both the timing differences (Δt_1, Δt_2) in Fig. 8. The colormap shows the change of weight across the memristor.

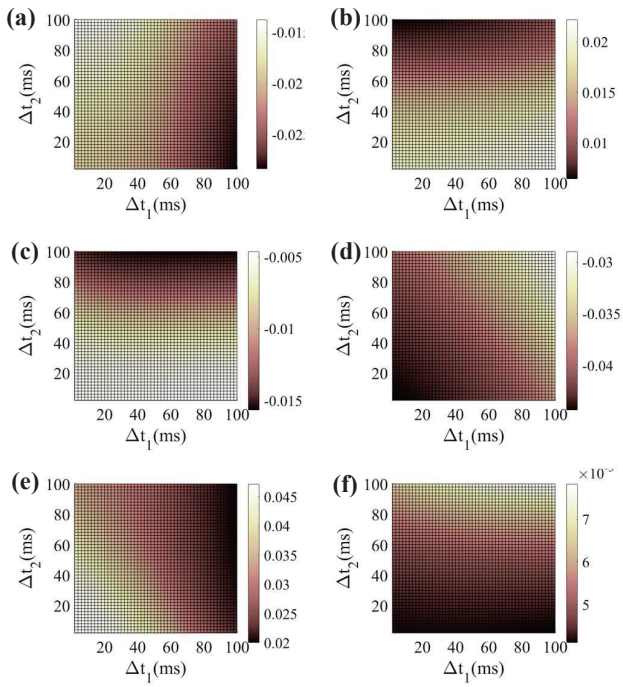

Fig. 8: Triplet-based STDP (a) Pre-Post-Pre, (b) Post-Pre-Post, (c) Pre-Pre-Post, (d) Post-Pre-Pre, (e) Pre-Post-Post, (f) Post-Post-Pre.

From Fig. 8(a-b), it is evident that the synaptic weight change can alter polarity due to considering the third spike, therefore resulting in a different ΔW/D window than pair based STDP which matches the pattern shown in refs. [11,16]. With the change in timing difference between consecutive pre- or post- pulses, ΔW/D changes for a single time difference between pre-post pair (Fig. 8(c-f)). Therefore, the frequency of pre- and post-synaptic spikes is impacting the synaptic weight, which does not happen in pair-based STDP.

IV. Conclusions

The STDP learning behavior from R(t)-based SNNs was analyzed. A generic model of R(t) elements was developed that paves the way for further modification in the actual architecture. Pair and triplet-based STDP with a generic R(t) model were investigated, demonstrating clear asymmetric temporal integration and learning that is dependent on the third spike in the set. Future work will investigate the effect of spike frequency on STDP in R(t)-based SNNs, the dependence of the shape of the R(t) function and will use other more realistic memristor models.

Acknowledgments

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