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iant memory window performance and low power consumption of hexagonal boron nitride monolayer atomristor

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Two-dimensional (2D) monolayers have gained signi cant attention as ultrathin active layers for fabricating atomic-scale memristor (atomristor) structures due to their crystalline structures and clean surfaces. This study reports on the giant memory window performance and low power consumption of the atomristor structures using a hexagonal boron nitride (h-BN) monolayer and symmetric silver (Ag) metal electrodes through a polypropylene carbonate (PPC) assisted transfer method. The h-BN atomristor exhibits the highest memory window (~4 × 10^9), the lowest leakage current (~0.24 pA), and the lowest power consumption (~3 × 10 ^{14} W) compared to the other 2D atomristors. Furthermore, the h-BN atomristor achieves signi cant endurances and yields of up to 10,000 switching cycles and 77%, respectively, due to the superior thermomechanical properties of the PPC support layer for transferring ultrathin and large-area h-BN monolayers. These results represent a signi cant step toward the realization of high-performance and energy-ef cient neuromorphic computing circuits based on 2D monolayers.

Two-dimensional (2D) materials have emerged at the forefront of material science research, promising advancements in nanoelectronics and nanotechnologies[1 13]. These 2D materials, including graphene, transition metal dichalcogenides (TMDs), and hexagonal boron nitride (h-BN), exhibit outstanding electrical, mechanical, and optical properties not readily found in their three-dimensional (3D) bulk counterparts[14 20]. Their ultrathin nature enables the fabrication of atomic-scale devices and circuits for high-density and low-power electronic applications[21 27]. However, unlike 3D bulk materials, 2D materials are typically grown on wafer-scale substrates through chemical vapor deposition (CVD), molecular beam deposition (MBE), or metal-organic chemical vapor deposition (MOCVD) and subsequently transferred to target substrates through dry or wet transfer methods with the aid of numerous polymer support layers, such as polydimethylsiloxane (PDMS), polymethyl methacrylate (PMMA), or polystyrene (PS)[28 37]. While these 2D materials possess favorable material properties, such as a highly crystalline lattice and clean surface, various morphological defects can arise during their growth or transfer processes to fabricate 2D devices and circuits. The localized or interfacial defects, such as wrinkles and contaminant particles, created during the transfer processes can signi cantly degrade the performance of these devices and circuits[38 43]. In particular, in the vertical metal-insulator-metal (MIM) memristor structures, cracks and wrinkles can lead to signi cant yield degradation, while contaminant particles can result in unclean interfaces and variability[44,45]. Therefore, it is crucial to select the transfer support layer based on how intact it can cleanly transfer ultrathin 2D materials.

The memory resistive switching effects have been demonstrated by atomic-scale memristor (atomristor) metal-insulator-metal (MIM) structures of 2D TMD and h-BN monolayers[46 52]. The memory switching mechanism of the 2D atomristors using gold (Au) electrodes has suggested that the resistive switching effects are attributed to the adsorption/desorption of metal atoms into the intrinsic vacancies of the monolayers[53,54]. Furthermore, recent research on atomristors using silver (Ag) electrodes has demonstrated that the transition between volatile and nonvolatile switching is attributed to the thickness and stiffness of the conductive bridge formed at the polymeric-residue-contaminated interface between the monolayer and electrode[55]. However, ironically, most atomristors have faced signi cant endurance and yield issues due to the extremely thin nature of the monolayers[56,57]. Therefore, it is necessary to nd a new transfer support layer that can minimize the wrinkles and contaminant particles in the metal-insulator-metal structures created during the transfer processes of these ultrathin monolayers.

Recently, Mondal et al. reported that a polypropylene carbonate (PPC) support layer signi cantly reduce wrinkles and residues than the PMMA support layer during the wet transfer process of the molybdenum disul de

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(MoS_2) monolayer[58]. This prior works aids in understanding that the PPC support layer was able to acquire fewer wrinkles during the transfer and annealing processes due to its higher elastic modulus and lower thermal expansion coef cient than the PMMA support layer and to minimize residues due to its superior solubility in solvent stripper[58–62].

This work investigates the giant memory window performance and low power consumption of the nanoscale nonvolatile atomristor structures using the h-BN active monolayer and Ag metal electrodes through a PPC-assisted wet transfer method. In particular, we focused on the minimization of cracks, wrinkles, and residues that have the most signi cant influence on the endurance and yield of the atomristors through polymer support layer and solvent stripper replacements. The endurance and yield of the h-BN atomristor showed a noticeable improvement while maintaining the highest memory window and the smallest leakage current among other 2D atomristors. This marks the rst successful demonstration of a PPC-assisted wet transfer method for transferring the ultrathin and large-area h-BN monolayer. We have demonstrated the enhancements in switching and reliability performances of the vertical atomristor structures for practical high-performance and energy-ef cient neuromorphic computing systems.

Results

Device characterization and fabrication of hexagonal boron nitride atomristor

Figure 1a and b provide the schematic illustrations of the h-BN atomristor using symmetric Ag metal electrodes. The h-BN atomristor was fabricated by sandwiching the h-BN monolayer between the top and bottom Ag electrodes to stimulate the formation and breakage of conductive bridges at either the top or bottom electrodes (Supplementary Fig. 1)[54,55]. Figure 1c presents the optical microscopy (OM) image of the h-BN atomristor. The junction area of the MIM structure is measured to be around 0.40×0.40 m^2. Figure 1d shows the atomic force microscopy (AFM) images of the h-BN atomristor on the diamond substrate. The thicknesses of the top and bottom Ag metal electrodes are measured to be around 90 nm and 50 nm, while the thickness of the h-BN monolayer on the clean SiO_2/Si substrate is estimated to be about 0.51 nm due to the van der Waals gap between the monolayer and substrate (Supplementary Fig. 2)[51,55]. Figure 1e shows the atomic-resolution transmission electron microscopy (TEM) image of the h-BN monolayer on the SiO_2/Si substrate. The lattice constant of the honeycomb structure is around 2.5 Å, in agreement with the theory[19]. Figure 1f shows the Raman spectra of the h-BN monolayer with a characteristic peak around 1360 cm^{-1} consistent with the material structure[63].

Hexagonal boron nitride monolayer wet transfer using PPC support layer

Figure 2a and b show the OM images of the bottom Ag electrodes on the diamond substrates after wet transfer of the h-BN monolayer using PPC and PMMA support layers (Supplementary Fig. 3). Unlike the PMMA-coated substrate, there was no need to scratch the sidewalls of the PPC-coated substrate with a diamond scriber due to the high viscosity of the PPC support layer (Supplementary Fig. 4). As a result, the sidewalls of the transferred PPC/h-BN stacking layer were signi cantly cleaner than those of the transferred PMMA/h-BN stacking layer on the target substrate (Supplementary Fig. 5). It was found that the PPC/h-BN stacking layer on the diamond substrate has no wrinkles, while the PMMA/h-BN stacking layer has tens of micrometers of wrinkles in a region of interest. This suggests that the stiffness of the PPC support layer is much greater than that of the PMMA support layer because elastic modulus of the PPC support layer (~993 MPa) is higher than that of the PMMA support layer (~8 MPa)[34,59,60,64]. Furthermore, the PPC/h-BN and PMMA/h-BN stacking layers were annealed to remove water droplets after they were transferred from deionized (DI) water to the diamond substrates. The water droplets were removed without the contraction of the PPC/h-BN stacking layer, while the PMMA/h-BN stacking layer

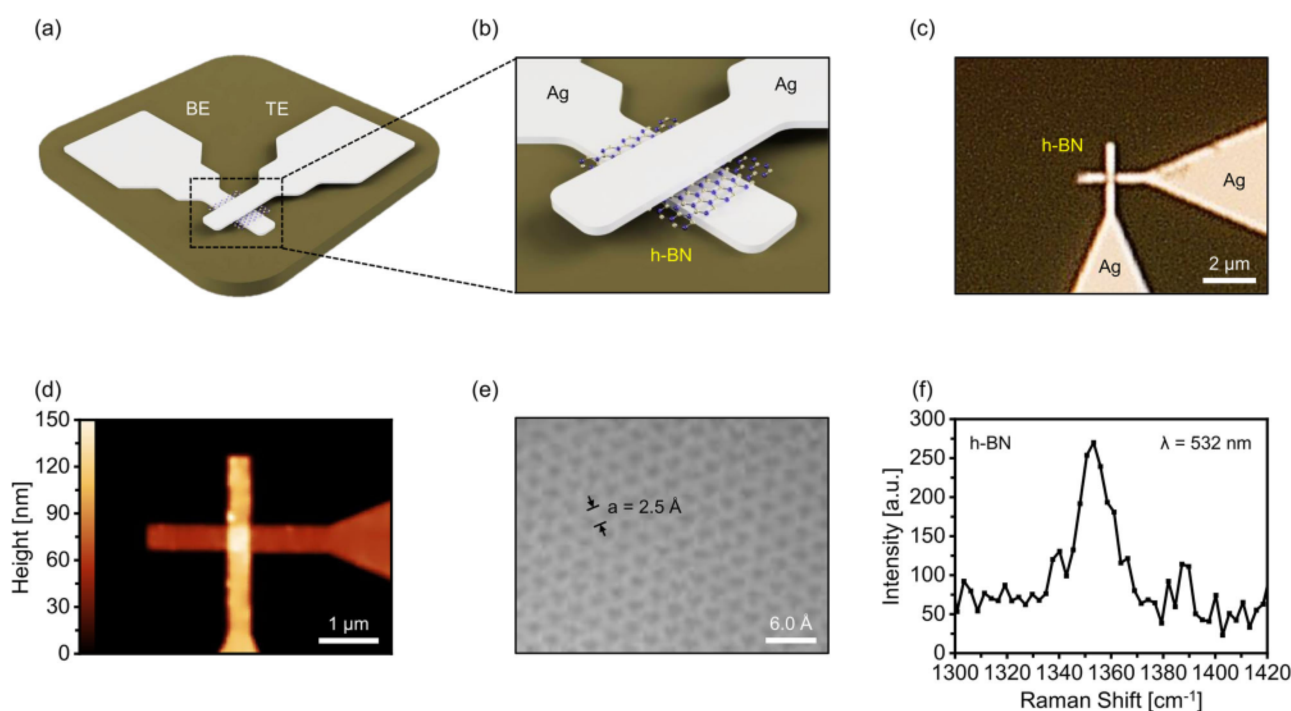

Fig. 1 | Device and material characterizations of two dimensional hexagonal boron nitride atomristor using silver metal electrodes. **a**, **b** Schematic illustrations of the h-BN atomristor using the Ag electrodes. **c** OM image of the h-BN atomristor on the polycrystalline diamond substrate. The junction area of the atomristor structure is measured to be around 0.40×0.40 μm^2. **d** Topological AFM image of the h-BN atomristor on the diamond substrate. The thicknesses of top and bottom Ag metal electrodes are measured to be around 90 nm and 50 nm. **e** Atomic-resolution TEM image of the h-BN monolayer on the on the SiO_2/Si substrate. Reproduced with permission from GrollTex, Inc. **f** Raman spectra of the h-BN monolayer on the on the SiO_2/Si substrate consistent with its Raman mode.

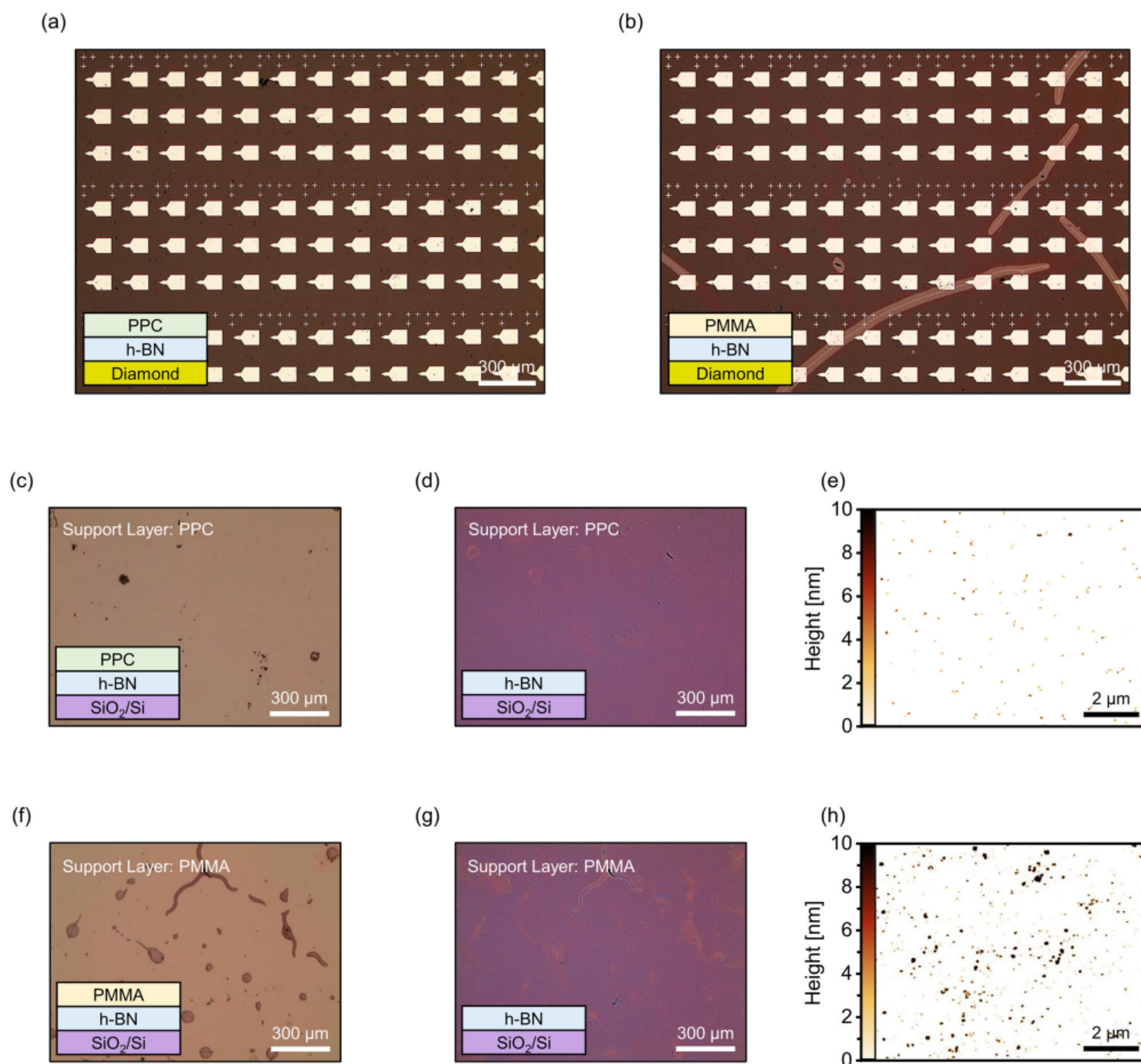

Fig. 2 | Wrinkle free and residue free PPC assisted wet transfer method of hexagonal boron nitride monolayer. a, **b** OM images of bottom Ag metal electrodes on the substrate after transferring h-BN monolayer using PPC and PMMA support layers. **c** **e** High-resolution OM and topological AFM images of h-BN monolayer on SiO_2/Si substrate before and after removing the PPC support layer. The area coverages of the transferred h-BN monolayer and PPC residues are estimated to be around 96 and 0.55 . **f** **h** High-resolution OM and topological AFM images of h-BN monolayer on the same substrate before and after removing the PMMA support layer. The area coverages of the transferred h-BN monolayer and PMMA residues are estimated to be about 90 and 2.1 .

contracted and formed micrometers of wrinkles. This is because the thermal expansion coef cient of the PPC support layer is close to that of the h-BN monolayer and is much lower than that of the PMMA support layer[34,58,65]. However, it was challenging to visually differentiate the transferred h-BN monolayer from the diamond substrate after dissolving the polymer support layers.

To further investigate this, we transferred the PPC/h-BN and PMMA/h-BN stacking layers onto bare SiO_2/Si substrates to characterize the physical and chemical properties of each polymer support layer. The h-BN monolayer transfer is more likely to create many cracks than the h-BN multilayer transfer during the dissolution of the polymer support layers, so we chose acetone as solvent stripper rather than anisole (~1.3 kPa) and remover PG (~0.039 0.043 kPa) due to its higher vapor pressure of 25 kPa at room temperature (Supplementary Fig. 6). Figure 2c and d show the OM images of the transferred h-BN monolayer on the bare SiO_2/Si substrate before and after dissolving the PPC support layer. Figure 2e presents the topological AFM images of the remaining PPC residues on the transferred h-BN monolayer on the SiO_2/Si substrate. Figure 2f and g shows the OM images of the transferred h-BN monolayer on the same substrate before and after removing the PMMA support layer. Figure 2h represents the topological images of the remaining PMMA residues on the transferred h-BN monolayer on the same substrate. The area coverage of the PPC-assisted transferred h-BN monolayer is measured to be about 96 , while that of the PMMA-assist transferred monolayer is estimated to be around 90 (Supplementary Fig. 7). It is noticeable that the cracked and wrinkled areas of the PPC-assisted transferred h-BN surface are much smaller than those of the PMMA-assisted transferred surface. Furthermore, the area coverages of the PPC and PMMA residues are extracted to be around 0.55 and 2.1 (Supplementary Fig. 8). It has been found that both the number and size of the PPC residues are signi cantly less than those of the PMMA residues. This is because the PPC support layer has better solubility in acetone than the PMMA support layer, thereby minimizing polymer residues that could degrade atomristor performance[58,61,62].

Memory window performance of hexagonal boron nitride atomristor using silver metal electrodes

Figure 3a shows the static current-voltage (I-V) characteristics of the 0.40×0.40 m^2 h-BN atomristor using symmetric Ag electrodes at 1 mA current compliance. The h-BN atomristor exhibits nonvolatile bipolar resistive switching behaviors with a giant memory window of more than 10^9, while the operating voltage and leakage current is measured to be less than 0.16 V and 5.7 pA. Figure 3b provides the statistical SET voltage (V_{SET}) and RESET voltage (V_{RESET}) distributions of the 43 atomristors at the same current compliance and atomristor area. Taking advantage of the PPC support layer, we fabricated 56 atomristors on the same substrate and improved the yield rate to 77 (= 43/56 × 100) (Supplementary Fig. 9). The mean (μ) values of V_{SET} and V_{RESET} are estimated to be about 0.96 V and 0.25 V, and the standard deviation ( ) values of these switching voltages are extracted to be around 0.44 V and 0.13 V with the coef cients of variation (V) of 46 and 52 . Figure 3c presents the statistical high-resistance-state resistance (R_{HRS}) and low-resistance-state resistance (R_{LRS}) distributions of the same atomristors at 1 mA current compliance. The μ and values of R_{HRS} are measured to be about 440 GΩ and 890 GΩ with a V of 200 , while these values of R_{LRS} are calculated to be around 230 Ω and 170 Ω with a V of 71 .

Figure 3d and e present the microsecond input voltage (V_{IN}) and output current (I_{OUT}) pulse waveform characteristics of the h-BN atomristor for both SET and RESET processes. The V_{SET} and V_{RESET} pulse amplitudes were set to approximately 2.0 V and 1.0 V with the same pulse width of 100 µs. The pulse amplitude of the READ voltage (V_{READ}) was set to around 0.2 V before and after the V_{SET} and V_{RESET} voltage pulses. The switching speeds are measured to be about 57 µs for the SET process and 1.7 µs for the RESET process, at which the Ag metal atom begins to move after the voltage pulse is applied[66 68]. Interestingly, the switching speed of the second SET process (~14 µs) is 4 times faster than that of the rst SET process (~57 µs) because the remaining Ag metal atoms were signi cantly utilized to form the conductive bridge between the surfaces even at lower energies (Supplementary Fig. 10)[55]. Furthermore, it clearly showed the transition for each resistance state through the I_{OUT} pulse measurements during subsequent READ processes. This indicates that a transition from high-resistance-state (HRS) to low-resistance-state (LRS) requires a greater pulse amplitude and a broader pulse width of input voltage than a transition from LRS to HRS.

Figure 3f shows the microsecond consumed power and energy characteristics of the h-BN atomristor for the initial SET process. The V_{IN} pulse waveform was multiplied by the I_{OUT} pulse waveform to extract the power consumption during each switching process, and the energy consumption was calculated by integrating this power consumption over the switching time[50]. The energy consumption was measured at 50 nJ for the initial SET process and 23 nJ for the subsequent RESET process (Supplementary Fig. 11). This demonstrated that the energy barrier for the initial SET process is more signi cant than that for the subsequent RESET process, attributed to a mechanism where the Ag metal atoms have a strong tendency to aggregate into the clustered Ag metal electrode[55,69]. The total energy consumption for the second SET process increased from 60 nJ to 81 nJ through multiple reaction steps of conductive bridge formation (Supplementary Fig. 12)[55]. The remaining Ag metal atoms are likely to reduce the energy barrier to form the conductive bridge, so the conductive bridge for the second SET process was formed much thicker and faster than that for the initial SET process, even under the same pulse conditions[55].

Memory endurance performance of hexagonal boron nitride atomristor using silver metal electrodes

Figure 4a shows the ramped-voltage-stress (RVS) endurance performance of the h-BN atomristor at 1 mA current compliance. The RVS endurance is measured to be 139 switching cycles. The statistical V_{SET}

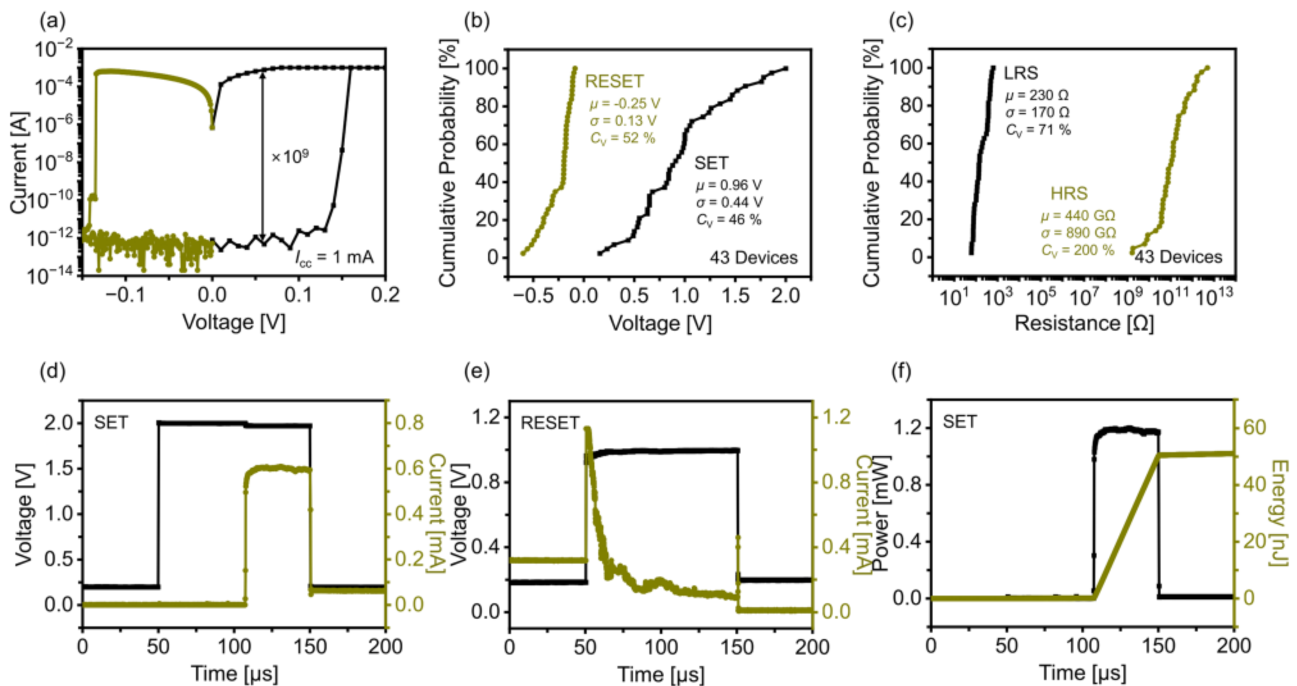

Fig. 3 | Memory window switching performances of hexagonal boron nitride atomristor using silver metal electrodes. a Static I-V characteristics of the 0.40×0.40 µm^2 h-BN atomristor. **b**, **c** Statistical V_{SET}/V_{RESET} and R_{HRS}/R_{LRS} distributions of 43 h-BN atomristors. The μ and values of V_{SET} are measured to be 0.96 V and 0.44 V, while these values for V_{RESET} are estimated to be 0.25 V and 0.13 V. The μ values of R_{HRS} and R_{LRS} are extracted to be 440 GΩ and 230 Ω, but the values of those state resistances are measured to be 890 GΩ and 170 Ω. **d**, **e** Microsecond V_{IN} and I_{OUT} pulse waveform characteristics of the h-BN atomristor during the SET and RESET processes. The V_{SET} and V_{RESET} pulse amplitudes were set to approximately 2.0 V and 1.0 V with the same pulse width of 100 µs. The V_{READ} pulse amplitude was set to around 0.2 V before and after the V_{SET} and V_{RESET} pulses. The switching speeds of the initial SET and RESET processes are measured to be about 57 µs and 1.7 µs, respectively. **f** Microsecond consumed power and energy characteristics of the h-BN atomristor during the initial SET process. The consumed energies are calculated to be 50 nJ for the SET process.

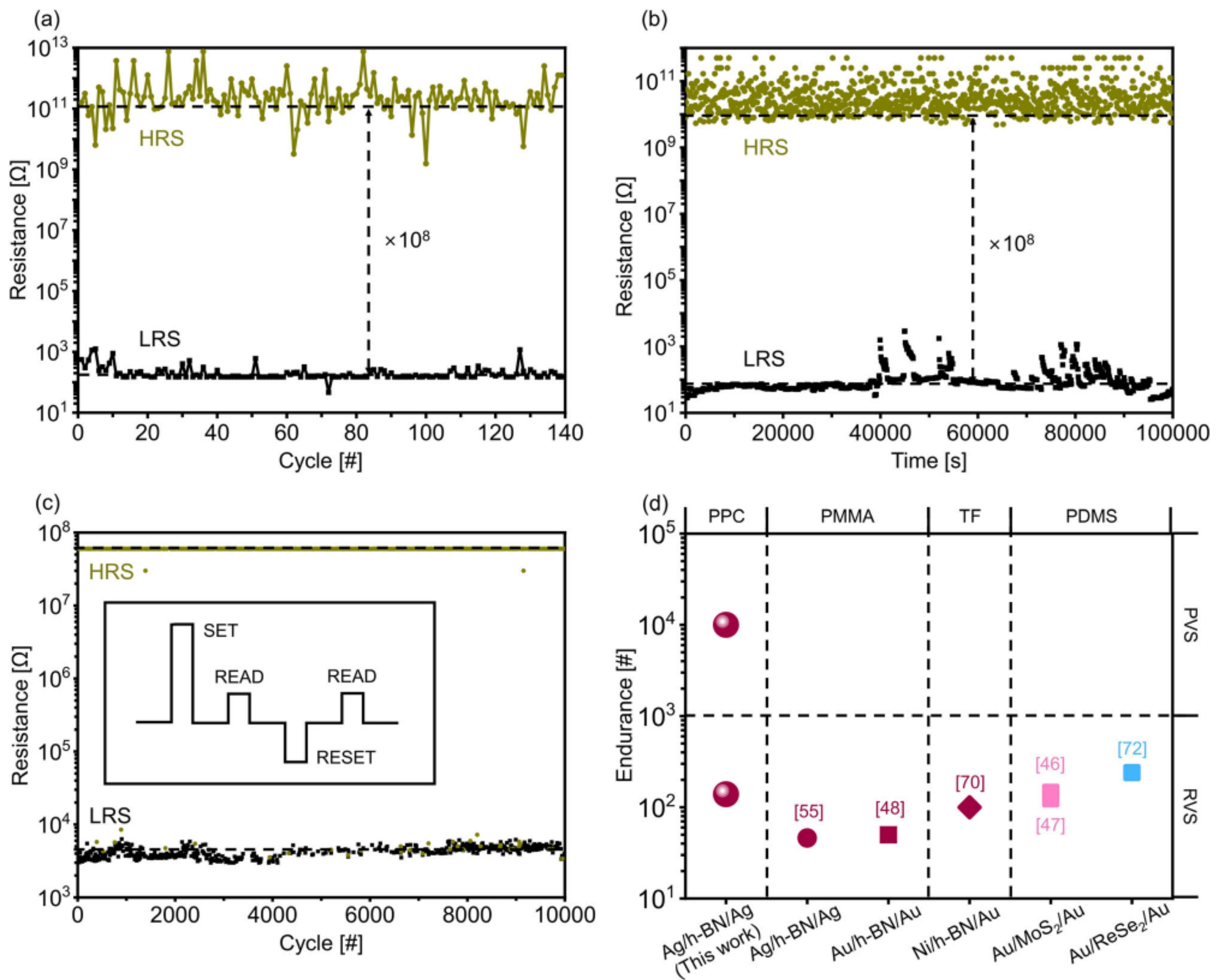

Fig. 4 | Memory endurance and retention performances of hexagonal boron nitride atomristor using silver metal electrodes. a RVS memory endurance performance of the h-BN atomristor. The RVS endurance is measured to be 139 switching cycles with a memory window of 10^8. **b** RVS memory retention characteristics of the h-BN atomristor. The memory retention time is estimated to be more than 10^5 s (~28 h). The dashed lines are a visual guide. **c** PVS endurance performance of the h-BN atomristor. The V_{SET} and V_{RESET} pulse amplitudes are set to 1.0 V and 0.4 V with the V_{READ} pulse amplitude of 0.3 V. Each pulse width and period are set to 30 ms and 50 ms. The PVS endurance is measured to be more than 10,000 switching cycles. **d** RVS and PVS memory endurance characteristics of the atomristors using various monolayers, electrodes, and transfer support layers.

and V_{RESET} distributions of the h-BN atomristor were measured at 139 switching cycles through the RVS endurance measurements. The μ and values of V_{SET} are estimated to be about 3.3 V and 1.7 V with a V of 52 , but those values of V_{RESET} are extracted to be about 1.7 V and 1.4 V with a V of 83 (Supplementary Fig. 13a). The statistical R_{HRS} and R_{LRS} distributions of the h-BN atomristor were also measured at the same switching cycles through the same measurements. The μ values of R_{HRS} and R_{LRS} are calculated to be around 550 GΩ and 220 Ω, and the values of each state resistance are extracted to be about 1.2 TΩ and 180 Ω with a V of 220 and 80 (Supplementary Fig. 13b). It was found that the statistical distributions of resistance for each state are almost the same between device-to-device and cycle-to-cycle variability results because the maximum current was restricted by the current compliance setting of the measurement equipment[46 48]. Figure 4b presents the memory retention characteristics of the h-BN atomristor at 1 mA current compliance. The memory retention was measured to be more than 10^5 s (~28 h) with a memory window of 10^8. This demonstrates that the h-BN atomristor using the PPC support layer showed improved endurance and retention performances compared to that using the PMMA support layer, even under the same fabrication and measurement conditions because the number and size of the PPC residues are signi cantly smaller than those of the PMMA residues after dissolving with acetone. This reduced residual effect causes the decreased interfacial distance between the h-BN and Ag surfaces and forms more stable conductive bridges between the surfaces[51,55]. Furthermore, we conducted the pulsed-voltage-stress (PVS) endurance measurements of the h-BN atomristor using repeated V_{SET} and V_{RESET} pulses. The PVS endurance was measured to be more than 10,000 switching cycles, but the memory window was reduced to about 10^4 due to the instrumental limitation of the measurement equipment (Fig. 4c). The V_{SET} and V_{RESET} pulse amplitudes were set to 1.0 V and 0.4 V with the same pulse width and period of 30 ms and 50 ms. This indicates that reliable PVS endurance measurements were achievable even in the Ag/h-BN/Ag atomristor structures because the reduced interfacial distance between the h-BN and Ag surfaces decreased the energy barrier for the dissociation of Ag atoms (Fig. 4d)[55]. However, further characterization is needed to investigate the combined mechanisms of defect and interface engineering in the atomristor structures.

Figure-of-merit comparison of memory window and endurance performances of two-dimensional monolayer atomristors

Figure 5 represents the figure-of-merit comparisons of nonvolatile memory switching performances of the h-BN atomristor using symmetric Ag electrodes with other 2D monolayer atomristors. Our best h-BN atomristor shows the highest memory window of 4×10^9 and relatively small switching voltages of less than 0.16 V, attributed to the high band gap of the h-BN monolayer (~6.0 eV) and low energetics of the Ag metal electrodes. The μ values of device-to-device variability results are also represented by the memory window of 2×10^9, along with the switching voltages and power consumption for SET and RESET processes. In addition, the h-BN atomristor using the PPC-assisted wet transfer method (139 switching cycles) has RVS endurance performance more than 3 times better than that using the PMMA transfer method (46 switching cycles)[55]. Furthermore, the h-BN atomristor using symmetric Ag electrodes demonstrates significant improvements in switching voltage and leakage current compared to the atomristor using symmetric Au electrodes[48,49,51,54,55]. This indicates that symmetric Ag electrodes have greater advantages over symmetric Au electrodes in memory devices and applications. On the other hand, the MoS_2 atomristor using symmetric Ag electrodes exhibits low switching voltages of less than 1.0 V when subjected to the same compliance current. However, it demonstrates a limited memory window performance of 10^2, due to the relatively small band gap of the MoS_2 monolayer (~1.8 eV)[46]. This finding suggests that the memory window is influenced by the combination of 2D monolayer and metal electrodes, while the endurance is determined by the stability of conductive bridge formation in the atomristor structures (Table 1). However, further research into asymmetric electrode structures is needed to characterize the detail switching mechanisms in the atomristor structures that use 2D monolayers as the active layers.

Figure 5b represents a comparison of the figure-of-merit SET and RESET power consumptions of the 2D atomristors, as measured through RVS measurements. Our best h-BN atomristor using symmetric Ag electrodes exhibits the lowest RESET power consumption of around 3×10^{-14} W, attributed to the low V_{RESET} of −0.14 V and high-resistance-state current (I_{HRS}) of around 0.24 pA. Moreover, our best h-BN atomristor shows the lowest SET power consumption of around 2×10^{-4} W among other 2D atomristors at the same current compliance, attributed to the low V_{SET} of 0.16 V. The μ value of 10^{-13} W in RESET power consumption also appears lower than that of other 2D atomristors. However, the μ value of 4×10^{-3} W in SET power (P_{SET}) consumption shows a slightly larger value than other 2D atomristors, which is still considered competitive given the large memory window. In contrast, the MoS_2 atomristor using symmetric Ag electrodes has a RESET power consumption (P_{RESET}) of about 5×10^{-5} W, which is 9 orders of magnitude higher than the h-BN atomristor using the same electrode because of its relatively smaller bandgap[46]. Furthermore, the V_{RESET} and I_{HRS} values are measured to be approximately −1.5 V and 10^{-7} A in the h-BN atomristor using symmetric Au electrodes, with the lowest P_{RESET} of 1.5×10^{-7} A among the same atomristor structures[48].

Discussion

In summary, this work has demonstrated giant memory window performance and low power consumption of symmetric h-BN atomristor structures using Ag metal electrodes via the wrinkle-free and residue-free PPC-assisted wet transfer method. Taking advantage of the superior material properties of the PPC support layer, we fabricated crossbar-shaped Ag/h-BN/Ag atomristor structures and measured their memory-switching behaviors through both RVS and PVS measurements. The h-BN atomristor exhibited the highest memory window of more than 10^9, the lowest leakage current of about 0.2 pA, and the lowest power consumption of around 10^{-14} W among other 2D atomristors. The h-BN atomristor also showed a much better memory endurance and retention performance of more than 10,000 cycles and 10^5 s (~28 h) as the interfacial distance between the h-BN and Ag surfaces became closer to the interfacial equilibrium distance due to the minimization of the polymer residues. Lastly, the yield of the fabricated h-BN atomristors was increased to 77% due to the high elastic modulus and low thermal expansion coefficient of the PPC support layer. This synergistic combination between highly insulating h-BN and electrochemically active Ag electrodes enables improved memristor characteristics at low power for future high-performance and energy-efficient neuromorphic computing components. Device-to-device variation remains a challenge and requires further systematic research studies.

Methods

Material characterization

The optical images of the h-BN atomristor and monolayer were captured by optical microscopy (BX51M-DP22 Metallurgical Microscope, Olympus).

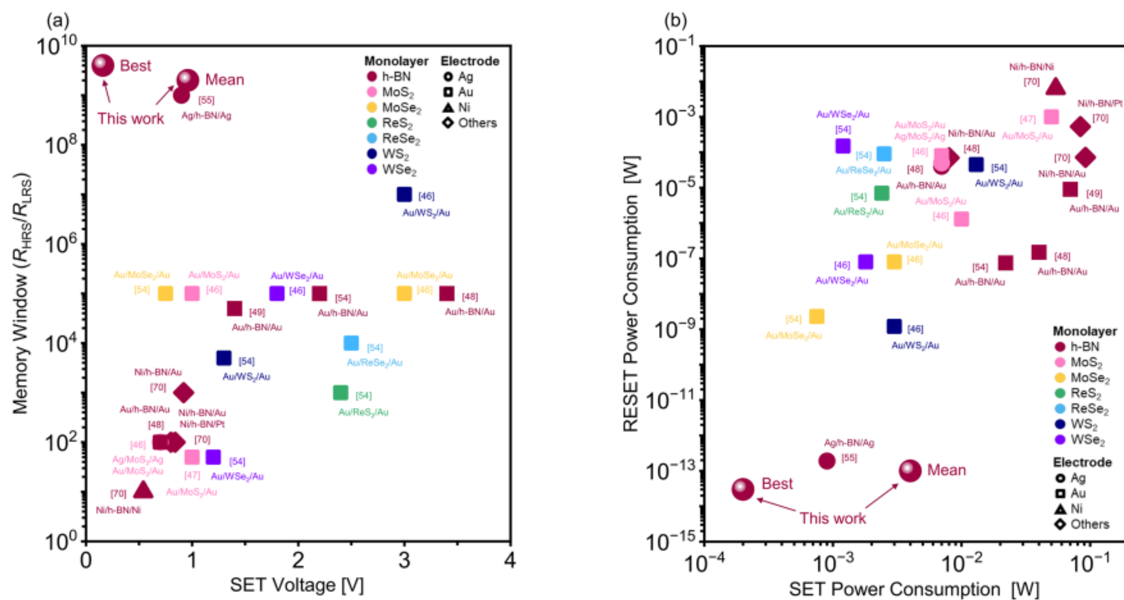

Fig. 5 | Figure of merit comparison of nonvolatile memory switching performances of two dimensional atomristors. **a** Memory window versus SET voltage characteristics from the atomristors using various active monolayers and electrodes. This work reports the highest memory window of 4×10^9 and a relatively small V_{SET} of 0.16 V, measured data with the best property from device-to-device variability results. **b** SET and RESET power consumption characteristics in the atomristors. This work shows the power consumption performances of 2×10^{-4} W for the SET process and 3×10^{-14} W for the RESET process.

Table 1 | Figure-of-merit comparison of nonvolatile resistive switching performances of two-dimensional monolayer atomristors

Active Layer	Electrode	Transfer Support Layer	V_{SET} [V]	V_{RESET} [V]	R_{HRS}/R_{LRS}	$_{SET}{}^{a}$ [W]	$_{RESET}{}^{b}$ [W]	Endurance [ ]	Reference
h-BN	Ag/Ag	PPC	0.16^{c} 0.96^{d}	0.14^{c} 0.25^{d}	$4 \times 10^{9\,c}$ $2 \times 10^{9\,d}$	$2 \times 10^{\ 4\,c}$ $4 \times 10^{\ 3\,d}$	$3 \times 10^{\ 14\,c}$ $10^{\ 13\,d}$	RVS 139 PVS 10^{4}	This work
h-BN	Ag/Ag	PMMA	0.9	0.19	10^{9}	$9 \times 10^{\ 4}$	$1.9 \times 10^{\ 13}$	RVS 46	55
h-BN	Au/Au	PMMA	3.4	1.3	10^{5}	$4 \times 10^{\ 2}$	$1.5 \times 10^{\ 7}$	RVS 50	48
h-BN	Au/Au	PMMA	1.4	0.9	5×10^{4}	$7 \times 10^{\ 2}$	$9 \times 10^{\ 6}$	–	49
h-BN	Au/Au	PMMA	2.2	0.75	10^{5}	$2.2 \times 10^{\ 2}$	$7.5 \times 10^{\ 8}$	–	54
h-BN	Au/Au	TF[e]	0.7	0.4	10^{2}	$7 \times 10^{\ 3}$	$4 \times 10^{\ 5}$	–	48
h-BN	Ni/Ni	TF[e]	0.54	0.63	10^{1}	$5.4 \times 10^{\ 2}$	$6.3 \times 10^{\ 3}$	–	70
h-BN	Ag/Cu	TF[e]	1.1	0.60	–	–	–	–	71
h-BN	Ni/Au	TF[e]	0.8	0.7	10^{2}	$8 \times 10^{\ 3}$	$7 \times 10^{\ 5}$	–	48
h-BN	Ni/Au	TF[e]	0.92	0.72	10^{3}	$9.2 \times 10^{\ 2}$	$7.2 \times 10^{\ 5}$	RVS 100	70
h-BN	Ni/Pt	TF[e]	0.84	0.53	10^{2}	$8.4 \times 10^{\ 2}$	$5.3 \times 10^{\ 4}$	–	70
MoS_2	Ag/Ag	TF[e]	0.7	0.5	10^{2}	$7 \times 10^{\ 3}$	$5 \times 10^{\ 5}$	–	46
MoS_2	Au/Au	PDMS	1.0	1.3	10^{5}	$10^{\ 2}$	$1.3 \times 10^{\ 6}$	RVS 146	46
MoS_2	Au/Au	PDMS	1.0	1.0	5×10^{1}	$5 \times 10^{\ 2}$	$10^{\ 3}$	RVS 124	47
MoS_2	Au/Au	TF[e]	0.7	0.8	10^{2}	$7 \times 10^{\ 3}$	$8 \times 10^{\ 5}$	–	46
$MoSe_2$	Au/Au	PDMS	0.75	0.75	10^{5}	$7.5 \times 10^{\ 4}$	$2.3 \times 10^{\ 9}$	–	54
$MoSe_2$	Au/Au	PDMS	3.0	0.8	10^{5}	$3 \times 10^{\ 3}$	$8 \times 10^{\ 8}$	–	46
ReS_2	Au/Au	PDMS	2.4	1.4	10^{3}	$2.4 \times 10^{\ 3}$	$7 \times 10^{\ 6}$	–	54
$ReSe_2$	Au/Au	PDMS	2.5	0.9	10^{4}	$2.5 \times 10^{\ 3}$	$9 \times 10^{\ 5}$	RVS 240	54,72
WS_2	Au/Au	PDMS	1.3	1.5	5×10^{3}	$1.3 \times 10^{\ 2}$	$4.5 \times 10^{\ 5}$	–	54
WS_2	Au/Au	PDMS	3.0	1.2	10^{7}	$3 \times 10^{\ 3}$	$1.2 \times 10^{\ 9}$	–	46
WSe_2	Au/Au	PDMS	1.2	1.5	5×10^{1}	$1.2 \times 10^{\ 3}$	$1.5 \times 10^{\ 4}$	–	54
WSe_2	Au/Au	PDMS	1.8	0.8	10^{5}	$1.8 \times 10^{\ 3}$	$8 \times 10^{\ 8}$	–	46

[a] $P_{SET} = V_{SET} \times I_{SET}$.
[b] $P_{RESET} = V_{RESET} \times I_{RESET}$.
[c, d] The V_{SET}, V_{RESET}, and R_{HRS}/R_{LRS} values are used from the best and mean values measured from device-to-device variability results.
[e] TF stands for transfer-free.

The thicknesses of the h-BN atomristor and monolayer were measured by atomic force microscopy (Dimension Icon, Bruker). The area coverage by percentages was obtained by post-processing the optical images using the ImageJ software. Thresholding was applied to identify and mask the regions containing polymeric residue selectively, and the areas of these regions were determined using the software. The Raman peaks of the h-BN monolayer were measured by Raman spectroscopy (inViaTM Confocal Raman Microscope, Renishaw PLC).

Device fabrication

The diamond substrate was rinsed with acetone, methanol, and isopropyl alcohol and dried by a nitrogen spray gun. The 50 nm-thick bottom Ag metal electrode was lithographed by an electron beam (e-beam) lithography system (JBX-8100FS/E, JEOL USA) and deposited on the diamond substrate by an e-beam evaporation system (PRO Line PVD 200, Kurt J. Lesker Company). The h-BN active monolayer was prepared on the 285 nm-thick SiO_2/Si substrate and transferred to the diamond substrate through two different PPC-assisted and PMMA-assisted wet transfer methods. The 90 nm-thick top Ag metal electrode was lithographed and deposited on the wet-transferred h-BN active monolayer by the same e-beam lithography and evaporation systems.

Polymer support layer preparation

The PPC pellets (389021-100G, Sigma-Aldrich) were dissolved into the anisole solution (123226-100 ML, Sigma-Aldrich) with a ratio of 15   PPC by weight. The hot plate and magnetic stirrer were used to promote the dissolution of the pellets in the anisole solution over the course of three days.

Material transfer

The CVD grown h-BN monolayer (Grolltex, Inc.) was prepared on the 285 nm-thick SiO_2/Si substrate. The h-BN monolayer on the SiO_2/Si substrate was rinsed with acetone/methanol/isopropyl-alcohol and dried with a nitrogen spray gun. The PPC support layer was spin-coated on the h-BN grown layer at 4000 rpm for 45 sand baked on the hot plate at 180 °C for 120 s. The PPC/h-BN stacking layer on the SiO_2/Si substrate was soaked with the BOE 6:1 until the SiO_2 substrate was wet etched with the BOE 6:1. The PPC/h-BN stacking layer was separated from the silicon (Si) substrate and   shed to the DI water. The PPC/h-BN stacking layer was rinsed and annealed in DI water on the hot plate at 40 °C. The PPC/h-BN stacking layer was transferred to the diamond substrate and annealed on the hot plate at 100 °C for 120 s to remove the water droplets of DI water. The PPC support layer was dissolved with acetone from the h-BN transferred layer on the diamond substrate.

Device measurement

The RVS measurements were carried out by using a semiconductor device parameter analyzer (B1500A, Keysight Technologies) on a cascade probe station (Summit 11000 AP, FormFactor). The V_{SET} bias was swept from 0.0 V to 2.0 V to 10 V at 1 mA current compliance, while the V_{RESET} was swept from 0.0 V to   0.2 V to   0.8 V without any current compliance. The V_{READ} bias was swept from 0.0 V to 0.2 V in the same direction as the V_{SET} bias. The PVS endurance measurements were conducted using a semiconductor parameter analyzer (B1500A, Keysight Technologies) on a semiconductor probe station (Summit 11000 AP, FormFactor, Inc.). The

block diagram in LabVIEW VI was designed to apply repetitive V_{SET}-V_{READ}-V_{RESET}-V_{READ} pulse sequences. LabVIEW from National Instruments was used for the measurement to repetitively apply voltage pulses. The amplitude and width of the V_{SET} pulses were set to 1.0 V and 30 ms, respectively, with a current compliance setting of 100 uA, while the amplitude and width of the V_{RESET} pulses were set to 0.4 V and 30 ms, respectively, with a current compliance setting of 100 mA. Similarly, the amplitude and width of the V_{READ} pulses were set to 0.3 V and 30 ms, respectively, with a current compliance setting of 100 A.

Data availability

No datasets were generated or analysed during the current study.

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Author contributions

S.J.Y. and Y.-R.J. contributed equally to this work. S.J.Y. carried out the characterizations, fabrications, and measurements. Y.-R.J. conducted the high-speed pulse measurements. D.K. created the automated test system for stable endurance measurements. S.M. analyzed the area coverages of transferred monolayer and organic residues after wet transfers. M.D. and S.K.B. prepared the polymer support layers for wet transfers. S.J.Y., Y.-R.J., and D.A. analyzed all the electrical data and wrote the manuscript. D.A. initiated and supervised the research and experiment of the collaborative project.

Competing interests

The authors declare no competing interests.

Additional information

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