

Ka-Band MMIC Implementation of a Load-Modulating Loop Combiner Power Amplifier

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Abstract—This letter presents a MMIC implementation of the Load-Modulating Loop Combiner (LMLC) power amplifier (PA) architecture for Ka-band operation. This architecture incorporates elements of a feed-forward amplifier topology and the Doherty power amplifier to provide load modulation operation and improved linearity performance. A GaN MMIC operating at 28 GHz was designed and measured. The device presented in this work operates with a peak output power of 33.4 dBm and 33.7% peak PAE. Modulated measurements with a 100 MHz LTE signal are also presented.

Index Terms—linearity improvement, power amplifiers, MMIC, feed-forward, efficiency enhancement, mobile communications, GaN

I. INTRODUCTION

The growth in high data-rate communications at millimeter-wave (mm-wave) frequencies has led to a need to scale efficiency-enhancing PA architectures to MMIC implementation. Ka-band systems typically use arrays for spatial power combining and electronic beam steering. As a result of this architecture shift compared to sub-6 GHz basestations, the ability to apply standard digital pre-distortion (DPD) techniques at the element level becomes prohibitively complex. Therefore, the dip in gain observed in many DPAs due to the turn-on characteristics of the auxiliary PA may be difficult to compensate for in the mm-wave front-end.

The load-modulating loop combiner (LMLC) architecture was recently proposed as an approach to improve the linearity of a Doherty PA (DPA) without compromising the efficiency performance [1]. This technique combines the operating principles of the DPA with the loop cancellation strategy of the feedforward amplifier (FFA). In contrast with the FFA architecture [2], which usually exhibits very low efficiency even at low frequencies, in the LMLC the auxiliary PA operates on the fundamental tones and therefore contributes to the in-band output power of the PA. Similar to linear DPA variants [3], [4], the LMLC does not display a strong second efficiency peak at output power back-off, but does exhibit improved efficiency at peak output power level.

This work evaluates the LMLC as a mm-wave PA architecture through a MMIC implementation operating at 28 GHz. The details of scaling this architecture, previously only demonstrated as a 3.5-GHz hybrid PA, to a MMIC are discussed.

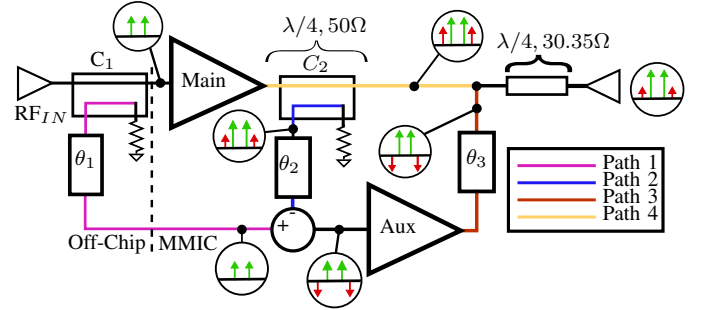


Fig. 1. Illustration of carrier and intermodulation term behavior throughout the LMLC architecture.

The fabricated MMIC is characterized under both CW and modulated measurements.

II. LMLC MMIC DESIGN PROCESS

The underlying theory and working principle behind the LMLC architecture is presented in [1] and will not be discussed in detail in this letter. Here, the focus is on adapting the architecture for implementation in WIN Semiconductors' NP12 GaN process at a 28-GHz operating frequency. As can be seen in Fig. 1, the architecture appears similar to a DPA but includes an additional path from the output of the main amplifier to the input of the auxiliary amplifier. This signal path allows for manipulation of the distortion terms generated at the main amplifier's output, and also dynamically adjusts the input to the auxiliary PA as the main PA starts to saturate. One effect of this LMLC approach is that the degradation in gain around the auxiliary PA turn-on is mitigated. To accomplish this effect, the critical design components are couplers C_1 , C_2 , the subtractor element and delay lines, θ_1 , θ_2 and θ_3 . The delay lines grant degrees of freedom to ensure the correct phase alignment of the carrier and distortion terms as illustrated in Fig. 1.

The first design step is the implementation of the main and auxiliary amplifiers which are both designed using 4x75μm periphery devices. The main amplifier is biased into Class-AB mode and the auxiliary amplifier is biased into Class-C mode, as is typical for Doherty power amplifiers. The 4x75μm device at 28 GHz requires impedances close to the edge of the

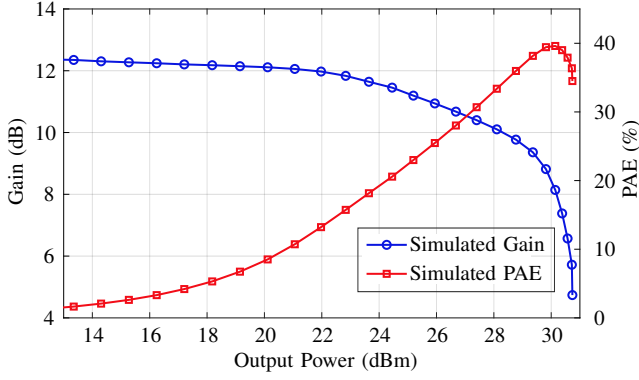


Fig. 2. Driveup simulation of PAE and gain of main amplifier only.

Smith Chart with values such as ($|\Gamma| \geq 0.92$) to be presented to the device. Similar to DPA design, the AB-mode amplifier in the LMLC is designed to operate with an output impedance termination of 100Ω . The high matching ratio leads to a trade-off in matching network size, insertion loss and match quality. Loss in the matching network, while generally undesirable, also serves to improve stability. At 28 GHz, one strategy to consider is to utilize a larger matching network with higher insertion loss to alleviate stability requirements. Stability was confirmed in this design via both k-factor analysis and the Nyquist stability criterion.

The simulated drive-up performance of the Class-AB main amplifier into its nominal 100Ω load is shown in Fig. 2. It can be seen that the device in class-AB mode provides 12 dB of gain at back-off output power levels and a maximum PAE of 39% at 30 dBm output power. The device delivers a maximum of 30.73 dBm of output power at saturation. PAE at 6 dB output back-off (OBO) is approximately 20%; note that the 6 dB OBO point is defined as the output power value that is 6 dB below the point of peak PAE.

The subtractor element of the design is implemented using a 90° branchline coupler (BLC). Other coupler topologies were considered, such as a rat-race combiner and a March combiner. Ultimately, the BLC topology was selected due to limitations in available die area. In contrast to the rat-Race and March topologies which offer "sum" and "delta" ports, allowing for a subtractor element to be easily implemented, the BLC provides a quadrature relation between its outputs. Knowing that if signals of equal amplitude and phase are applied to the input ports, (ports 1 and 4), then the output components at port 3 will be:

$$S_{31} = 0.707 \angle -180^\circ \quad (1)$$

$$S_{34} = 0.707 \angle -90^\circ \quad (2)$$

By adding a 90° delay line at port 1 of the BLC, the applied terms can be made to interact destructively at port 3. This satisfies our desired behaviour of implementing a subtractor circuit at the input of the auxiliary amplifier. Delay lines θ_1, θ_2 were tuned to ensure that signal paths 1 and 2 [Fig. 1] present the required electrical length for the desired behaviour.

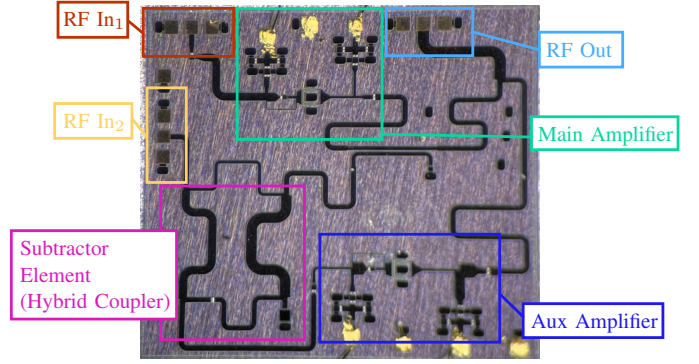


Fig. 3. Labeled image of MMIC die with key components outlined.

A key design consideration with the LMLC architecture is the selection in coupling values for C_1 and C_2 . By adjusting these values, and specifically the relative difference between the coupling coefficients, the magnitude of the carrier signal fed into the auxiliary amplifier can be increased. This, of course, impacts the output power delivered by the auxiliary amplifier which affects the PAE and gain characteristics of the larger system. Conversely, minimizing the magnitude of the input carrier term to the auxiliary amplifier results in only the intermodulation terms being amplified which yields improved linearity performance. Consequently, it can be seen that these design degrees of freedom allow for a trade-off between gain, PAE and linearity.

Based on the analysis in [1], the coupling value C_2 should nominally be made equivalent to the gain of the auxiliary amplifier for the LMLC to produce simultaneous linearity and efficiency improvements. Because the amplifier gains vary as a function of input power, a specific point in the amplifier driveup must be pre-selected for the C_2 coupling factor design. The coupling coefficient C_1 is calculated with the assumption that the gain values of both the main and auxiliary amplifiers are equal, which is similarly dependent on the drive powers of the two PAs as well as their bias conditions. Consequentially, in the design process we select a point in the driveup of both amplifiers wherein non-linear terms become increasingly dominant and the desired coupling values are physically manufacturable.

With these assumptions in place, for this design a value of 6 dB is selected for C_1 and a coupling coefficient of 9 dB is selected for C_2 . Note that the lower coupling coefficient required in this design for C_1 (in contrast to the 3 dB value used in the input power divider of a DPA) assists in improving gain at backoff levels when the auxiliary device is in an off state. This value is obtained via tuning the design to achieve a balance of gain / PAE performance, linearity and manufacturability. It should also be noted that C_2 also serves as a section of the $\lambda/4, 50\Omega$ transmission line that is required at the output of the main amplifier (Path 4 in Fig. 1) to provide the appropriate impedance transformation behavior. In actuality, coupler C_2 is not set to present an electrical length of 90° due to layout constraints and the need for additional line

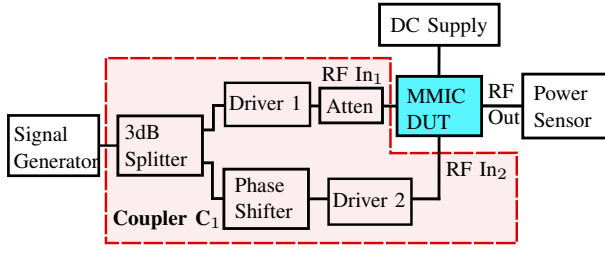


Fig. 4. Block diagram of the test bench setup used for measurement.

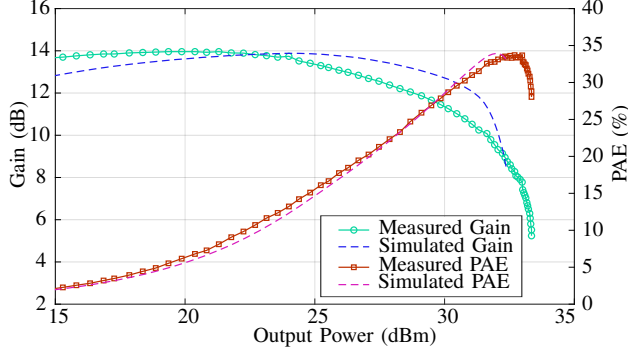


Fig. 5. Simulated and measured CW gain and PAE performance of the LMLC MMIC.

length to connect the subtractor circuit and the main amplifier. Coupler C_1 and delay line θ_1 are implemented off-chip due to limited available die area and to allow for an additional degree of freedom when characterizing the device. Path 3 (θ_3) was tuned to ensure that the output terms generated by the auxiliary amplifier combined correctly at the output combining node.

III. TESTBENCH SETUP AND MEASURED RESULTS

Fig. 4 illustrates the experimental test bench used to characterize the proof-of-concept MMIC. Because a Ka-band coupler with the desired coupling ratio was not available for use in this setup, the structure shown in Fig. 4 was used instead. The variable attenuator after driver 1 ensures a constant 6-dB difference between the outputs of the driver stages. A coupler-based power tracking setup was used to enforce this power ratio, even over the different gains and drive-up characteristics of the two drivers. An analog phase shifter in the auxiliary amplifier path emulates the delay line θ_1 .

TABLE I
COMPARISON TO OTHER GaN MMIC PAS AT KA-BAND.

Ref.	Tech.	Arch.	Stages	Freq. (GHz)	Psat (dBm)	PAE (%)	PAE@ 6-dB OBO
[5]	150nm	DPA	2	26–29	36.5	27%	27%
[6]	150nm	class A/AB	3	30	37.6	39.8%	NR
[7]	100nm	DPA	3	30	36	33%	10%*
[8]	150nm	DPA	2	27.5–29.5	35.6	26%*	22.7%
This work	120nm	LMLC	1	28	32.4	33.7%	19.5%

* – read from graph; NR = not reported

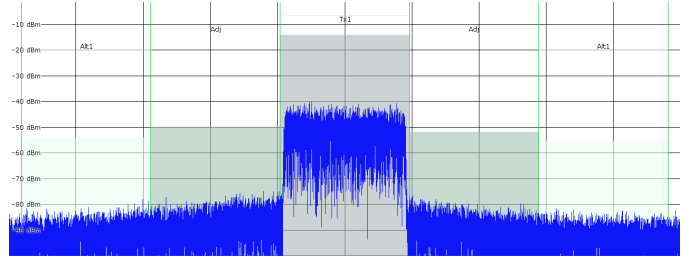


Fig. 6. Spectrum view of applied, 100 MHz LTE-like signal.

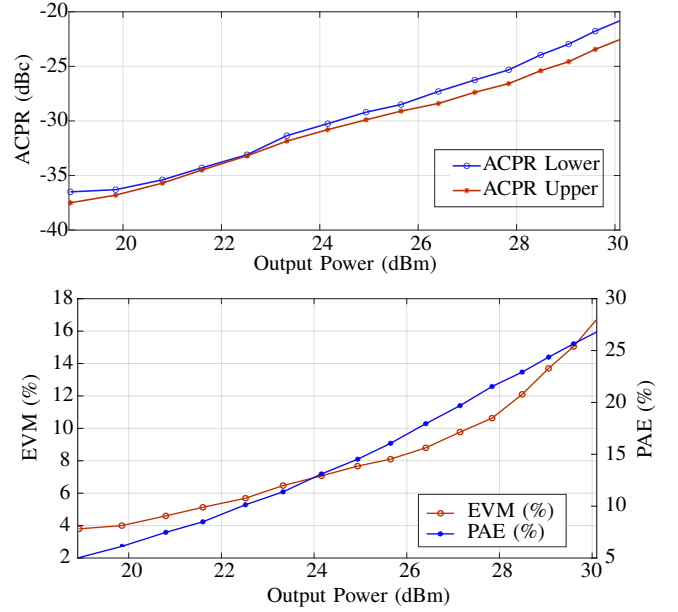


Fig. 7. Upper/Lower ACPR measurements and EVM performance.

Fig. 5 shows the simulated and measured continuous wave (CW) performance of the LMLC MMIC amplifier. It can be seen that similar absolute values of peak gain and PAE were observed (approximately 14 dB and 33.7% respectively). Measured gain at back-off was slightly higher than that of simulation but lower at higher power levels suggesting slightly different turn on behavior for the auxiliary amplifier than expected. PAE at 6 dB OBO is approximately 19.5%, using the same definition as the aforementioned standalone, main amplifier. The MMIC was also measured to have a higher saturated output power than simulated with approximately 33.4 dBm output power measured and 32.4 dBm output power simulated.

The CW performance is compared to other GaN MMICs operating in a similar frequency range in Table I. Even though this proof-of-concept LMLC MMIC does not explicitly show a second efficiency peak at output back-off, its PAE at 6-dB OBO falls in between the expected Class-AB back-off performance and the high OBO PAE reported in, for example, [5]. Not conveyed in the table is the CW gain flatness, with the LMLC exhibits a more gradual gain compression characteristic compared to that in [5] and similar DPA MMICs.

An example output spectrum under modulated excitation is shown in Fig. 6, which corresponds to a 100 MHz LTE-like, 10 dB peak to average power ratio (PAPR) signal. Both error vector magnitude (EVM) and adjacent power channel ratio (ACPR) measurements were conducted with 100 MHz spacing between the modulated band and adjacent bands. No form of digital pre-distortion (DPD) was applied to the DUT. Fig. 7 shows the ACPR performance of the DUT against output power. Upper and lower ACPR below -30 dBc was maintained up to 24 dBm output power. The device operates with under 7% EVM up to approximately 24 dBm output power.

IV. CONCLUSION

The GaN MMIC presented in this work implements the LMLC architecture for Ka-band applications. The ability to eliminate the characteristic gain dip of conventional DPAs at the expense of a strong second efficiency peak is verified. While a strong efficiency enhancement behavior is not seen, the LMLC MMIC performance is on par with other designs in the same frequency range. The design space can be further explored to trade the gain flatness for back-off efficiency performance.

V. ACKNOWLEDGMENTS

This material is based on work supported by the National Science Foundation under Grant No. 1846507. The authors thank WIN Semiconductors for access to their GaN NP12 process and their donation of reticle space to the University of Colorado Boulder.

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