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Silicon-On-Silicon Carbide Platform for Integrated Photonics

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Silicon carbide (SiC)'s nonlinear optical properties and applications to quantum information have recently brought attention to its potential as an integrated photonics platform. However, despite its many excellent material properties, such as large thermal conductivity, wide transparency window, and strong optical nonlinearities, it is generally a difficult material for microfabrication. Here, it is shown that directly bonded silicon-on-silicon carbide can be a high-performing hybrid photonics platform that does not require the need to form SiC membranes or directly pattern in SiC. The optimized bonding method yields defect-free, uniform films with minimal oxide at the silicon–silicon–carbide interface. Ring resonators are patterned into the silicon layer with standard, complimentary metal–oxide–semiconductor (CMOS) compatible (Si) fabrication and measure room-temperature, near-infrared quality factors exceeding 10^5. The corresponding propagation loss is 5.7 dB cm^{-1}. The process offers a wafer-scalable pathway to the integration of SiC photonics into CMOS devices.

1. Introduction

Having proven to be a high-performing material in power and high-frequency electronics, silicon carbide (SiC) also has a significant potential in the field of integrated photonics. It has demonstrated remarkable optical performance across a variety of applications, including spin-based quantum computation,[1–4] high-power electro-optic modulators,[5] and nonlinear photonics.[6–9] The latter of these applications have capitalized on SiC's large infrared second-order coefficient ($\chi^2 \approx 38$ pm V^{-1}),[10] third-order Kerr refractive index ($n_2 \approx 6 \times 10^{-19}$ m^2 W^{-1}),[8,11,12] and Pockel coefficient ($r \approx 1$ pm V^{-1})[5] which is comparable to aluminum nitride.[13] Such demonstrations highlight SiC's potential as a material platform for the future of photonic integrated circuits (PICs), notably for quantum and nonlinear devices.

Critical to the advancement of integrated SiC photonics is the development of scalable fabrication methods. Heteroepitaxial growth of the 3C-SiC polytype on silicon (Si) is a cost-effective, large-scale approach. However, the large lattice and thermal expansion mismatch between Si and 3C-SiC create crystal defects, which have been shown to deteriorate device performance.[14,15] Bulk, monolithic patterning in SiC remains a significant challenge at wafer scale and is particularly deleterious for spin coherence, although recent fabrication results show the processing can be spin-preserving.[16] SiC-on-insulator (SiCOI)[6,7] has emerged as an alternative and very promising approach, mirroring the early development of photonic silicon-on-insulator (SOI) platforms, albeit via chemical-mechanical polishing (CMP) to remove the SiC donor wafer as opposed to SmartCut. However, the total thickness variation across the SiC thin film is prohibitively large for wafer-scale production and consistent device performance across these

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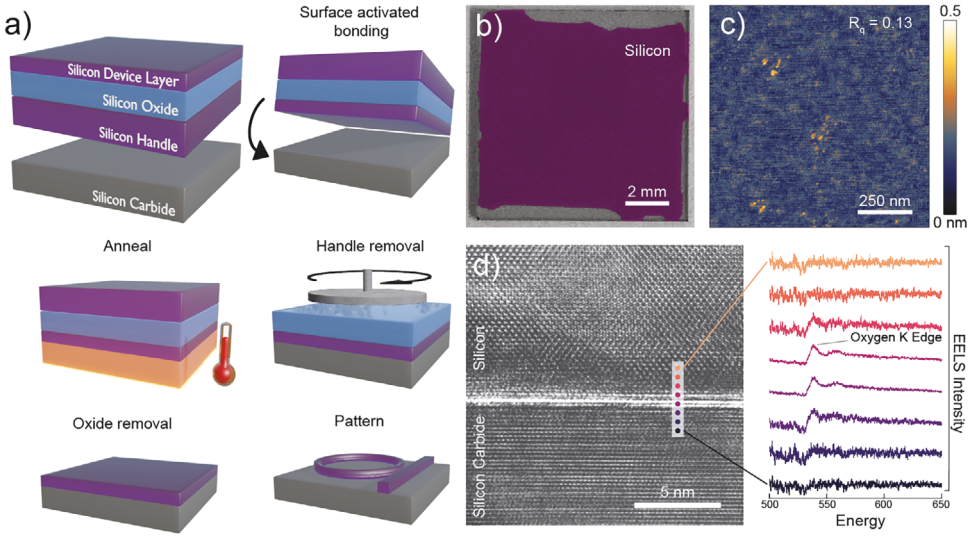

Figure 1. Wafer bonding and material quality. a) Schematic of the wafer bonding fabrication. b) Optical micrograph of a SiSiC film with the 220-nm-thick Si device layer shown in purple. c) Atomic force microscope height profile over a 1 × 1μ m^2 area. The RMS surface roughness is 0.13 nm. d) HRTEM of the Si–SiC interface showing high-quality crystal Si and SiC. EELS spectra (right side) correspond in color to the measured spatial position across the interface. The appearance of the oxygen K-edge signature near 530 nm suggests a 2-nm-thick silicon oxide amorphous region at the interface.

dimensions has not been demonstrated. Furthermore, CMP creates subsurface damage[17] which requires additional processing steps and complexities to remove. As such, high-yield, wafer-scale SiC fabrication remains a substantive challenge.

In this work, we demonstrate a heterogeneous single crystal silicon-on-SiC (SiSiC) photonic platform which utilizes CMOS-compatible wafer bonding and standard pattern transfer into the Si layer. Our optimized processes yields Si films with a 2 nm thickness variation, 0.13 nm root-mean squared (RMS) surface roughness, and a 2-nm-thick amorphous oxide at the bonded interface. We simulate and experimentally demonstrate SiSiC ring resonators with quality factors as high as 116 000 at wavelengths near 1550 nm, corresponding to a 5.7 dB cm^{-1} propagation loss. Our approach is scalable and may facilitate cost effective heterogeneous SiSiC photonic integrated circuits which incorporate the maturity of Si photonics with the outstanding properties of SiC.

2. Results

2.1. Wafer Bonding and Fabrication

We use a hydrophilic direct bond method to fabricate the SiSiC films. A summary of our process is shown in **Figure 1a**. We begin with a commercial SOI wafer (220-nm-thick Si device layer, Soitec) and a high purity semi insulating (HPSI) 4H-SiC wafer with a 0°-miscut (Cree). They are each then diced into 10 × 10mm^2 dies. Both Si and SiC dies are treated with a modified RCA clean to activate the surfaces via the creation of hydroxyl groups (-OH) at the Si interfaces. We use drop-shape analysis to measure a contact angle change from 41° to 7° following RCA treatment, indicating a hydrophilic surface termination. Immediately after RCA, we bring the two dies into contact to form a van der Waals bond. To promote the formation of covalent bonds,[18] we anneal the stack in a two-step process: the sample is placed in a bonding jig (BJ2, Logitech) to apply a pressure of ≈4 N cm^{-2} while the entire setup is annealed in atmosphere at 250° C for 3 h; the stack is then removed from the bonding jig and annealed at 900° C in a nitrogen atmosphere for 2 h.

To remove the Si handle from the SOI, we first grind the handle wafer down to 250 μm with multiple passes of a 500 μm resin blade. Subsequently, we etch the remaining handle away using 30% potassium hydroxide (KOH) solution heated to 70° C. The wet etch rate is 50 μm hr^{-1}. Finally, we remove the buried oxide layer with diluted HF.

Our process yields millimeter-scale, sub-nanometer smoothness SiSiC carbide films. The Si film coverage yield typically exceeds 90% (Figure 1b), limited by KOH lateral etching at the exposed Si die edges. We use profilometry and atomic force microscopy (AFM) to measure the Si film thickness of 220 ± 1 nm across the die. Local, 1 × 1 μm^2, AFM scans yield an RMS Si surface roughness of R_q = 0.13 nm (Figure 1c). In the future, sidewall etch barriers could improve the Si coverage up to 100%. Scaling our process to ≥100-mm wafer dimensions may require optimizing a low-temperature bonding technique similar to Gammon et al.[19] to mitigate wafer bowing from the thermal expansion mismatch and defect formation from gas byproducts.[20] This approach and additional process optimization could readily offer a path toward wafer-scale production.

In addition to surface topography, a critical measure of bond quality is the interfacial morphology between the Si and SiC layers. Furthermore, surface defects from contaminates and dangling bonds contribute to optical loss and should be mitigated. We examine the Si–SiC interface using high resolution transmission electron microscopy (HRTEM) and electron energy loss spectroscopy (EELS) (Figure 1d). The cross sectional TEM sample was prepared using a Zeiss NVision 40 focused ion beam (FIB) with a standard lift-off process, and HRTEM and EELS measurements were obtained from a Thermo Fisher Spectra 200 (S)TEM, equipped with a Gatan EELS system and operated at 200 kV. HRTEM images reveal uniform single crystal structure

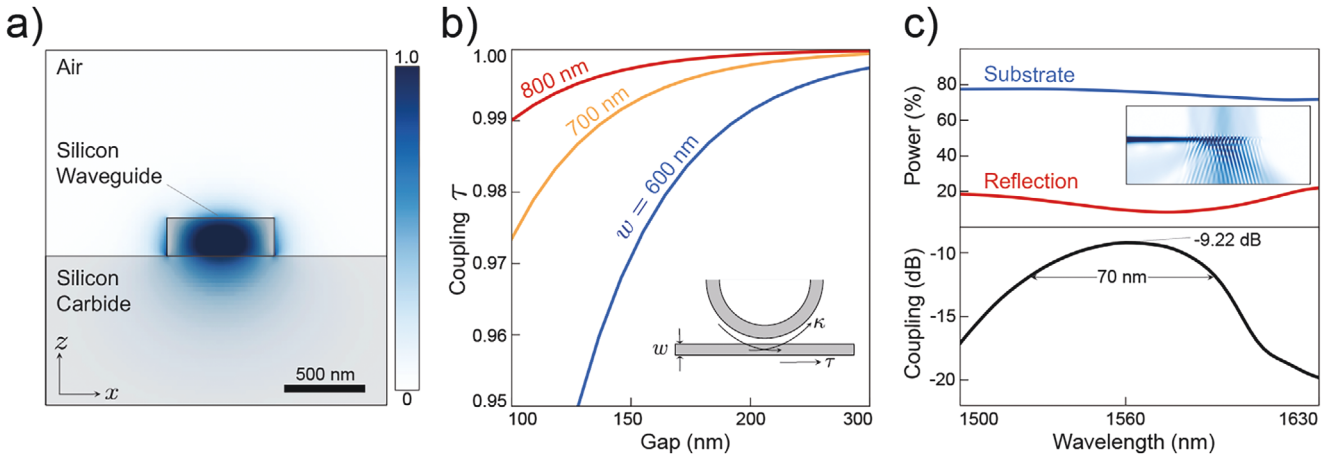

Figure 2. Resonator design. a) Quasi-TE single mode field profile of a waveguide with dimensions w = 600 nm and height = 220 nm. b) Numerically-calculated self coupling coefficient (τ) as a function of ring-waveguide gap for waveguide widths 600, 700, and 800 nm. c) Substrate and back-reflected power for our optimized apodized focusing grating (top). Inset shows the electric field profile. Calculated grating-to-fiber coupling efficiency (bottom) with peak value of –9.22 dB (≈ 12%) at 1550 nm and a 70 nm bandwidth.

throughout the 220-nm-thick Si film and SiC substrate. We observe an amorphous region at the interface, which we quantify using EELS taken at 0.39-nm-steps across the interface. As shown in the Figure 1d inset the oxygen K-edge spectral signature—present near 530 eV—persists across a 2 nm interval, indicating the formation of an amorphous silicon oxide layer. These findings are consistent with the hydroxyl termination we anticipate from our modified RCA activation process. Depending on the final application, the interfacial oxide can be reduced/eliminated using high-temperature anneals (>1150 °C).[21] We then realize photonic devices using well-established CMOS-compatible Si fabrication. Following electron beam lithography exposure (Raith EBPG+) into ≈100-nm-thick 6% hydrogen silsesquioxane (HSQ) resist, patterns are transferred into the Si layer using a chlorine-based inductively coupled plasma (ICP) reactive ion etch (RIE). To minimize SiC substrate exposure to the plasma etchants, we carefully monitor the unmasked Si device layer thickness by frequently measuring the remaining thickness of a 220-nm-thick SOI chip taken from the same wafer used to fabricate the SiSiC heterostructures. We do not observe an increase in the SiC surface roughness following ICP etching. Finally, the developed HSQ mask is removed with a 30 s buffered oxide etch.

2.2. Resonator Design

We design the Si waveguide to support a single quasi-transverse electric (TE) mode at near-infrared wavelengths (**Figure 2**a). Using a finite difference time domain solver (FDTD, (Tidy3D[22]) we find a TE mode at $\lambda = 1500$ nm with an effective mode index $n_{eff} = 2.61$. For waveguides with a width and height of 600 and 220 nm, respectively, the mode overlap within SiC is $\Gamma_{SiC} = 22\%$; however, mode overlap is geometry dependent, increasing to 50% for heights less than 170 nm. Engineering the field overlap factor is critical for applications such as hybrid material nonlinear devices and coupling to near-surface quantum defects.

The design parameters of our ring resonators were chosen to 1) minimize bending loss and 2) operate at or below critical coupling. We perform mode simulations and find a bending loss of 0.1 dB cm^{-1} for a ring radius of $R = 50$μ m. The coupling constants as a function of gap size is estimated using a semi-analytic method[23] for waveguide widths 600, 700, and 800 nm (Figure 2b). To operate at or below critical coupling, we estimate gap sizes in the range of 100–200 nm.

To couple infrared light into the ring resonators, we optimize an apodized focusing grating coupler design. Apodized gratings have a linear variation in fill fraction and period, allowing for an improved impedance match between the waveguide and the grating; optimized SOI designs have demonstrated coupling efficiencies near –1 dB (79%).[24] Using 2D FDTD simulations (Tidy3D[22]), we compute the coupling efficiency into a 10.3 μm mode field diameter fiber for different linear apodization factors and coupling fiber positions. The optimal parameters from the 2D simulations are then used to compute the full 3D fields of a device. The top plot in Figure 2c shows the calculated power into the substrate (blue) and back-reflected into the waveguide (red); the inset is a cross-sectional electric field intensity profile of the grating. The large substrate power transmission is attributed to SiC's large refractive index. The bottom plot in Figure 2c shows the coupling efficiency into a tilted (8°) fiber. The optimal coupling efficiency is calculated to be –9.22 dB (≈ 12%) at 1550 nm with a bandwidth of 70 nm. Coupling efficiencies can be improved with addition of a cladding material, such as silicon dioxide, or a partial grating etch depth. **Figure 3** shows an optical image of a complete ring resonator device (Figure 3a), along with false-color scanning electron micrographs of the waveguide-ring gap (Figure 3b) and waveguide cross section (Figure 3c).

2.3. Ring Resonator Characterization

Optical device characterization is performed at room temperature using the setup shown in **Figure** 4a. A 127 μm pitch, 8°-angled fiber array is used to couple and collect light from each device, positioned using an automated fiber alignment station (MapleLeaf Photonics). A continuous wave tunable laser (Santec)

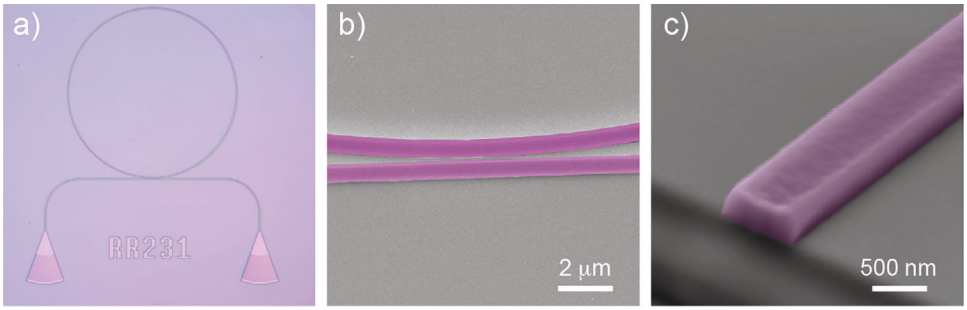

Figure 3. Device images. a) Optical microscope image of a full ring resonator device. b) SEM of the ring-waveguide gap (125 nm). c) Cross-section SEM following FIB milling showing minimal sidewall roughness and proper waveguide dimensions (220 nm × 600 nm). For clarity, we use purple as a false color for Si in (b) and (c).

is used as the infrared light source and is scanned over the range 1500–1630 nm in steps of 0.2 pm at an output power of –8 dBm. Polarization maintaining fibers are used and a three-paddle polarization controller is configured for TE input polarization. Transmitted intensity is detected using an infrared photodiode.

Figure 4b shows a transmission spectrum of our best performing device with an 800 nm waveguide width and a 125 nm ring-waveguide gap. The device is undercoupled, and resonances are separated by a free spectral range of 2 nm, corresponding to a group index of 3.75. The sinusoidal background signal

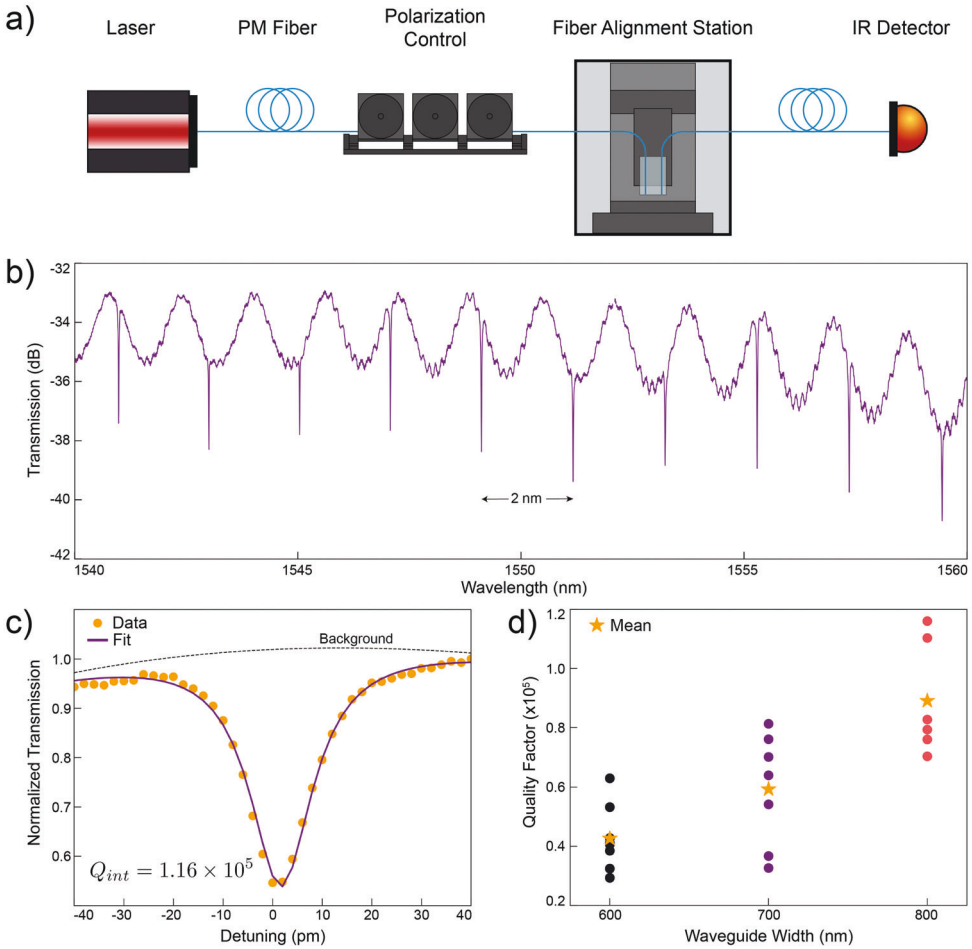

Figure 4. Sample characterization. a) Experimental setup used to characterize our devices. b) Transmission specrtum of an exemplary device with a FSR of 2 nm. The periodic background signal originates from multiple backreflections from the grating couplers. c) Transmission spectrum of our best-performing device with an internal quality factor of $Q_{int} = 1.16 \times 10^5$, extracted by fitting the measured data to Equation 1 after removing the background. d) Stacked histrogram of the extracted internal quality factors for devices of different waveguide widths. The average quality increases with increasing widths, indicating sidewall scattering as the dominant loss mechanism.

originates from a Fabry–Perot cavity formed between the two grating couplers. We estimate quality factors by fitting transmission data to the analytic formula for the transmission of an all-pass resonator,[25]

$$T = \frac{a^2 - 2\tau a cos(\beta L) + \tau^2}{1 - 2\tau a cos(\beta L) + \tau^2 a^2} \quad (1)$$

The variables in Equation 1 are as follows: a is the single-pass amplitude transmission; τ is the self-coupling coefficient; β is the propagation constant; and L is the ring's circumference. After extracting coefficients a and τ, we can calculate the external and internal Q from,

$$Q_{int} = \frac{2Q_{ext}}{(1 + \sqrt{T_0})} = \frac{2\pi n_g L\sqrt{\tau a}}{\lambda_0(1 - \tau a)(1 + \sqrt{T_0})} \quad (2)$$

where λ_0 is the resonance wavelength and T_0 is the transmission at resonance.[26,27] As shown in Figure 4c, we find an internal Q of $Q_{int} = 1.16(0.05) \times 10^5$ at $\lambda = 1447.1$ nm, corresponding to a propagation loss of $\alpha = 5.71$ dB/cm. The Q-factor is comparable to that measured in typical heterogeneously integrated Si ring resonators[28] and an order-of-magnitude greater than reported in Wang et al.[29]

Material propagation loss in Si and SiC have been demonstrated to exceed 2.7 dB m^{-1}[30] and 7.4 dB m^{-1},[8] respectively. Under the assumption of negligible bending loss, we attribute the limiting loss mechanism to sidewall scattering. This conclusion derives from collecting quality factor statistics on several devices of varying waveguide widths. Figure 4d shows the distribution of quality factors for our measured devices for varying waveguide widths. Average internal quality factors (stars in Figure 4d) for devices with waveguide widths of 600, 700, and 800 nm are, respectively, 4.26×10^4, 5.29×10^4, and 8.92×10^4 for operating wavelengths near 1550 nm. This trend is consistent with a sidewall scattering loss mechanism because mode confinement increases in wider waveguides, reducing field overlap with the sidewalls. Ring resonators with waveguide widths larger than 900 nm were fabricated but did not have sufficient coupling to resolve transmission resonances. In the future, "pulley" ring-waveguide coupling geometries would allow for wider waveguides with reduced sidewall scattering without the necessity of sub-100-nm gaps that are both a fabrication challenge and a potential source of loss.[31] Furthermore, post-patterning anneals and treatments in Si have been demonstrated to reduce surface roughness, a potential route toward ultra-high quality factor devices.

In addition to sidewall scattering, optical loss may originate from interfacial defects such as interstitial defects and dangling bonds.[31] The 2-nm-thick amorphous silicon oxide region at the Si–SiC interface is a potential source of these defects. In order to reduce this layer in future devices, a key step would be to understand it better by correlating optical loss measurements with chemical composition techniques like energy-dispersive, X-ray photo-electron, and Raman spectroscopy. Additionally, high-temperature anneals might greatly reduce or completely eliminate the amorphous region. Understanding the interface effects will likely be a critical factor for advancing our SiSiC photonics platform and other hybrid SiSiC devices.

Looking beyond low-loss integrated photonic resonators, we envision our SiSiC as a promising platform for quantum and nonlinear photonics, particularly for applications that would otherwise suffer performance from harsh SiC etching. As practical demonstrations, we have numerically designed a 1D photonic crystal (PC) cavity and an electro-optic (EO) modulator based on our SiSiC platform (see Supporting Information). We have designed the PC cavity to operate near the emission wavelength (1300 nm) of the SiC vanadium spin-defect[32,33] and calculated Purcell factors in the SiC substrate as large as 900. Our design could improve the emission rates of these quantum emitters or easily be modified to address other SiC near-surface telecom defects. For the EO modulator device, we have calculated a half-wave voltage length product of $V_\pi L \approx 56\ V \cdot$ cm, a value comparable to current SiC-on-insulator integrated modulators.[5] Further design optimization could reduce this value and provide functionality to a wide range of modulator-based applications, such as high-speed communications, frequency comb generation, and wavelength conversion. These devices demonstrate the relevant application of our SiSiC platform to the important fields of both quantum and nonlinear photonics.

3. Conclusion

In summary, we have demonstrated a heterogeneous Si-on-SiC platform that supports infrared ring resonators with quality factors exceeding 10^5. We have identified several design parameters which, with further optimization, may enable resonators to approach bulk material loss-limited quality factors of 10^7 or greater.[8] Our fabrication processes are scalable and CMOS-compatible, offering a path toward wafer-scale SiSiC integrated devices free from SiC microfabrication. Moreover, the geometry-dependent mode overlap means we can engineer the effective optical properties and leverage attributes of both Si and SiC. This feature is of particular importance to quantum and nonlinear applications, which we have shown in our PC cavities and EO modulator numerical designs. Therefore, our versatile hybrid platform has great potential for future wafer-scale linear, quantum, and nonlinear photonic integrated devices.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

direct bonding, heterogeneous materials, integrated photonic circuits

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