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On-Chip Active Pulse-Clamp Stimulation (APCS) for Rapid Recovery, Charge-Balanced Neural Stimulation

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***Abstract*—Rapid and charge-balanced electrical stimulation is imperative for neurostimulation implants aimed at chronic safety and closed-loop usage. We present an innovative stimulation technique, Active Pulse-Clamp Stimulation (APCS), designed to ensure dependable charge balance with rapid recovery. The APCS technique has two distinctive modes, linear and slewing modes, both incorporated into the on-chip APCS system. APCS employs discrete-time feedback to sense the residual voltage across the electrode's double-layer capacitance, expediting the settling of the electrode interface by either grounding (slewing) or clamping with an amplifier (linear). APCS combines the strengths of both biphasic stimulation and passive recharge, with a customizable recovery time constant set by the user while offering a guaranteed charge balance for safety. To showcase the proof-of-concept for APCS, we implemented the on-chip APCS using a 180nm CMOS process. We demonstrated combined APCS functionality using a benchtop electrode model and a real clinical deep brain stimulation (DBS) electrode in vitro.**

***Index Terms*—Active Pulse-Clamp Stimulation (APCS), charge balancing, CMOS, electrodes, neurostimulation**

I. Introduction

Closed-loop neuromodulation is a promising advancement that delivers dynamic treatment based on the physiological response from the stimulation site [1]. However, stimulation artifacts can saturate sensitive recording circuitry with a long recovery time, preventing the front end from recording until the residual voltage on the electrode settles within the front end's linear input range for closed-loop applications [2].

Biphasic stimulation with a current-mode reversal phase can freely control the charge recovery time. Unfortunately, biphasic stimulation poses risks to the charge balance of the electrode interface. Slight discrepancies in the stimulation circuit can introduce a charge imbalance between the stimulation and reversal phases [3]. In addition, the inherent nonlinearity of the electrode model may lead to further deterioration of the charge imbalance situation [4]. As a result, many biphasic stimulators are complemented by a passive recharge phase to guarantee charge balance, prolonging the recovery time [5], [6].

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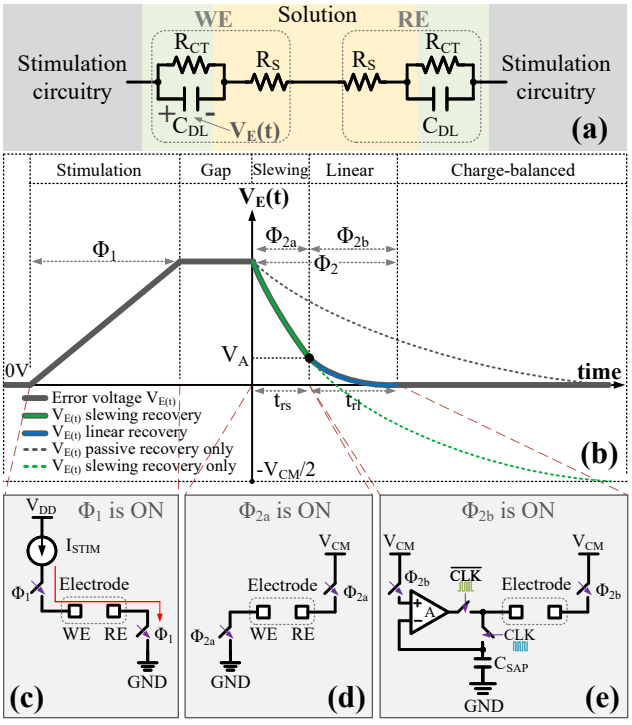

Fig. 1. APCS Theory. (a) Randles circuit model for the electrode-electrolyte interface. (b) Error voltage $V_E(t)$ across C_{DL}. (c) Equivalent circuit during Φ_1. (d) Equivalent circuit during Φ_{2a}. (e) Equivalent circuit during Φ_{2b}.

Monophasic stimulation followed by a passive recharge phase can help ensure the charge balance of the stimulation on the electrode interface [7], [8]. According to the Randles circuit model of the electrode [9] (Fig. 1a), the recovery period typically follows an exponential decay function with an intrinsic time constant determined by the electrode properties ($\tau \approx R_S \cdot C_{DL}$) [10]. This method is reliable for charge balancing. However, the limitation of passive recharge is the often long recovery time set by the electrode's inherent time constant. For example, a typical deep brain stimulation (DBS)

electrode has a τ of a few milliseconds, and several τ are needed to sufficiently recover the interface.

Here, we present an on-chip Active Pulse-Clamp Stimulation (APCS) system, which achieves rapid interface recovery stimulation with charge balance. APCS has two different modes of operation: linear and slewing. The principle behind both modes involves discrete-time feedback and sense, where a small on-chip capacitor monitors the residual voltage across the electrode. The APCS stimulation starts with slewing mode for maximum speed and efficiency, then transitions to linear mode for final fine settling. The linear mode of APCS was introduced in previous work [11].

II. Theory

A. Active Pulse-Clamp Stimulation (APCS)

Based on the Randles circuit model for the electrode in Fig. 1a, the charge transfer resistor R_{CT}, modeling charge transfer across electrode interface at steady state, is often considered to be very large if little irreversible Faradaic chemical reactions are occurring. R_S is the spread resistance, representing the resistivity of the tissue due to the current distribution. C_{DL} is the double-layer capacitor that models the charge separation at the electrode-tissue interface. C_{DL} is also the main storage for any reversible charge incurred. The electrode has an intrinsic time constant dictating passive recharge time (exponential decay in grey dashed line in Fig. 1b), given by

$$\tau = R_S \cdot C_{DL} \tag{1}$$

Fig. 1b shows the error voltage $V_E(t)$ across C_{DL}. The goal is to rapidly clear the residual charge stored across C_{DL} and return V_E to 0V. During Φ_1, the stimulation current I_{STIM} charges the C_{DL} linearly with the assumption that R_{CT} is very large (Fig. 1c). Assuming no charge is lost during the interphase gap, $V_E(0)$= $\frac{I_{STIM} \cdot T}{C_{DL}}$. Then the recovery phase Φ_2 must transfer the same amount of charge to achieve charge-balanced stimulation so V_E returns to 0V.

B. Slewing Mode of APCS

Slewing APCS (Fig. 1d) uses an increased current for improved recovery speed and dynamically detects V_E to stop the discharge and prevent overshoot, which is described by the solid green line in Fig. 1b. During Φ_{2a}, the return electrode (RE) is connected to common-mode voltage supply V_{CM}, and the working electrode (WE) is connected to the lowest potential on the chip (e.g., ground). While the time constant is unchanged (electrode time constant), the discharge time is reduced due to the increased current. Dynamic detection of V_E is required to stop the discharge and prevent overshoot. During Φ_{2a}, a 2-electrode load's V_E follows,

$$V_E(t) = \left(V_E(0) + \frac{1}{2}V_{CM}\right) \cdot e^{(-t/\tau)} - \frac{1}{2}V_{CM} \tag{2}$$

where τ is the intrinsic electrode time constant. V_E settles to negative $0.5V_{CM}$ if time goes to infinity, illustrated by the green dashed line in Fig. 1b. To prevent this over-discharge, slewing should be disabled when V_E drops to a certain threshold, V_A. Thus the duration of Φ_{2a}, t_{rs}, becomes,

$$t_{rs} = -ln\left(\frac{V_A + \frac{1}{2}V_{CM}}{V_E(0) + \frac{1}{2}V_{CM}}\right) \cdot \tau \tag{3}$$

C. Linear Mode of APCS

During Φ_{2b}, slewing APCS is disabled, and linear APCS takes over (Fig. 1e). Linear APCS uses an amplifier to precisely settle the electrode interface. It has two distinctive states toggled by a nonoverlapping clock. At first, during the monitoring state, a relatively small sampling capacitor C_{SAP} samples the error voltage across the electrode. The sampling time constant, $R_S{\cdot}C_{SAP}$, must be small enough to sample accurately and quickly during this sampling period T_{SAP}. During the second state, the active clamping state, C_{SAP} is disconnected from the electrode, and the amplifier discharges the electrode. The discharge current is $-V_E(t){\cdot}G_M$ (G_M is the amplifier's transconductance). Following certain periodic clock cycles, the amplifier clears the remaining residual charge stored in C_{DL}. In theory, linear APCS modifies the original electrode time constant to a new time constant, when the ideal amplifer has high output impedance [11], τ_{mod} becomes

$$\tau_{mod} \approx \frac{C_{DL}}{G_M} \tag{4}$$

making the duration of Φ_{2b} for a certain accuracy ε (ε=$\Delta V/V_E(0)$) to be

$$t_{rl} = -ln\left(\varepsilon \cdot \frac{V_E(0)}{V_A}\right) \cdot \tau_{mod} \tag{5}$$

where ΔV and ε are the final settling voltage and accuracy respectively. For settling accuracy of 0.1%, t_{rl} is approximately $6.9\tau_{mod}$. And the total recovery time is equal to the sum of t_{rs} and t_{rl},

$$t_{tot} = t_{rs} + t_{rl} \tag{6}$$

With a careful design of a threshold voltage V_A, usually small but larger than ΔV, the slewing portion dominates for best effectiveness.

III. System Description

A. Architecture

Fig. 2e shows the system architecture of the on-chip APCS system with an electrode load. During Φ_1, the 6-bit IDAC injects I_{STIM} into the electrode with the RE electrode connected to the ground to maximize stimulation headroom. During Φ_2, the RE electrode is switched to a common mode voltage V_{CM} while the clock drives the APCS circuitry. During the monitoring state, the on-chip sampling capacitor C_{SAP}, 500fF, samples the total residual voltage across the electrode. The sampling voltage V_{SAP} is,

$$V_{SAP} = V_{CM} + \frac{2Q}{C_{DL}} \tag{7}$$

where Q=$I_{STIM} \cdot T_{\Phi_1}$. Then the clock goes low, the StrongARM latch compares V_{SAP} with a reference voltage V_{CM}+V_{TR} ($V_A \approx 0.5V_{TR}$). V_{TR} determines when APCS

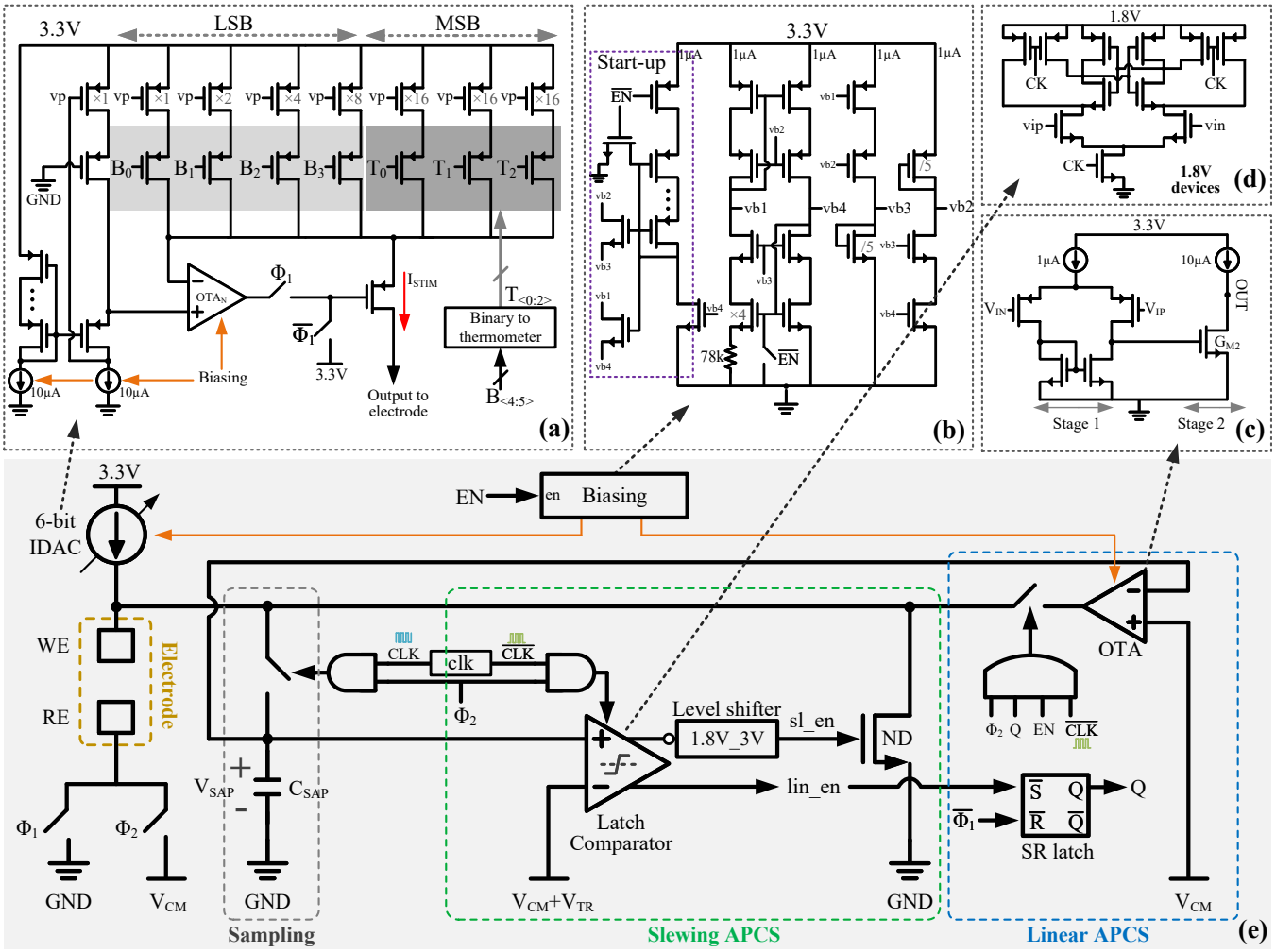

Fig. 2. APCS system description. (a) 6-bit IDAC. (b) constant-gm biasing with start-up and enable. (c) 5T-OTA for the linear mode of APCS recovery (d) StrongARM latch comparator. (e) System architecture combining slewing and linear mode of APCS.

stops slewing and enters linear mode. Slewing APCS can only sink current from the electrode load, unlike linear APCS. The ability to source and sink current is essential for linear APCS to stabilize and maintain the final electrode voltage at a specified steady-state level. The StrongARM in Fig. 2d was implemented with 1.8V core devices to facilitate comparison speed. The comparator's output is inverted and level-shifted to control the 3.3V NMOS pull-down switch (ND). The duty ratio (DR=$\frac{T_{SAP}}{T_{CLK}}$) is small so that more of the clock period is spent discharging the electrode rather than sampling its voltage. The comparator's other output can set the SR latch and gate 4-input AND gate to enable linear APCS circuitry when V_{SAP} drops below V_{TR}. The complement of Φ_1 resets the SR latch during each stimulation phase. The clock generator provides non-overlapping clocks. The static power consumption is 128.7μW during Φ_1, with a power shut-down mode controlled by EN signal. The power consumption is 1.8μW when the circuit is shut down. The chip core area is 0.098mm^2.

B. 6-bit IDAC

Fig. 2a, the 6-bit IDAC has 4-bit LSBs implemented with binary codes, and the 2-bit MSBs implemented with thermometer codes. All switches are 3.3V PMOS devices and an NMOS input folded cascode OTA regulates the IDAC cascode node and boosts the current source output impedance. The number of PMOS biasing devices stacked determines the bias voltage at the positive input of this folded cascode OTA. The output compliance voltage ranges from 0 to 3.17 V, corresponding to a 10% decrease in the maximum output current. The regulation feedback loop demonstrates a loop gain of 50dB, a phase margin of 80 degrees, and a gain-bandwidth product of 2MHz under maximum current load conditions. The nominal least significant bit (LSB) is 10μA, producing a maximal stimulation current I_{MAX}=630μA. Also, LSB can be adjusted by an external reference (Vb4) making the current range adjustable. The current mirror devices are sized to ensure that three times the maximum standard deviations of DNL and INL fall within half of the LSB. The measured maximum INL and DNL are 0.39LSB and 0.22LSB respectively.

C. Biasing

As in Fig. 2b, a constant-gm biasing with a start-up circuit provides bias to the stimulator IDAC and two OTAs. The external enable signal EN can duty cycle the bias circuit to turn off all static current flow to save power.

D. Amplifer

The 2-stage OTA for linear APCS is a 5T-OTA followed by a common source stage (Fig. 2c). The first stage provides a gain of 35dB and the second stage is a class-A type G_M stage for sinking or sourcing the electrode load. Fig. 3a shows the ideal continuous-time model for the discrete-time based linear APCS (Fig. 1e) when using a 2-stage OTA at periodic steady-state. At DC or low frequency, the equivalent output impedance $R_{S,mod}$,

$$R_{S,mod} = \frac{R_2 + R_S}{1 + A_1 A_2 \beta} \tag{8}$$

where A_1=$G_{M1} \cdot R_1$ and A_2=$G_{M2} \cdot R_2$ are DC gain of the first and second stage respectively. Feedback factor β=1. Typical spread resistance R_S is much smaller than R_2, which is the output impedance of the second stage. Thus the new modified time constant of the linear APCS is the product of the $R_{S,mod}$ and C_{DL},

$$\tau_{mod} \approx \frac{C_{DL}}{G_{M2}} \cdot \frac{1}{A_1} \tag{9}$$

in comparison to equation (4), the modified time constant is reduced by the gain of the first stage.

Fig. 3b shows a simplified circuit model for periodic steady-state stability analysis. The transfer function of the loop gain ($\frac{V_E}{V_{in1}}$) is,

$$LG(s) \approx A_1 A_2 \cdot \frac{1}{1 + s/p_1} \cdot \frac{1}{1 + s/p_2} \cdot \frac{1}{1 + s/p_3} \tag{10}$$

where $p_1 \approx -\frac{1}{R_2 \cdot C_{DL}}$ is the dominant pole. The second pole $p_2 \approx -\frac{1}{R_1 \cdot C_1}$ and third pole $p_3 \approx -\frac{1}{R_S \cdot C_2}$ are located at relatively high frequencies, making the loop gain almost behave like a single-pole system. For example, as shown in Fig. 3c, when V_{CM}=825mV is connected to the positive input of the OTA, the DC magnitude of the loop gain is $|A|$=$|A_1 \cdot A_2|$=70dB, the gain-bandwidth product is approximately 60kHz, and the phase margin is around 87 degrees.

IV. Results

A. Measurement across Electrode Model

Fig. 4a shows the timing diagram of the control signals for a single stimulation cycle. Fig. 4b shows the test setup for measuring the recovery voltage across the DBS electrode. To validate the theory equation (3), we built a Randle circuit model using surface mount components and measured t_{rs}. R_{CT}, R_S, and C_{DL} were 10MΩ, 2kΩ, and 120nF, respectively, based on modeling [2]. We set I_{STIM} to 130μA with a 300μs pulse width and 200μs interphase gap. The clock

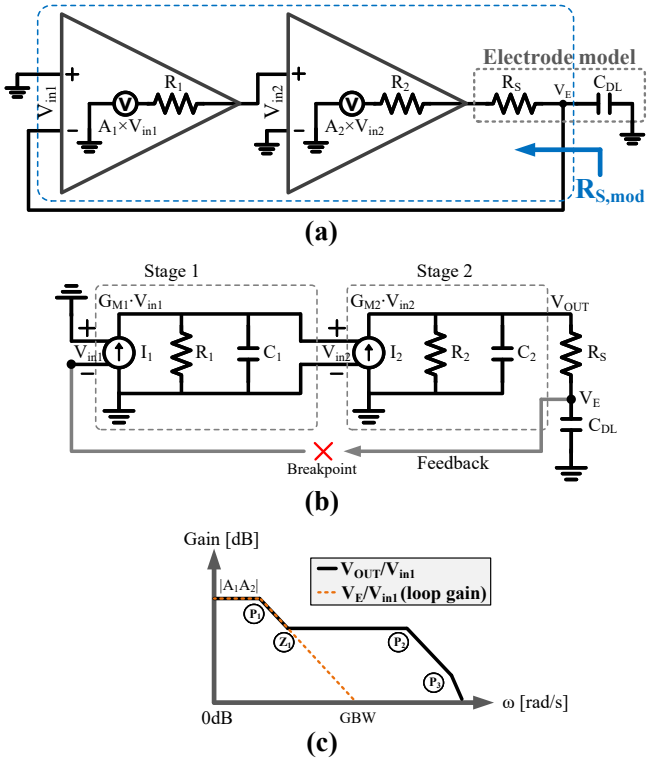

Fig. 3. Ideal steady-state model for low-frequency impedance and frequency response analysis during ϕ_{2b}. (a) Ideal continuous-time model for the linear APCS utilizing a 2-stage OTA. (b) Frequency response analysis model of a 2-stage OTA driving an electrode load. (c) Magnitude response of the loop gain.

frequency was 100kHz with a duty ratio DR of 0.1. Common-mode voltage supply V_{CM} and comparison threshold V_{TR} is set to 825mV and 20mV respectively ($V_A \approx 0.5V_{TR}$). The measured t_{rs} was 184μs, as in Fig. 5. By considering the nonidealities, equation (3) becomes

$$t_{rs} = -ln\left(\frac{V_A + \frac{1}{2}V_{CM} - V_{COR}}{V_E(0) + \frac{1}{2}V_{CM} - V_{COR}}\right) \cdot \tau \cdot \frac{1}{1 - DR} \tag{11}$$

where V_{COR} (=80mV) and $\frac{1}{1-DR}$ are used to compensate for the effect of the average ON-resistance of the ND switch and the non-zero duty ratio of the clock. The calculated theoretical t_{rs} was 174μs, which closely matched the measurement. Compared to the passive recharge which takes 835.5μs to reach V_A, the recovery speed is increased by almost 5 times.

B. In-Vitro Measurement

To demonstrate APCS with a real electrode, we conducted experiments measuring the differential electrode voltage in a 4-lead DBS electrode (Medtronic 3389-40) immersed in saline solution. With the same test setup and stimulation parameters except I_{STIM}=410μA, the measured V_{DIFF}, in Fig. 6b, quickly converges to zero in approximately 500μs. This DBS electrode has a time constant of about 1.8ms. To verify the chronic charge balance of the APCS system, we conducted experiments measuring the differential voltage across the DBS

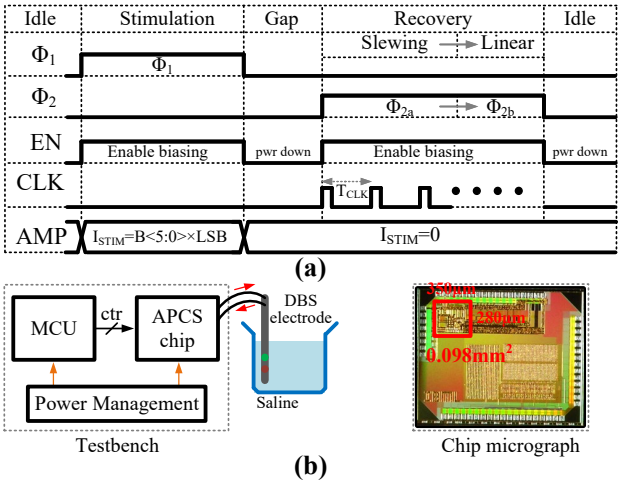

Fig. 4. Timing diagram and test setup. (a) Simplified digital timing control protocol. (b) Testbench setup concept and chip micrograph.

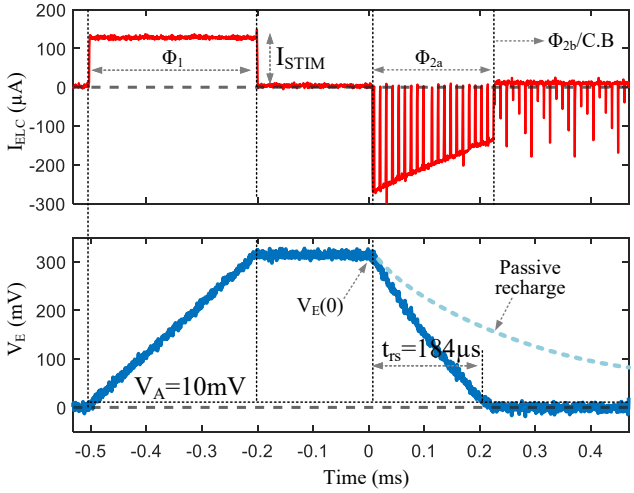

Fig. 5. Electrode current and error voltage measurement across ideal surface mount electrode circuit model.

electrode in saline with 500 cycles of consecutive APCS stimulation. For a charge-balanced APCS (T_{STIM}=11.5ms, stimulation pulse period), the measured differential electrode voltage shows a 0 average DC level throughout the whole 500 cycles in Fig. 6a. We used a moving mean window to calculate this DC level.

V. Conclusion

We presented an on-chip system, designed to perform rapid and charge-balanced stimulation. We combined slewing and linear modes of APCS operation to maximize recovery speed with a constrained headroom voltage available on-chip. We validated the theory governing the recovery time for slewing mode using the surface mount electrode model. We demonstrated combined APCS functionality and chronic safety with a clinical DBS electrode in vitro, allowing swift and safe stimulation for closed-loop neuromodulation.

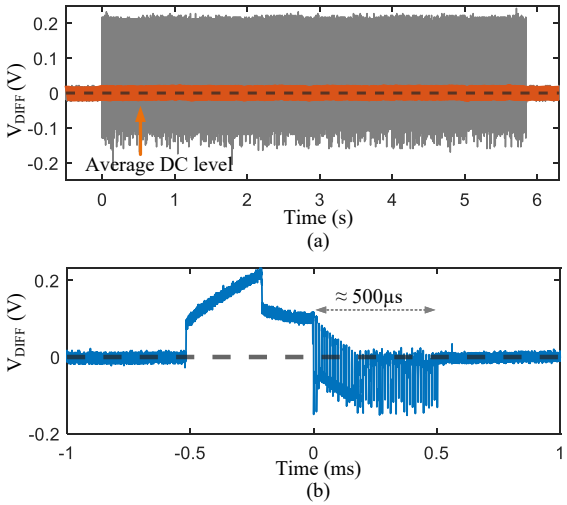

Fig. 6. Differential electrode voltage measurement of Medtronic DBS electrode. (a) V_{DIFF} of 500 consecutive stimulation pulses. (b) V_{DIFF} of a single APCS stimulation.

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