

A 4-Channel 0.23mm^2 Voltage-to-Time Converter AFE with $3.7\mu\text{V}_{\text{rms}}$ Noise and 480nW Galvanic Impulse Uplink

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Abstract—We present a 4-channel 15 kS/s Voltage-to-Time Converter (VTC) analog front-end (AFE) with a $0.49\mu\text{W}$ impulse-based galvanic uplink for a peripheral nerve interface. Multiple, low-noise, high-data-rate channels are needed to sense compound action potentials and measure their conduction velocity as they propagate down a peripheral nerve. To achieve high energy efficiency for these constraints, the AFE encodes and transmits data with time-domain charge-balanced impulses through an implantable galvanic link. Each channel consists of an integrator with charge-based sampling and amplification for rapid multiplexing. A shared VTC encodes the amplitude-domain outputs of each integrator into differential time-domain impulses. Since the timing can be synchronized with stimulation, this AFE achieves instant artifact recovery after rail-to-rail stimulation events. We designed this AFE in a 180nm CMOS process, and the simulation results show an SNDR of 60dB and noise of $3.7\mu\text{V}_{\text{rms}}$. Thanks to the new galvanic uplink protocol, this front-end only consumes $11.28\mu\text{W}$ including wireless data transmission for four channels.

Index Terms—Analog front-end (AFE), Neural recording, Voltage-to-time converter (VTC), Galvanic interface, Bidirectional neural interfaces, Wireless implant

I. INTRODUCTION

Deeply implanted wireless bidirectional peripheral neural interfaces will enable on-demand patient-specific therapeutic electrical stimulation. Ideally, these devices are miniaturized into an active extraneural nerve interface that is minimally invasive and placed at the target site. Also, an energy-efficient, high data rate uplink is desirable for back-and-forth communication with a wearable for closed-loop processing of electroneurogram (ENG) signals. ENG signals contain rich information related to function and dysfunction within the body. However, decoding ENG signals with an extraneural interface is exceptionally challenging due to the large number of fibers within each nerve and the low signal-to-noise ratio (SNR). Decoding these signals requires multiple sensing channels for spatial selectivity and a high sample rate for velocity selective recording [1]–[3].

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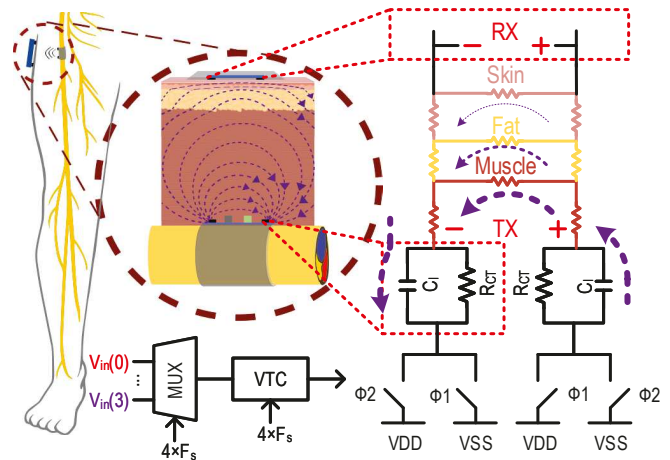


Fig. 1. Wireless peripheral implantable recording system with galvanic impulse uplink.

We previously showed that a galvanic interface is an efficient approach for deep-implant uplink protocol [2]. In heterogenous tissue (22mm of muscle, 20mm of fat, 2mm of skin), the link had only 36dB of loss with a 3mm implant. Here, we present a novel 4-channel VTC-based analog front-end (AFE) that enables a wireless time-domain galvanic uplink. Due to the use of memoryless charge-based sampling, this front-end achieves instant artifact recovery and fast settling time while achieving high linearity [4]. We utilize a chopping technique to reduce flicker noise, kT/C noise, and die area. Fig. 1 shows a conceptual figure of the system that wraps around the sciatic nerve [1], and sends galvanic time-domain impulses to the wearable for data acquisition. Overall, this solution achieves low noise, small die and system area, high linearity, instant artifact recovery, and fully-differential sensing across the electrodes.

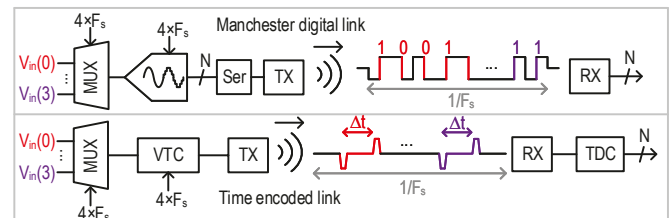


Fig. 2. The concept of digital and time encoded wireless data transition for an implanted galvanic link.

II. TIME-BASED DATA TRANSMISSION FOR A GALVANIC INTERFACE

One method of sending data through a galvanic interface is to use a Manchester-encoded digital link to ensure that the interface is safely charge-balanced [5] (Fig. 2). However, this method results in a constant current draw through the galvanic interface since the output pulse needs to be either one or zero. Using a small window of the sample time for data transmission can reduce TX power consumption by transmitting data faster; however, this requires a faster clock which increases system power consumption. For example, [6] has a pulse width of 500ns. Assuming that the electrode's spread resistance (R_s) is 300Ω [7], the protocol transmits 10 bits of data with a sample rate of 15 kS/s, and the system uses a supply voltage of 1.2 V, the power consumption of the Manchester encoded protocol with four recording channels would be $720\mu W$. To improve this, time-encoded data telemetry makes the data rate independent of the resolution. Here, the AFE encodes neural data in the delay between two impulses. As we show in Fig. 2, there are only two pulses per channel regardless of resolution. In the wearable, a time-to-digital converter (TDC) converts the time-encoded data into the digital domain. This technique results in much fewer pulses for equivalent information and places most of the processing burden on the wearable that has relaxed size and power constraints.

III. ARCHITECTURE AND CIRCUIT DESIGN

Two approaches have been presented for implementing a VTC-based neural AFE: voltage-controlled oscillator (VCO) based VTCs [8] and sample and evaluation-based VTCs [9]. Although VCO-based VTCs can achieve high linearity with mixed signal feedback techniques, this creates major challenges in wireless recording circuitry since it increases the data rate and complexity of the system [10]. [9] presented a neural recording system that encoded neural data in time-domain pulses and used a capacitive link for data transmission. While pulse width modulation reduces the data rate requirement in an implantable recording system, it will alias electrode thermal noise and be susceptible to stimulation artifacts.

We present a VTC-based AFE co-designed with a galvanic interface to enable a high data rate and energy-efficient wireless link. Overall, this solution achieves low noise, small die and system area, high linearity, instant artifact recovery, and fully-differential sensing across the electrodes.

Fig. 3 shows the architecture and circuit details of the AFE. Each channel contains an integrator and a nonoverlapping clock generator and shares the VTC and pulse encoder (ENC) with the other channels. To enable memoryless charge-based sampling in this integrator, an auto-zero (AZ) clock is used to reset the integrator before every integration window. Charge-based sampling enables intrinsic anti-aliasing characteristics since the integrator has a sinc transfer function and a band-

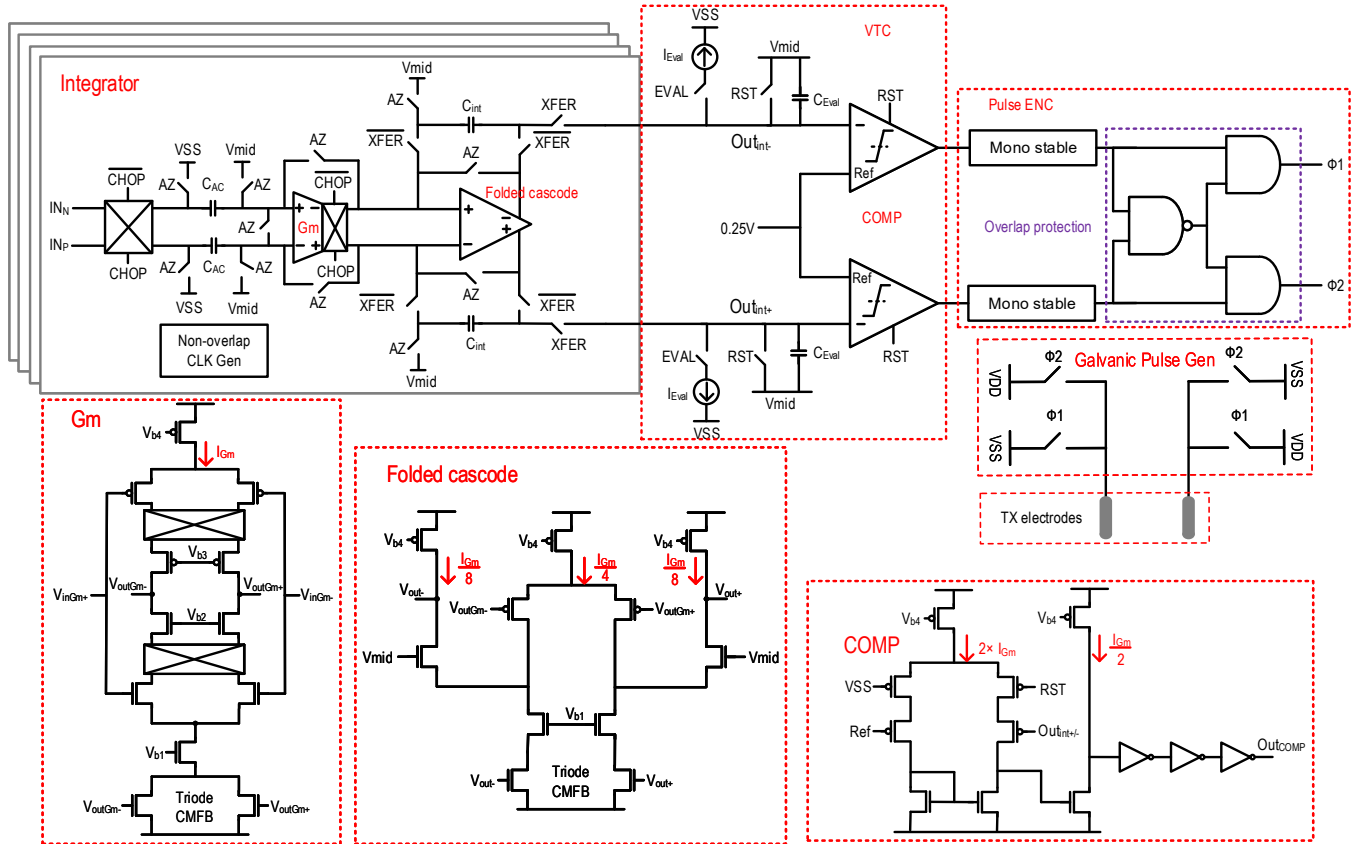


Fig. 3. Circuit architecture of the 4-channel VTC-based AFE.

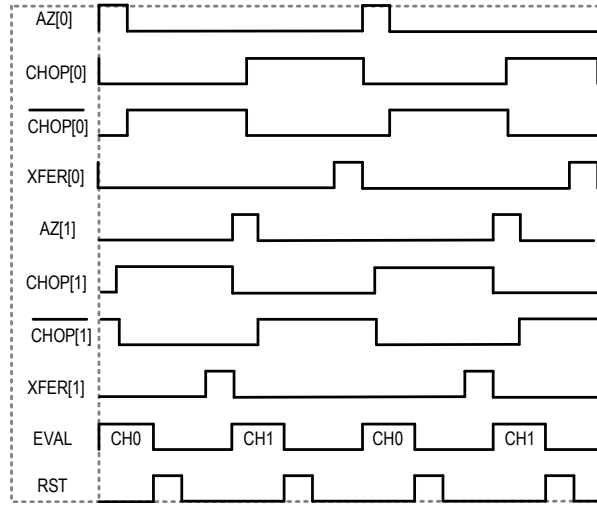


Fig. 4. Front-end timing diagram. The timing is interleaved for all four channels.

width of $0.44/T_S$ [11]. Here, T_S is the sample time (integration window).

The chopping technique mitigates flicker and kT/C noise using double integration with opposite polarities [12], [13], maintaining a small size for the input devices in the Gm-cell (NMOS: $W/L = 8 \times 2.8\mu\text{m}/4\mu\text{m}$, PMOS: $W/L = 8 \times 4.7\mu\text{m}/2\mu\text{m}$) and input capacitors, $C_{AC} = 4\text{pF}$. Utilizing a current reuse topology for the Gm-cell improves overall g_m/I_d and the integrator gain which is $G_M \times T_S/C_{int} = 120\text{V/V}$ with $G_M = 10\mu\text{S}$ and $C_{int} = 5.28\text{pF}$. To achieve fast settling for the chopping switches, the down-modulation switches are placed at low-impedance nodes inside the Gm-cell [14]. We used a folded cascode to drive the integrator output to satisfy the output swing requirements (1.2Vpp fully differential).

Fig. 4 shows the timing operation of the integrator. For clarity, the timing diagram shows only two channels. To multiplex the VTC between the channels, the input clocks of the four channels are shifted by 90° with respect to each other. The repetition rate of the VTC is four times the repetition rate of the integrators to process all channels in every $1/F_s$ cycle. The voltage-to-time conversion for each channel happens in two steps. First, the integrator integrates the charge on the capacitors during a T_S cycle using the charge-based sampling technique. In the next step, the charges are transferred to $C_{EVAL} = 1\text{pF}$ capacitors and discharged using current sources $I_{EVAL} = 200\text{nA}$ (Fig. 3 and Fig. 5). The time difference between the output ramps (Out_{int+} and Out_{int-}) crossing the reference voltage (0.25 V) determines the delay between $\Phi 1$ and $\Phi 2$ pulses. These signals control the galvanic uplink interface in Fig. 1 [2]. The delay between $\Phi 1$ and $\Phi 2$ pulses can range between $-2.363\mu\text{s}$ to $+2.363\mu\text{s}$ to represent the front-end's input voltages that can range from -5mV to $+5\text{mV}$. The total gain of the front-end is $472.6\text{ps}/\mu\text{V}$.

At the galvanic interface, two electrodes are used on the TX side to generate the galvanic impulse. These electrodes transfer the ions across the tissue. Two electrodes receive the waveform on the RX side. The ENC uses an overlap protection

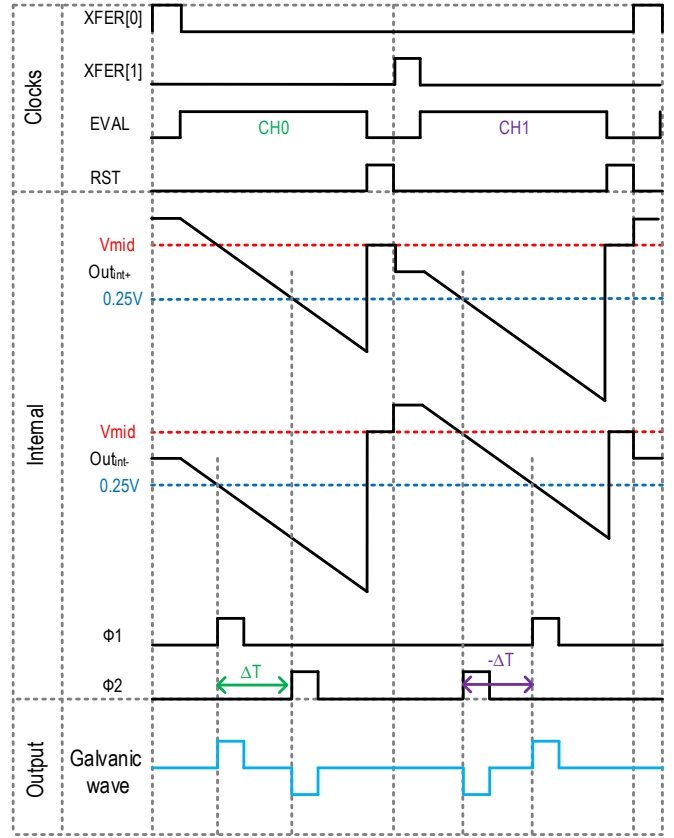


Fig. 5. The VTC timing diagram.

circuit to ensure $\Phi 1$ and $\Phi 2$ do not overlap and short VDD and VSS. In this case, neural data are encoded in the pulse width of the first impulse instead of the delay between impulses. The VTC also encodes the sign of the input data using the order of the impulses (up, down OR down, up) (Fig. 5). In Fig. 5, CH0 has an output value above the mid-scale and CH1 has an output value below the mid-scale. The VTC consists of two pairs of degenerated current mirrors for high linearity and low noise, and asynchronous comparators. The comparators consist of two stages. The first stage functions as a pre-amplifier and the second stage of inverters enables a high gain. A RST input is used in the comparator to ensure that the initial condition of the comparator is not correlated with its input. The triode reset switch source degenerates the input device to increase linearity. In order to mitigate the mismatch effects, we designed the layout of all the analog circuitry including the gm cell, folded cascode, comparators, and current mirrors with an interdigitated method.

In contrast to [9], this front end uses a different set of capacitors for voltage-to-time conversion than sampling to enable the evaluation of the current channel while the next channel is sampled. With charge-based sampling paired with coordinated stimulation and recording [4], this front-end can withstand rail-to-rail stimulation artifacts and instantly recover. Fig. 6 shows the chip micro-graph and layout of this 4-channel front-end that we designed using 180nm CMOS technology.

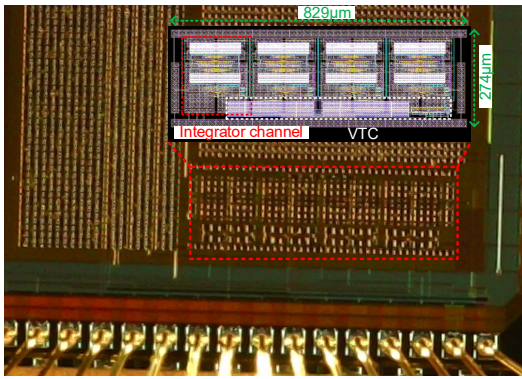


Fig. 6. The chip micro-graph and layout.

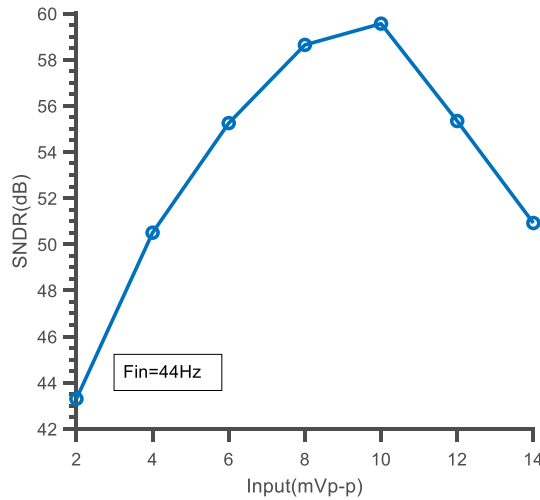


Fig. 7. The SNDR versus peak-to-peak input.

IV. RESULTS

The noise of this VTC-based front-end will present as a timing jitter caused by various noise sources, dominated by the Gm-stage. To simulate this effect, we performed repetitive transient noise simulations and calculated the standard deviation of the output to be 1.75 ns. This corresponds to a total input-referred noise of $3.7\mu V_{rms}$. The digital and analog power consumption per channel were $17.26nW$ and $2.8\mu W$, respectively. Fig. 7 shows the SNDR versus the peak-to-peak input. The effective number of bits (ENOB) was 9.6 at a 10mVp-p input. To evaluate the spike-sensing capability, we used extracellular prerecorded data from the hippocampus region of a rodent [15]. Fig. 8 shows representative time-encoded pulses and the reconstructed amplitude domain signal output that accurately tracked the neural data input.

To evaluate artifact mitigation capability, we combined a 100Hz 10mVp-p sinusoidal signal with a stimulation pulse that had a 130Hz repetition rate, $266\mu s$ pulse width, and 1.2V amplitude. Fig. 9 shows that the front-end instantly recovered after each stimulation pulse.

V. CONCLUSION

We presented a VTC-based analog front-end for peripheral nerve recording applications. This front-end encodes and trans-

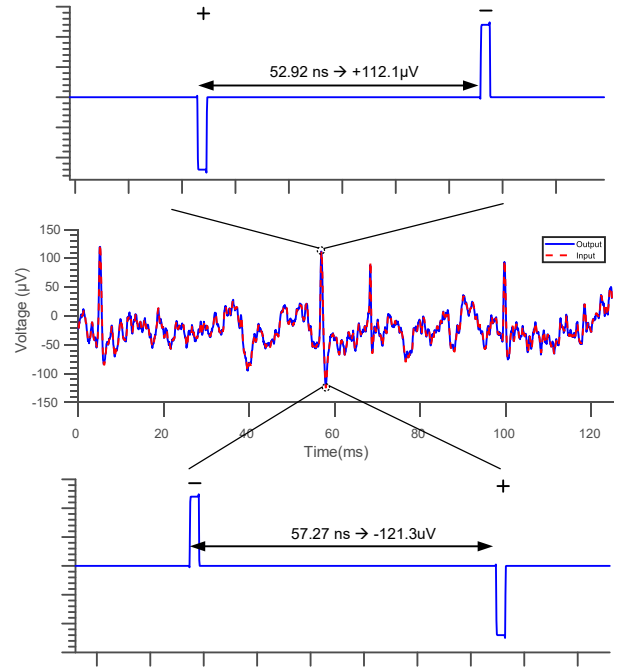


Fig. 8. The prerecorded spike data, output impulse of the galvanic TX link, and the input-referred amplitude domain output of the front-end.

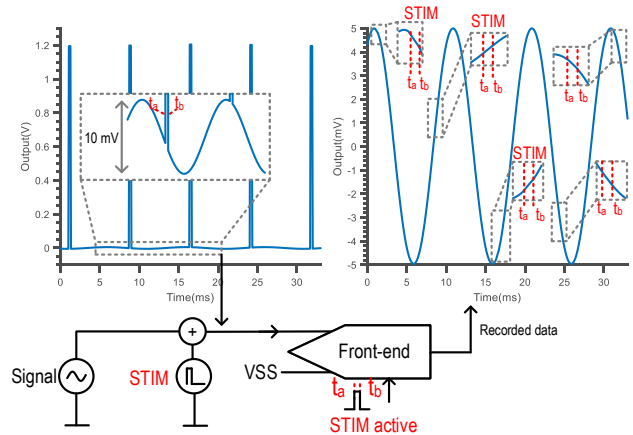


Fig. 9. The test bench for evaluating artifact mitigation capability.

mits data in the delay between two impulses with opposite polarities to relax the data rate requirement and power consumption in the galvanic link. We designed this front end for a galvanic interface and ensured electrical safety by consecutive galvanic impulses with opposite polarity to ensure charge balance. In addition to enabling a high data rate and a power-efficient data transmission protocol, this front-end achieved a small area, low noise, low power consumption, high artifact tolerance, and instant artifact recovery which are critical in a closed-loop neuromodulation system. Table I compares this work with state-of-the-art. Our work achieves the best noise performance in this table and is the only work to have artifact cancellation capability while having comparable power, area, and linearity.

TABLE I
THE COMPARISON TABLE

Specs	[6] JSSC 2022	[16] ISSCC 2020	This work
Tech(nm)	40	180	180
Supply(V)	1.1	1.5	1.2
Num. CH	2	1	4
Power/CH (μ W)	>14.1	0.74	2.82
Area/CH(mm^2)	>0.16	0.0323	0.06
BW/CH (kHz)		0.18-0.95	7.5
ENOB	5		9.6
IRN ($nV/\sqrt{Hz}$)	>72.35	172.98	42.72
Artifact cancellation	None	None	Instant artifact recovery
TX interface	Galvanic	Optical	Galvanic
TX protocol	Event-driven delta-encoded impulses	Symbol interval modulation	Time encoded impulses
TX power (μ W)	1.2 (With 125X data compression)		0.49 (Full data rate)

REFERENCES

- [1] Morgan Riley, FNU Tala, Katherine J Johnson, and Benjamin C Johnson. Fully customizable, low-cost, multi-contact nerve cuffs for spatially selective neuromodulation. 2023.
- [2] Morgan Riley, FNU Tala, Mehdi Bandali, and Benjamin C Johnson. Wireless galvanic impulse communication for high-throughput, low-power, miniaturized neuromodulation implants. 2023.
- [3] Felipe Rettore Andreis, Benjamin Metcalfe, Taha Al Muhammadee Janjua, Winnie Jensen, Suzan Meijs, and Thomas Gomes Nørgaard dos Santos Nielsen. The use of the velocity selective recording technique to reveal the excitation properties of the ulnar nerve in pigs. *Sensors*, 22(1):58, 2021.
- [4] M. Bandali and B. C. Johnson. An artifact-resilient neural recording front-end with rail-to-rail dm and cm offset correction. In *IEEE ISCAS 2023 - 58th Edition IEEE International Symposium on Circuits and Systems*, 2023.
- [5] Daniel R Merrill, Marom Bikson, and John GR Jefferys. Electrical stimulation of excitable tissue: design of efficacious and safe protocols. *Journal of neuroscience methods*, 141(2):171–198, 2005.
- [6] Yuming He, Federico Corradi, Chengyao Shi, Stan van der Ven, Martijn Timmermans, Jan Stuijt, Paul Detterer, Pieter Harpe, Lucas Lindeboom, Evelien Hermeling, et al. An implantable neuromorphic sensing system featuring near-sensor computation and send-on-delta transmission for wireless neural sensing of peripheral nerves. *IEEE Journal of Solid-State Circuits*, 57(10):3058–3070, 2022.
- [7] F. Tala, M. Bandali, and B. C. Johnson. Automated distributed element model generation for neural interface co-design. In *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 917–920, 2020.
- [8] Fernando Cardes, Ebrahim Azizi, and Andreas Hierlemann. A time-domain readout technique for neural interfaces based on vco-timestamping. *IEEE Transactions on Biomedical Circuits and Systems*, 2023.
- [9] Baibhab Chatterjee, K Gaurav Kumar, Shulan Xiao, Gourab Barik, Krishna Jayant, and Shreyas Sen. A 1.8μ W 5.5 mm^3 adc-less neural implant soc utilizing 13.2pj/sample time-domain bi-phasic quasi-static brain communication with direct analog to time conversion. In *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC)*, pages 209–212, 2022.
- [10] Mahin Esmaeilzadeh, Yves Audet, Mohamed Ali, and Mohamad Sawan. A low-phase-noise cmos ring voltage-controlled oscillator intended for time-based sensor interfaces. *IEEE Access*, 10:101186–101197, 2022.
- [11] Gang Xu and Jiren Yuan. Performance analysis of general charge sampling. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 52(2):107–111, 2005.
- [12] Simone Gambini, Karl Skucha, Paul Peng Liu, Jungkyu Kim, and Reut Krigel. A 10 kpixel cmos hall sensor array with baseline suppression and parallel readout for immunoassays. *IEEE journal of solid-state circuits*, 48(1):302–317, 2012.
- [13] Benjamin C Johnson, Simone Gambini, Igor Izyumin, Ali Moin, Andy Zhou, George Alexandrov, Samantha R Santacruz, Jan M Rabaey, Jose M Carmenta, and Rikky Muller. An implantable 700μ W 64-channel neuromodulation ic for simultaneous recording and stimulation with rapid artifact recovery. In *2017 Symposium on VLSI Circuits*, pages C48–C49. IEEE, 2017.
- [14] Tim Denison, Kelly Consoer, Wesley Santa, Al-Thaddeus Avestruz, John Cooley, and Andy Kelly. A 2μ W 100 nV/rthz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials. *IEEE journal of solid-state circuits*, 42(12):2934–2945, 2007.
- [15] DA Henze, KD Harris, Z Borhegyi, J Csicsvari, A Mamiya, H Hirase, A Sirota, and G Buzsáki. Simultaneous intracellular and extracellular recordings from hippocampus region cal of anesthetized rats. *CRCNS. org*, 2009.
- [16] Jongyup Lim, Eunseong Moon, Michael Barrow, Samuel R Nason, Paras R Patel, Parag G Patil, Sechang Oh, Inhee Lee, Hun-Seok Kim, Dennis Sylvester, et al. $26.9\text{ a }0.19\times 0.17\text{ mm}^2$ wireless neural recording ic for motor prediction with near-infrared-based power and data telemetry. In *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*, pages 416–418. IEEE, 2020.