Design and Implementation of a D-Band Bidirectional Common-Gate Amplifier in 45-nm RFSOI

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***Abstract*— This article presents a new design methodology for a D-band bidirectional amplifier that leverages the inherent symmetry of CMOS transistors in a common-gate amplifier. The proposed design exploits symmetric passive networks that achieve interstage conjugate matching conditions in forward and reverse amplifications while minimizing the switching loss in support of bidirectional amplification. A current-reuse technique is proposed to reduce power consumption by sharing the supply current between the adjacent amplifier stages. Two prototype D-band bidirectional amplifiers have been implemented using a 45-nm RFSOI process: transformer and transmission line-based amplifiers. The 103–123-GHz transformer-based amplifier reports measured peak gains of 9 and 7.5 dB in forward and reverse amplifications with a 3-dB bandwidth of 20 GHz, an average noise figure (NF) of 6.3 dB, and a DC power consumption of 25.5 mW. The 124–145-GHz transmission line-based amplifier reports a measured peak gain of 14 dB, a 3-dB bandwidth of 21 GHz, and an average NF of 7 dB with a DC power consumption of 28.5 mW.**

***Index Terms*— 140-GHz, bidirectional amplifier, CMOS, D-band, low-noise amplifier, phased array, transceiver (TRX).**

I. Introduction

As THE demand for wireless data continues to explode and emerging applications such as augmented reality (AR), virtual reality (VR), autonomous vehicles, and industrial Internet of Things (IoT) become increasingly prevalent, the utilization of the D-band spectrum (110–170 GHz) becomes critical due to its large available bandwidth [1], [2]. However, exploiting such a high-frequency spectrum poses significant challenges due to the severe path loss and limited transistor performance of silicon RF ICs [3], [4]. To address the challenges, large-scale phased array transceivers are essential [5]. To reduce the size of the phased array transceiver module, each antenna can be shared for both the transmitter (TX) and receiver (RX) operation using time division duplex (TDD) operation. Separate amplifier chains for TX and RX are combined through single-pole–double-throw (SPDT) switches, which connect shared components to either the TX or RX circuits depending on the mode of operation [6], [7]. However, at the D-band frequencies, the insertion loss of silicon-based SPDT switches can be as high as 2.5 dB [8], [9]. Furthermore, beamformer ICs with separate TX and RX blocks make fitting them in small antennas-in-package (AiP) difficult.

To remove lossy SPDT switches and reduce chip area, a bidirectional amplifier can be a good solution, which provides forward and reverse amplifications within a single amplifier footprint. Different types of bidirectional amplifiers have been proposed for frequencies below 90 GHz [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. One of the prior bidirectional amplifiers was based on two cross-connected common-source amplifiers, as shown in Fig. 1(a). In this topology, one transistor's gate and drain are connected to the other transistor's drain and gate, respectively, with switchable bias. Depending on whether the circuit is amplifying signals in forward or reverse, only one transistor is turned on at a time, and the same matching networks are shared in both directions for a small footprint [12]. However, sharing passive networks for both signal directions presents challenges for achieving simultaneous input and output matching conditions [12]. In addition, loading from OFF-state transistors degrades the maximum available gain (MAG), which becomes more critical above 100 GHz. Differential variations of this topology were proposed to improve the MAG by adding neutralization capacitors, as shown in Fig. 1(b) and (c) [15], [19]. Fig. 1(b) utilizes series switches at the gate terminals to isolate PA and LNA operations to address PA linearity degradation caused by the OFF-state LNA transistor. However, additional resistance due to the gate switch significantly degrades the achievable gain and noise figure (NF) [15]. Fig. 1(c) employs a PMOS-based LNA to remove the gate switches. However, the PMOS-based amplifier has lower $f_{\max}$ and MAG than the NMOS-based implementation, which limits its use at the D-band frequencies. In addition, the loading from OFF-state transistors still degrades the MAG.

For power-efficient, bidirectional amplification at the D-band frequencies, we propose a new design methodology that exploits the source–drain symmetry of a common-gate amplifier, as shown in Fig. 1(d). The proposed design leverages symmetric passive networks that achieve the interstage conjugate matching condition for forward and reverse amplifications without lossy switches on the RF signal path in a multistage bidirectional amplifier. A current-reuse technique is proposed to reduce DC power consumption by sharing the same supply current between the adjacent stages. Based on the

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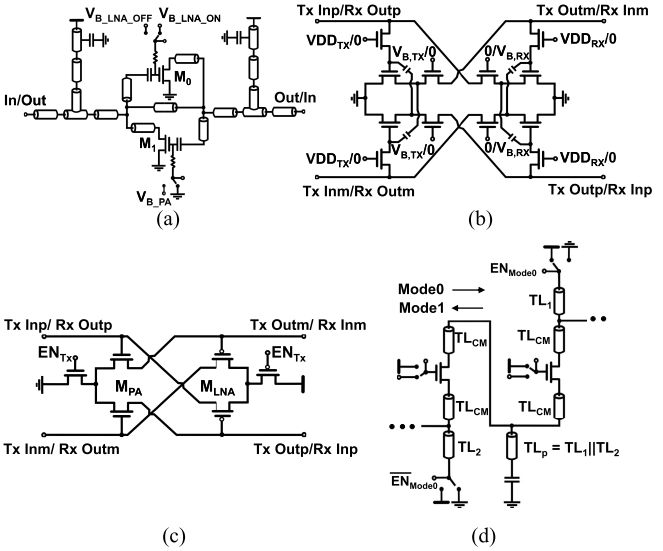


Fig. 1. (a)–(c) Prior arts of bidirectional amplifiers. (d) Proposed bidirectional amplifier. Matching networks are not included in (b) and (c).

proposed design methodology, two prototype D-band bidirectional amplifiers are designed using GlobalFoundries 45-nm RFSOI process: a 103–123-GHz transformer-based bidirectional amplifier and a 124–145-GHz transmission line-based bidirectional amplifier. The transformer-based design reports measured gains of 9 and 7.5 dB at 110 GHz for forward and reverse amplifications with a 3-dB bandwidth of 20 GHz and a DC power consumption of 25.5 mW. The transmission line-based design reports a measured gain of 14 dB at 130 GHz in both directions with a 3-dB bandwidth of 21 GHz and a DC power consumption of 28.5 mW. This article expands on a prior conference publication in [20]. Beyond the brief description of the prototype transmission line-based design reported in the conference article, this article presents a general design methodology of the proposed bidirectional amplifier and two prototype D-band bidirectional amplifiers based on transformers and transmission lines using the proposed design methodology.

II. Applications of CMOS Bidirectional Amplifiers

The proposed CMOS bidirectional amplifier can be utilized for: 1) distribution loss compensation in a multi-channel beamformer IC and 2) a compact CMOS beamformer transceiver co-integrated with indium phosphide (InP) front-end ICs for a sub-THz beamformer module. For a multi-channel mmWave beamformer transceiver using the RF phase-shifting architecture, line amplifiers can compensate for high distribution loss [7], [21] and relax the gain requirement of each TRX front end for reduced overall power consumption, as shown in Fig. 2(a). TX and RX signal chains need separate distribution networks with unidirectional line amplifiers, increasing chip area significantly [7]. Instead, bidirectional line amplifiers shared by TX and RX signal paths can be used with a single passive distribution network for smaller chip areas and simpler interconnects, as shown in Fig. 2(b).

On the other hand, a CMOS bidirectional amplifier can be the key building block of a heterogeneously integrated

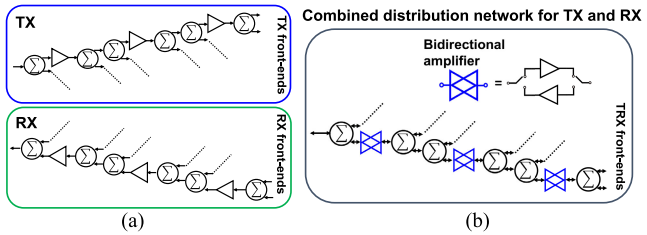


Fig. 2. (a) Separate TX and RX distribution networks of a multi-channel beamformer transceiver due to uni-directional line amplifiers [7]. (b) TX and RX common distribution networks enabled by bidirectional line amplifiers for a compact chip area.

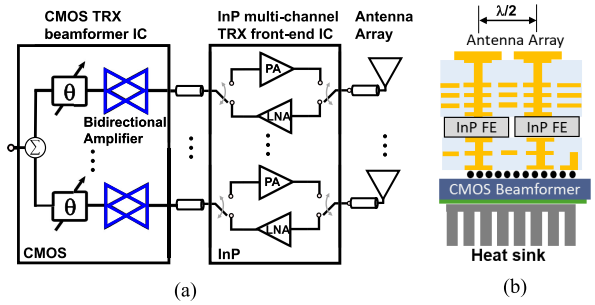


Fig. 3. InP and CMOS IC co-integration for sub-THz beamformer transceiver modules, where bidirectional amplifiers are used as CMOS TRX front ends. (a) Block diagram and (b) AiP cross section for $\lambda/2$ pitched 2-D tiled arrays.

sub-THz beamformer module where a CMOS beamformer IC and an InP transceiver front-end IC are co-integrated, as shown in Fig. 3 [4], [23]. A CMOS beamformer IC can offer precise RF phased array signal processing such as phase and gain control [24], [25] and complex calibration and fast beam steering [26] within a compact chip area due to its integration capability. However, the TX output power, efficiency, and RX noise performance of a CMOS RFIC are limited at frequencies above 100 GHz due to the limited f_{max} and breakdown voltage (e.g., $f_{max} \simeq 300$ GHz and $BV_{dss} \simeq 2.2$ V for GF's 45RFSOI [27]). To overcome the limitation of silicon RFICs, InP front-end ICs with significantly higher f_{max} and breakdown voltage (e.g., $f_{max} \simeq 650$ GHz and $BV_{CEO} \simeq 4.5$ V for Teledyne's 250-nm InP technology) can be co-integrated [4], [28]. The co-integration of InP TRX front-end ICs relaxes the required TX output power and RX NF of the CMOS beamformer IC. For an AiP platform of the heterogeneously integrated sub-THz beamformer module, the vertical stacking of CMOS beamformer ICs, InP front-end ICs, and antenna arrays must be explored for tiled 2-D arrays, as shown in Fig. 3(b) [29]. Therefore, sub-THz CMOS beamformer ICs that fit within a $\lambda/2$ lattice are critical, which calls for developing a compact transceiver based on a bidirectional amplifier.

III. Proposed Bidirectional Amplifier Design Methodology

The proposed bidirectional amplifier is based on the source–drain symmetry of MOSFETs in a common-gate amplifier, as shown in Fig. 4. The relative potential between P1 and P2 determines the source and drain for forward

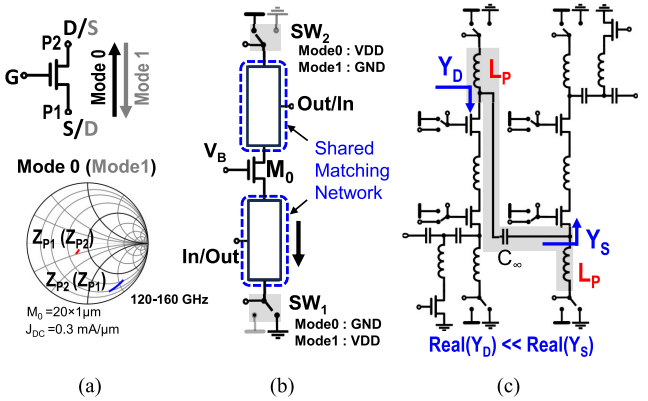


Fig. 4. (a) Source–drain symmetry of a CMOS common-gate amplifier, (b) challenges of bidirectional impedance matching using shared passive networks due to a large impedance difference between source and drain terminals, and (c) interstage matching network used in [22], which does not meet the conjugate matching condition.

signal amplification (Mode 0) and reverse signal amplification (Mode 1). It is found that a common-gate amplifier can be stabilized with the intrinsic loss of a passive matching network in our D-band design prototype, which allows using a single-ended amplifier topology. The single-ended topology reduces DC power consumption compared to a differential amplifier that uses neutralization capacitors for stabilization. In addition, a common-gate amplifier provides a wide input return loss bandwidth [30] due to the intrinsic real impedance from the source terminal. A common-gate bidirectional amplifier was previously explored in a GaAs technology [31] and more recently in a CMOS technology [22] below 30 GHz by implementing a shared matching network and power supply/ground switches. However, the interstage matching network implemented in [22] does not meet the conjugate matching condition, significantly limiting the maximum achievable gain. As shown in Fig. 4(c), the interstage matching network is formed with two parallel identical shunt inductors, L_P, to resonate the device capacitance out at the operation frequency. However, the drain conductance from the first stage is still largely different from the source conductance from the second stage, causing a substantial impedance mismatch. As a result, the measured gain for the two-stage bidirectional amplifier was only 9.5 dB at 28 GHz with a DC power consumption of 30 mW [22].

To address these challenges, we propose a new design methodology of a bidirectional common-gate amplifier, as shown in Fig. 5. The proposed design methodology achieves the conjugate matching condition for an interstage matching network, as well as input and output matching networks in both forward and reverse signal directions. A current-reuse technique is proposed to reduce DC power consumption and chip area by sharing the same supply current between the adjacent stages. The design procedure of the proposed bidirectional amplifier is summarized as follows.

1) *Symmetric Interstage Matching Network Design:* A low-loss interstage matching network is critical since several gain stages must be cascaded at frequencies above 100 GHz due to the limited MAG per stage. For the design of a symmetric interstage matching network, a common series component, Z_{CM}, shared by input and output matching networks of a common-gate amplifier is selected, as shown in Fig. 5(a). Adding Z_{CM} in series transforms the source and drain impedances, Z_S and Z_D, to have the same conductance. Then, Z_1 and Z_2 are selected to resonate the remaining susceptance on the source and drain sides after adding Z_{CM}, respectively. The selected Z_{CM}, Z_1, and Z_2 form a symmetric interstage matching network for cascaded common-gate amplifiers, as shown in Fig. 5(b), since Z_1 and Z_2 are in parallel and Z_{CM} is shared for both signal directions. Power supply and ground switches are placed at the top and bottom of each amplifier stage to swap the source and drain terminals depending on the signal direction. The proposed symmetric passive network achieves interstage conjugate matching conditions for forward and reverse signal paths without lossy switches on the RF signal path.
2) *Tunable Input/Output Matching Network Design:* Input and output matching network designs are completed by adding a common switched shunt component, Z_T, as shown in Fig. 5(c). Z_2 at the last stage (rightmost) is replaced with Z_1 for bidirectional symmetry. Z_T in parallel with Z_1 provides an equivalent impedance to Z_2 for output matching. Regardless of the number of amplifier stages, the switched shunt components are used only at the input and output to minimize the additional loss.
3) *Current Reuse Topology:* To reduce the power consumption, a current-reuse technique is applied, as shown in Fig. 5(d). Power and ground connections are removed from Z_2 at the first stage and Z_1 at the second stage, and Z_1 and Z_2 are replaced with a single equivalent shunt component $Z_P = Z_1||Z_2$ in series with a DC-blocking capacitor. A switchable biasing network is added, connecting the cascode transistor gate to VDD. The current-reuse topology allows sharing the same supply current between the adjacent stages, significantly reducing DC power consumption.

IV. Circuit Implementation

Based on the proposed design methodology, two prototype D-band amplifiers using transformers and transmission lines for symmetric interstage matching networks are implemented using the GlobalFoundries 45-nm RFSOI process. In the following design process and simulations, the RC extracted view of a common-gate transistor and via inductance modeled with HFSS, an electromagnetic (EM) simulator, are used, as shown in Fig. 6(a). The RC extracted view includes two vertical natural capacitors (VNCAPs) connected to the gate using the lowest metal layer to minimize gate inductance. The transistor model is verified with the measured input and output impedance of a standalone common-gate transistor breakout, as shown in Fig. 6(b). Using this common-gate transistor model, the simulated MAG and maximum stable gain (MSG) are very close between forward and reverse modes, validating

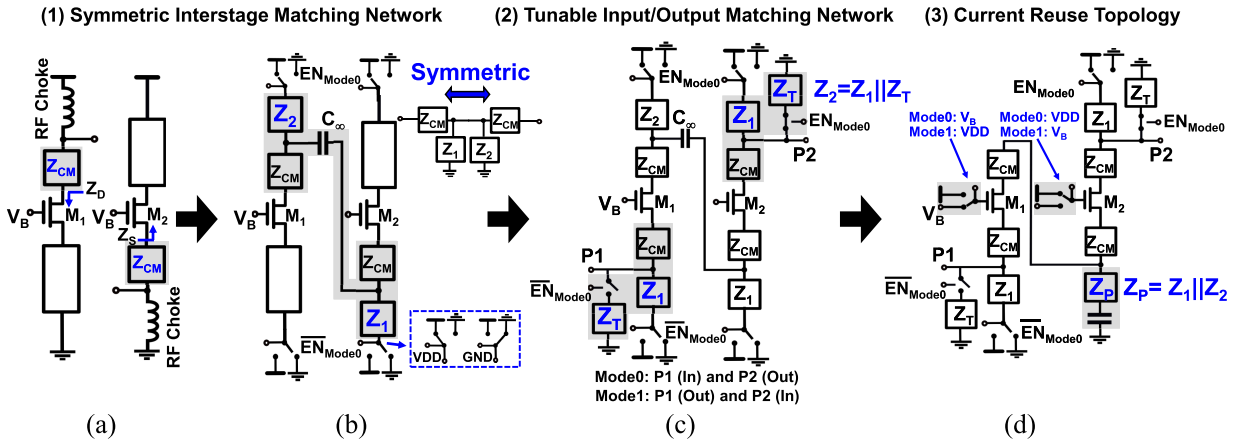


Fig. 5. Proposed bidirectional amplifier design methodology with (a) selecting a common series component Z_{CM} to transform Z_S and Z_D to have the same conductance, (b) achieving symmetric interstage matching networks formed with Z_{CM}, Z_1 and Z_2, (c) adding a tunable component Z_T to the input and output ports to complete input and output matching networks, and (d) applying current reuse topology to share the same supply current between the adjacent stages for low power consumption.

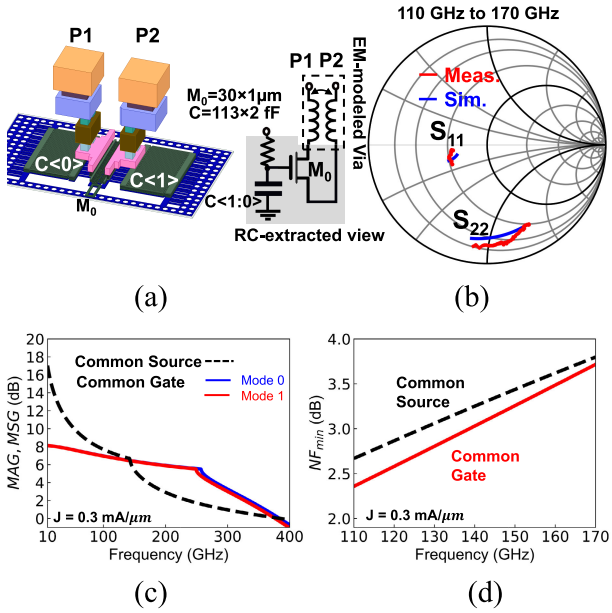


Fig. 6. (a) Three-dimensional layout view of a common-gate transistor and its modeling based on RC-extracted view and EM-modeled vias, (b) simulated and measured input and output impedance of the common-gate transistor using a transistor breakout, (c) simulated MAG and MSG for forward and reverse modes, and (d) simulated minimum achievable NF.

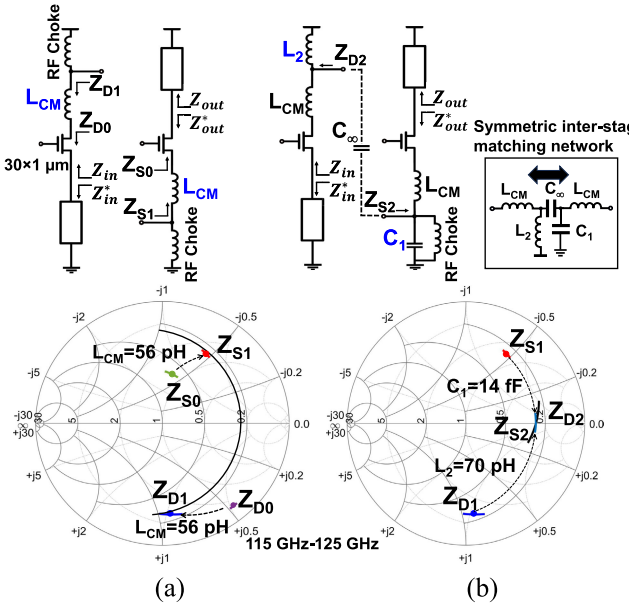


Fig. 7. Implementation example of the proposed interstage matching network design using inductors and capacitors. (a) L_{CM} is selected to transform Z_{D0} and Z_{S0} to Z_{D1} and Z_{S1} on the same conductance circle on the Smith chart. (b) L_2 and C_1 are added to resonate the remaining imaginary part of the admittance.

the symmetry of the device layout, as shown in Fig. 6(c). The minimum achievable NF of the common-gate transistor is comparable to that of a common-source transistor with a current density of 0.3 mA/μm, as shown in Fig. 6(d).

A. 120-GHz Transformer-Based Bidirectional Amplifier

Fig. 7 illustrates an implementation example of the proposed interstage matching network using inductors and capacitors. The impedance looking into the drain terminal of the first stage, Z_{D0}, must be transformed for conjugate-matching to the impedance looking into the source terminal of the second stage, Z_{S0}. Note that the imaginary part of the source impedance, Z_{S0}, is positive. For a standalone common-gate transistor, the imaginary part of the source and drain impedance is negative due to device and parasitic capacitance, as shown in Fig. 6(b). However, when the drain impedance, Z_{out}, contributes to the source impedance through drain–source coupling capacitance, the imaginary part of Z_{S0} can be positive as shown in the Smith chart of Fig. 7(a). For the design of a symmetric interstage matching network, we first need to find a common series inductor L_{CM} to move Z_{D0} and Z_{S0} to the same constant conductance circle (Z_{D1} and Z_{S1}) on the Smith chart. Then, shunt components, L_2 and C_1, are added to resonate out the imaginary part of Z_{D1} and Z_{S1} to complete impedance matching, respectively. As shown in the inset of Fig. 7, the designed interstage matching network is symmetric for both directions since L_2 and C_1 can be swapped in a

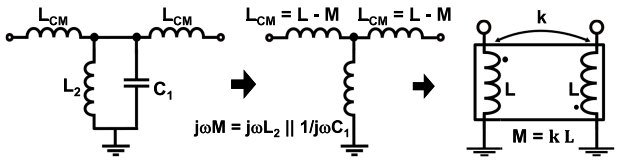


Fig. 8. Proposed inductor-based interstage matching network is transformed into a single transformer for a compact chip area.

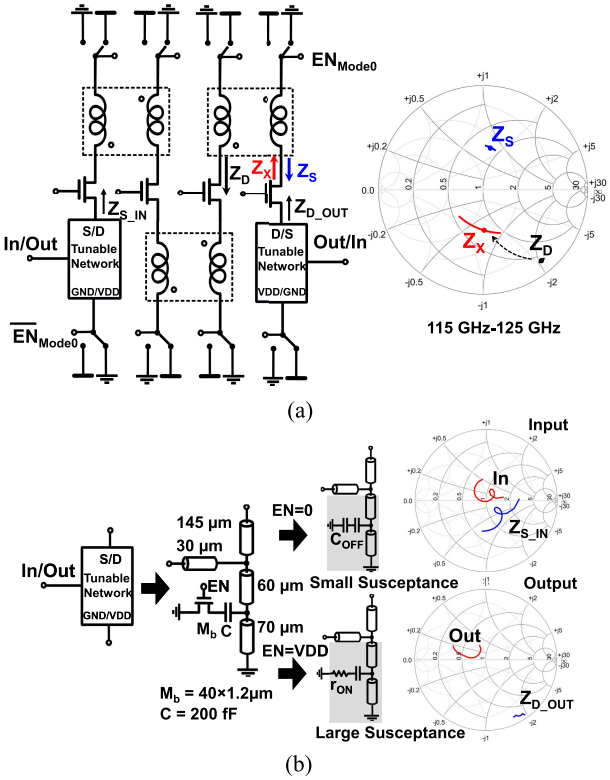


Fig. 9. (a) Impedance matching through the designed transformer-based interstage matching network. (b) Input and output matching networks implemented with a common tunable component.

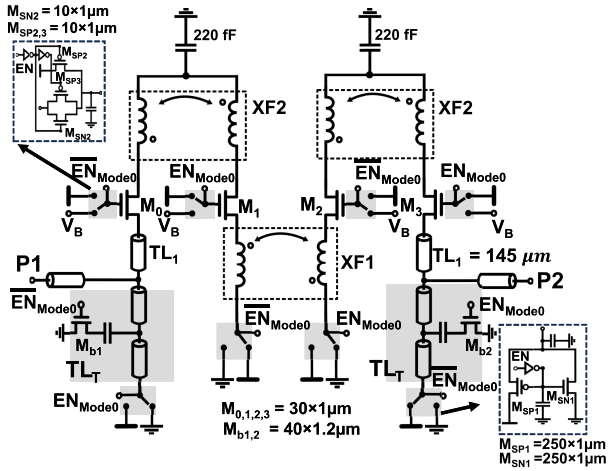


Fig. 10. Two-stage 120-GHz current-reuse transformer-based bidirectional amplifier.

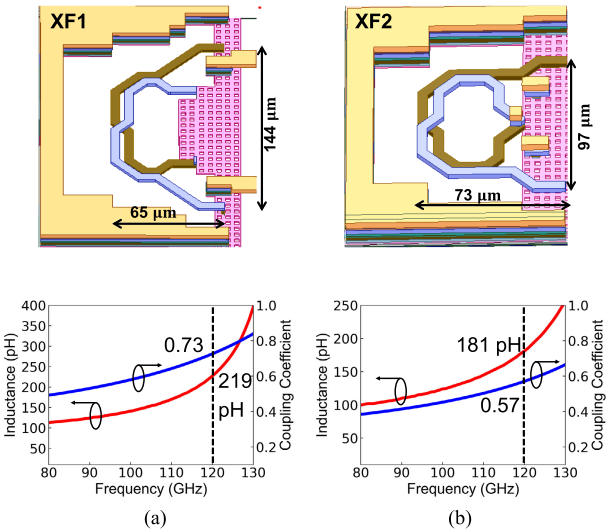


Fig. 11. Interstage transformer design and simulated self-inductance and coupling factor of (a) XF1 and (b) XF2.

parallel combination, and the same series inductor is used on both ends.

To reduce the chip area occupied by inductors in the interstage matching network, three inductors (two L_{CM}s and one L_2) and a capacitor (C_1) can be implemented using a single transformer, as shown in Fig. 8. The designed interstage matching network can be transformed to a T network equivalent to a transformer, where a mutual inductor, M, provides an equivalent impedance at the design frequency to the parallel combination of shunt capacitor, C_1, and inductor, L_2. The transformer's self-inductance L and coupling factor k are selected based on M and L_{CM}. Fig. 9(a) shows how the drain impedance, Z_D, is transformed to Z_X close to the conjugate of the source impedance, Z_S at the following stage, on the Smith chart. The input and output matching networks are completed with a common tunable network formed with transmission lines and a switched capacitor, as shown in Fig. 9(b). The switch is turned off (EN = 0) for the shunt component to provide negligible susceptance for input matching. For output matching, the ON-state switch (EN = VDD) shortens the effective length of the shunt transmission line for larger susceptance.

Fig. 10 shows the schematic of the designed 120-GHz transformer-based bidirectional amplifier. The proposed current reuse technique described in Fig. 5(d) is applied to reduce power consumption. The XF1 and XF2 transformers are designed using OA and OB metal layers and simulated using EMX, as shown in Fig. 11. The self-inductance values and coupling coefficients of XF1 and XF2 are shown in Fig. 11. The self-inductance value and coupling coefficient of XF2 are adjusted by considering parasitic inductance from the bypass capacitor placed in the middle. The quality factors of XF1 and XF2 are greater than 30 within the 3-dB bandwidth of the designed amplifier. The simulated self-resonance frequencies are around 140 and 148 GHz for XF1 and XF2, respectively. The DC blocking capacitors are implemented with a high-Q metal–insulator–metal capacitor (MIMCAP), and the bypass capacitors at the gate of the common-gate transistors and the switched capacitor of the input and output matching

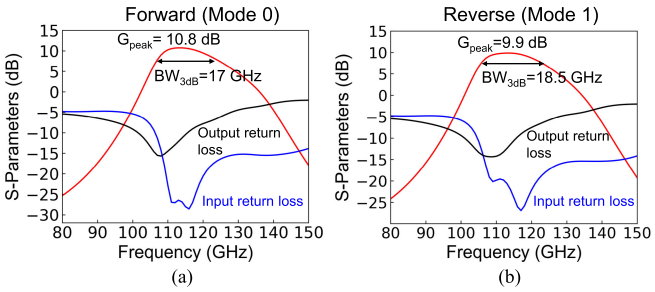


Fig. 12. Simulated S-parameters of the transformer-based 120-GHz bidirectional amplifier for (a) forward and (b) reverse modes.

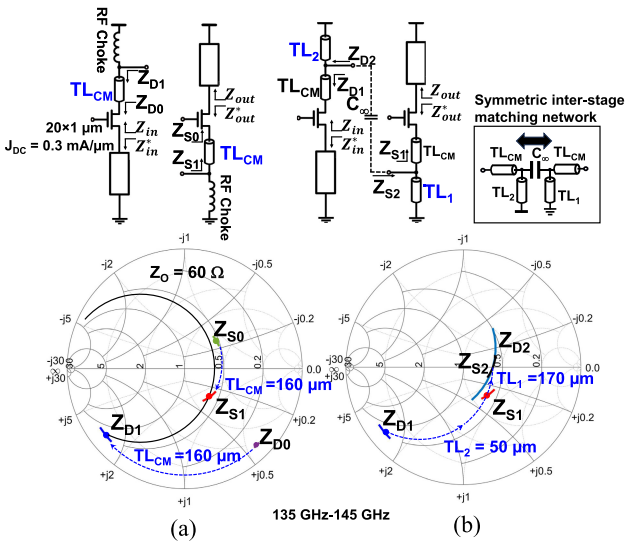


Fig. 13. Implementation example of the proposed interstage matching network design using transmission lines. (a) TL_{CM} is selected to transform Z_{D0} and Z_{S0} to Z_{D1} and Z_{S1} on the same conductance circle on the Smith chart. (b) TL_1 and TL_2 are added to resonate the remaining imaginary part of the admittance.

networks are implemented with a VNCAP to minimize parasitic inductance. The transmission lines are implemented with a ground-shielded co-planar waveguide. The pad capacitance is absorbed as a part of the matching networks. Fig. 12 shows the simulated S-parameters for the forward and reverse amplification modes (Mode 0 and Mode 1). The simulated peak gain in the forward mode is 10.8 dB at 114 GHz with a 3-dB bandwidth of 17 GHz, whereas, in the reverse mode, the peak gain is 9.9 dB at 114 GHz with a 3-dB bandwidth of 18.5 GHz. The 0.9-dB difference in the peak gain results from the asymmetry between the two ports of the transformers implemented using two different metal layers. The simulated OP1dB and OIP3 vary from −4.6 to −3.6 dBm and from 4.3 to 7.5 dBm, respectively, over the 3-dB gain bandwidth.

B. 140-GHz Transmission Line-Based Bidirectional Amplifier

A 140-GHz transmission line-based bidirectional amplifier is implemented using the proposed design concept. Fig. 13 shows an implementation example of the proposed interstage matching network using transmission lines. For the design of the symmetric interstage matching network, a common series transmission line, TL_{CM}, is selected to move Z_{S0} and

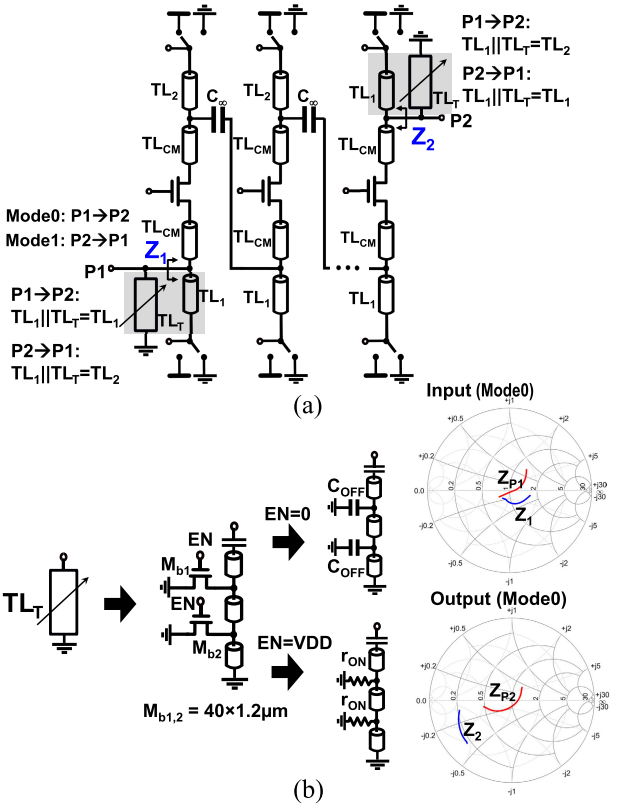
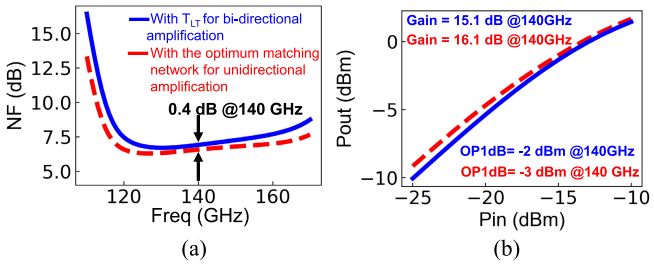


Fig. 14. (a) Reconfigurable input and output matching networks using a tunable transmission line TL_T and (b) tunable transmission line design and OFF/ON-state operation for input and output matching.

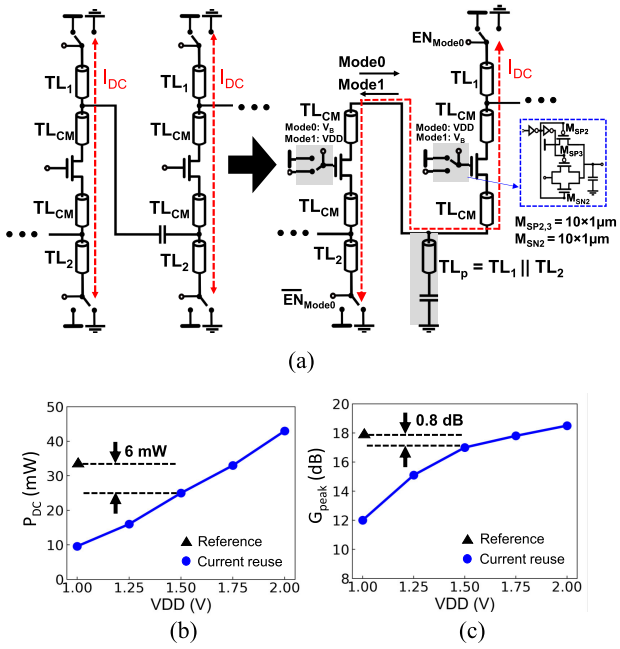
Z_{D0} to the same constant conductance circle (Z_{S1} and Z_{D1}) on the Smith chart by choosing the appropriate characteristic impedance and lengths. Then, shunt transmission lines, TL_1 and TL_2, are added to resonate out the imaginary part of Z_{S1} and Z_{D1}, respectively. As shown in the inset of Fig. 13, the designed interstage matching network is symmetric for both directions since TL_1 and TL_2 in a parallel combination can be swapped, and the common series transmission lines, TL_{CM}, are used.

To complete the input and output matching networks, a tunable transmission line, TL_T, formed with a transmission line loaded by switched capacitors, is added at the input and output ports, as shown in Fig. 14. Note that TL_2 of the rightmost stage is replaced with TL_1 to ensure the symmetry. When the switches of TL_T are in the OFF-state for input matching, TL_T exhibits a high impedance as the effective electrical length is close to $\lambda/4$ with a short-circuited termination. When the switches of TL_T are in the ON-state for output matching, the effective length is shortened to adjust the combined impedance of TL_T and TL_1 to the impedance of TL_2. As illustrated in Fig. 14(b), this design achieves simultaneous input and output matching while maintaining bidirectional symmetry. The effect of the loss of the switched transmission line on the overall performance is evaluated, as shown in Fig. 15. Compared to switchless input and output matching networks designed for unidirectional amplification, the proposed bidirectional matching network degrades the NF and gain only by 0.4 and 1 dB, respectively.



(a) (b)

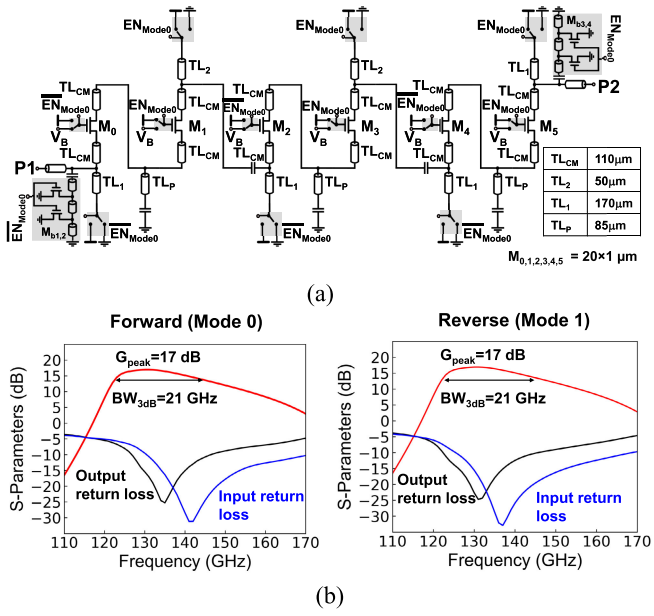
Fig. 15. Simulated performance degradation in (a) NF and (b) linearity due to the loss of the tunable transmission lines compared to the optimum input and output matching networks for unidirectional amplification.



(a) (b) (c)

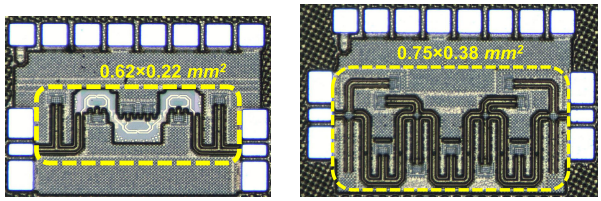
Fig. 16. (a) Current-reuse bidirectional amplifier to share the same supply current between the adjacent stages for low power consumption. Simulated (b) DC power consumption and (c) peak gain of the three-stage current-reuse bidirectional amplifier for different VDDs compared to the six-stage bidirectional amplifier with VDD of 1.0 V and no current reuse.

The proposed current reuse technique is applied to the transmission line-based bidirectional amplifier, as shown in Fig. 16(a). TL_2 at the first stage and TL_1 at the second stage are combined in parallel into a single transmission line, TL_P, to present an equivalent impedance at the design frequency with a compact chip area. Power and ground connections are removed from TL_1 and TL_2, and a DC-blocking capacitor is placed in series with TL_P. A switchable biasing network is added to connect the gate terminal of the cascode transistor to VDD. Fig. 16(b) and (c) shows the simulated DC power consumption and peak gain of the three-stage current-reuse bidirectional amplifier for different VDDs compared to a six-stage bidirectional amplifier with a VDD of 1.0 V and no current reuse. When a VDD of 1.5 V is chosen for the current reuse topology, the peak gain decreases only by 0.8 dB with 20% lower DC power consumption. Fig. 17(a) shows the designed three-stage 140-GHz transmission line-based bidirectional amplifier. Fig. 17(b) shows the simulated S-parameters for forward and reverse amplification modes (Mode 0 and



(a) (b)

Fig. 17. (a) Schematic of the 140-GHz transmission line-based bidirectional amplifier and (b) simulation results.



(a) (b)

Fig. 18. Chip die photo of (a) 120-GHz transformer-based bidirectional amplifier and (b) 140-GHz transmission line-based bidirectional amplifier fabricated in the GlobalFoundries 45-nm RFSOI process.

Mode 1). The simulated peak gain is 17 dB at 132 GHz with a 3-dB bandwidth of 21 GHz in both forward and reverse modes. The simulated OP1dB and OIP3 vary from −2.7 to −1.7 dBm and from 5.7 to 8.4 dBm, respectively, over the 3-dB gain bandwidth.

V. Measurement

The prototype transformer and transmission line-based bidirectional amplifiers were fabricated in the GlobalFoundries 45-nm RFSOI process with the core chip areas of 0.13 and 0.28 mm^2, respectively, as shown in Fig. 18. The total DC currents are 17 and 19 mA for the transformer- and transmission line-based designs, respectively, with a nominal 1.5-V power supply. The fabricated bidirectional amplifiers are characterized on a probe station using Keysight N5242B PNA-X, 5292A mmWave test controller, N5295AX03 120-GHz frequency extender, and N5262BW06 D-band VNAX modules. Input power levels applied to the IC from the VNAX module are calibrated with a VDI-Erickson PM5B power meter.

The measured S-parameters for forward and reverse amplification modes (Mode 0 and Mode 1) compared to the simulation are shown in Figs. 19 and 20 for the transformer- and transmission line-based designs, respectively.

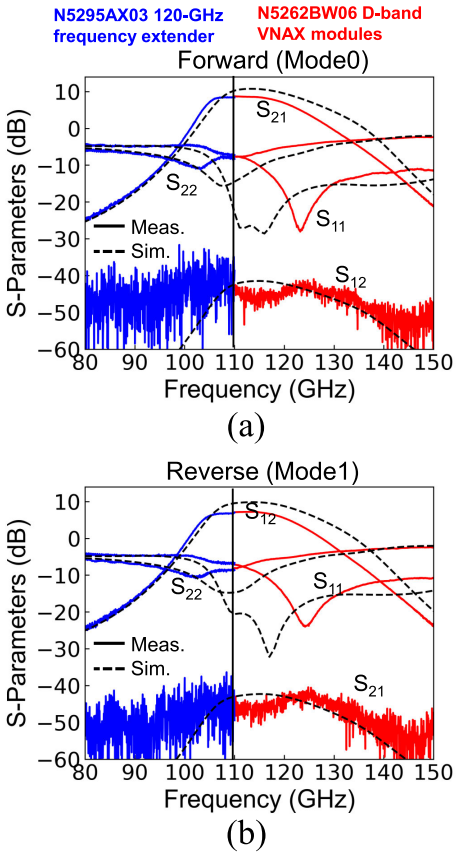


Fig. 19. Measured and simulated S-parameters (a) forward amplification (Mode 0) and (b) reverse amplification (Mode 1) for the transformer-based bidirectional amplifier.

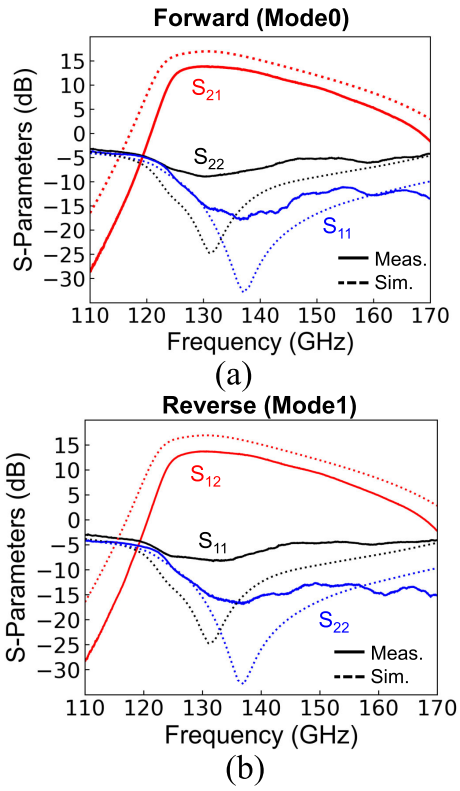


Fig. 20. Measured and simulated S-parameters (a) forward amplification (Mode 0) and (b) reverse amplification (Mode 1) for the transmission line-based bidirectional amplifier.

The transformer-based design reports a measured peak gain of 9 dB in forward amplification mode and 7.5 dB in reverse amplification mode at 110 GHz with a 3-dB bandwidth of 20 GHz, which agrees with the simulations. The measured peak gain for the transmission line-based design is 14 dB at 130 GHz with a 3-dB bandwidth of 21 GHz in forward and reverse modes. For both transformer- and transmission line-based designs, the measured input return loss is higher than 10 dB over >40 GHz. The measured output return loss for the transmission line-based design has a relatively large discrepancy from the simulation results. The potential source of this discrepancy is an inaccurate EM modeling of the ON-state tunable transmission line. To investigate this further, Fig. 21(a) shows the inductance modeling of interconnects (including vias) between the decoupling capacitor (implemented with a MIMCAP) and the tunable transmission line. In the design process, $L_{\text{par1}} + L_{\text{par2}}$ of 12 pH is used based on a one-port MIMCAP breakout measurement. However, as shown in the 3-D layout view, a large junction on the top plate of the MIMCAP formed by TL_1, TL_{CM}, and $\text{TL}_{\text{out/in}}$ makes accurate EM modeling challenging. We hypothesized that the junction might reduce $L_{\text{par1}} + L_{\text{par2}}$. The effect of the reduced inductance on the output impedance and gain is shown in Fig. 21(b). As the inductance is reduced, the simulated output impedance is closer to the measured one on the Smith Chart, and the simulated gain is also reduced,

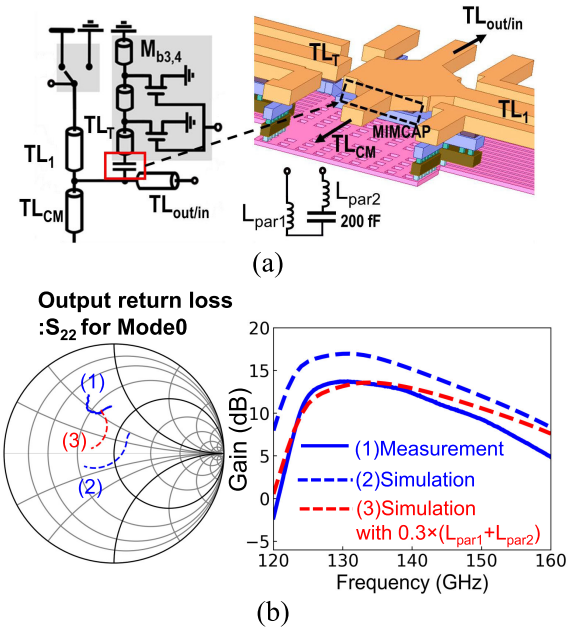


Fig. 21. (a) Inductance modeling of interconnects between the decoupling capacitor and tunable transmission line and (b) effect of the parasitic inductance on output impedance and gain compared to the measurement.

which validates the hypothesis. The transmission line-based design demonstrates identical S-parameters for the forward and reverse amplification modes. On the other hand, the transformer-based design exhibits a 1.5-dB difference in the measured peak gain between forward and reverse amplification

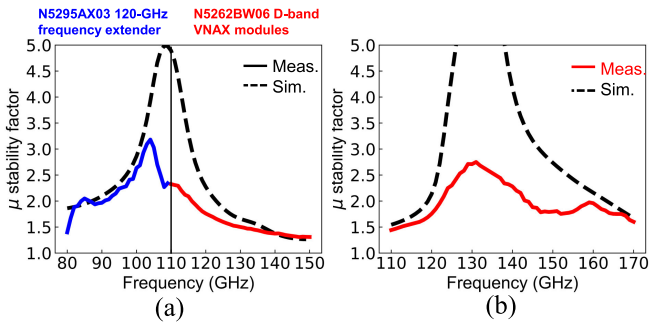


Fig. 22. Measured stability factor μ of (a) transformer- and (b) transmission line-based bidirectional amplifiers.

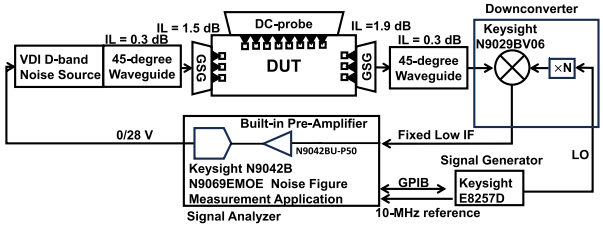


Fig. 23. Block diagram of the NF measurement setup.

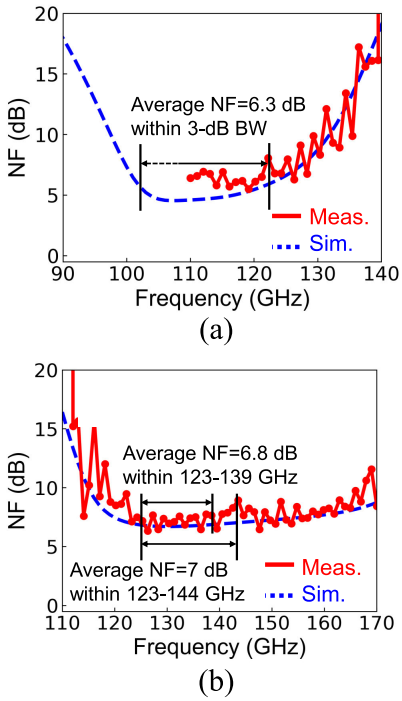


Fig. 24. Measured NF of (a) transformer-based design and (b) transmission line-based design.

modes. The stability of the two amplifiers is measured with μ factor, as shown in Fig. 22. The measured μ factor is greater than unity for both designs, validating that they are unconditionally stable.

The NF is measured based on the Y-factor method using a VDI WR6.5NS D-band noise source, Keysight N9029BV06 D-band SAX module, and Keysight N9042B signal analyzer using the experimental setup, as shown in Fig. 23. Fig. 24 shows the measured NF of the transformer- and transmission

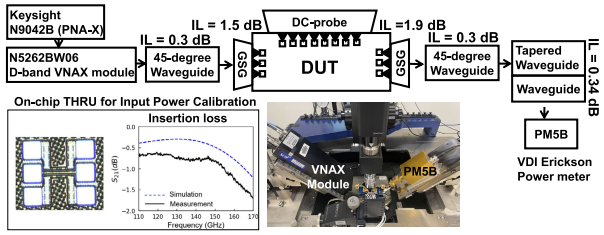


Fig. 25. Linearity measurement setup.

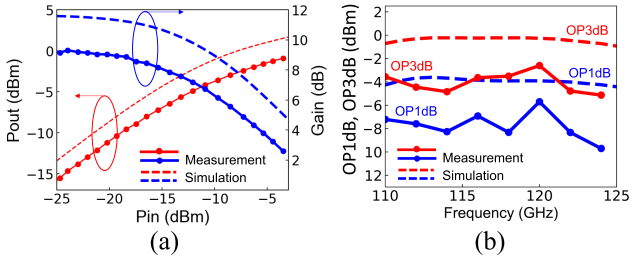


Fig. 26. Measured linearity of the transformer-based design with (a) large-signal response at 110 GHz and (b) OP1dB and OP3dB across frequency.

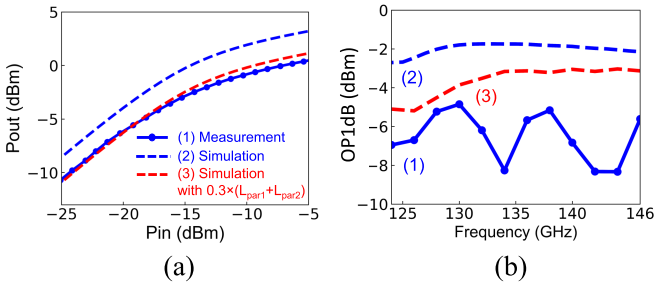


Fig. 27. Measured linearity of the transmission line-based design with (a) large-signal response at 130 GHz and (b) OP1dB across frequency.

line-based designs. The measured average NF values of the transformer- and transmission line-based designs within the 3-dB gain bandwidth are 6.3 and 7 dB, respectively, in good agreement with the simulation.

The linearity of the amplifiers is measured using the experimental setup, as shown in Fig. 25. The input signal is generated from a Keysight N5242B PNA-X and N5262BW06 D-band VNAX module. The output power is measured using a VDI-Erickson PM5B power meter. The input power applied to the amplifiers is measured using an on-chip thru in the same setup. Fig. 26 shows the measured linearity of the transformer-based design with output power levels and gains for different input power levels at 110 GHz [see Fig. 26(a)] and OP1dB and OP3dB over the 3-dB bandwidth [see Fig. 26(b)]. The measured OP1dB and OP3dB vary from -9.7 to -5.7 dBm and from -5.1 to -2.6 dBm, respectively, at frequencies from 110 to 124 GHz. Fig. 27 shows the measured linearity of the transmission-line-based design. The OP1dB and OP3dB vary from -8.3 to -5.1 dBm and from -4.6 to -2.1 dBm, respectively, at frequencies from 124 to 146 GHz. To investigate the linearity degradation in the measurement, OP1dB is also simulated with a reduced inductance associated with the decoupling capacitor

TABLE I
PERFORMANCE SUMMARY IN COMPARISON TO STATE-OF-THE-ART MMWAVE BIDIRECTIONAL AMPLIFIERS AND STANDALONE D-BAND LNA

References	**This Work**		[18]	[15]	[13]	[12]	[22]	[32]	[33]	[34]	[35]
Freq.(GHz)	**124-145**	**103-123**	77-90	52-67	52-67	57-65	24-32	125.5-157	143-166	146-157	147-157
Type	**Bidirectional Amplifier**							**Low-noise amplifier**			
Gain (dB)	**14**	**9**	16	11.3	16.1	22	9.5	16	15.7	18	17.9
Gain BW(GHz)	**21**	**20**	14.5	15	15	8	8*	31.5	23	11	10
NF (dB)	**7**	**6.3**	10.9	6.9 (sim)	7.1 (sim)	5.4	7.4	8	8.5	7.9	6 (avg)*
OP1dB (dBm)	**-5.1 @130GHz**	**-7.2 @110GHz**	N/A	12.8(PA) 2.3*(LNA)	5.1	0 (PA) -9 (LNA)	0.1	0.5	-3	1	-6.9
Input Return Loss BW(GHz)†	**>46**	**>55**	60	9*	8*	8*	10*	10*	25*	18*	15*
DC Power (mW)	**28.5**	**25.5**	65.8	291 (PA) 78 (LNA)	70	55 (PA) 44 (LNA)	30	75	32	27.5	13.7
Area(mm^2)	**0.28**	**0.13**	0.47	0.08	0.067	0.44	0.28	0.07	0.34	0.09	0.13*
Technology	**45nm RFSOI**	**45nm RFSOI**	0.12µm SiGe	40nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	45nm RFSOI	28nm FDSOI	22nm FDSOI	65nm CMOS

*Estimated from the graph †Frequency range where input return loss > 10 dB

of the tunable transmission line discussed in Fig. 21. The decreased OP1dB with the reduced inductance implies that the overestimated inductance might degrade the linearity in the measurement.

The performance of the proposed bidirectional amplifier is summarized in Table I compared to other published symmetric bidirectional mmWave amplifiers and standalone D-band LNAs in silicon [32], [33], [34], [35]. This work demonstrates the first D-band bidirectional amplifier with a higher operation frequency, comparable gain and NF, and lower DC power consumption than previously reported bidirectional amplifiers below 90 GHz. The reported NF is also as low as those of the state-of-the-art D-band LNAs while supporting bidirectional amplification, which shows the effectiveness of the proposed topology. The 3-dB bandwidth of the proposed bidirectional amplifiers is comparable with the existing D-band LNAs in the literature. To improve the bandwidth further, the staggered tuning technique can be applied in designing multistage bidirectional amplifiers, whereby each stage is tuned to a slightly different frequency [36].

VI. CONCLUSION

This work introduced a new design methodology of a common-gate bidirectional amplifier based on symmetric passive networks to minimize the switching loss in support of bidirectional amplification. A current-reuse technique has been proposed to reduce power consumption by sharing the supply current between the adjacent stages. Based on the proposed design methodology, two prototype D-band bidirectional amplifiers have been designed and fabricated in a 45-nm RFSOI process. The transmission line-based bidirectional amplifier reports a peak gain of 14 dB at 130 GHz with a 3-dB bandwidth of 21 GHz, an average NF of 7 dB over the 3-dB bandwidth, and a DC power consumption of 28.5 mW for both forward and reverse amplification modes. The transformer-based bidirectional amplifier demonstrates peak gains of 9 and 7.5 dB at 110 GHz for forward and reverse amplification modes, respectively, with a 3-dB bandwidth of 20 GHz. The transformer-based bidirectional amplifier presents an average NF of 6.3 dB over the 3-dB bandwidth and a DC power consumption of 25.5 mW. The proposed bidirectional amplifier is expected to motivate further development of compact, low-power D-band transceivers for next-generation communications and sensing.

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