A Low-Loss Passive *D*-Band Phase Shifter for Calibration-Free, Precise Phase Control

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***Abstract*— A low-loss passive phase shifter is presented for calibration-free, precise phase control at *D*-band. The proposed topology manipulates time delay by controlling propagation distance in a trombone-like structure formed with two parallel transmission lines periodically connected via switch networks. The proposed phase control exploits only one switched signal transition for all phase states, significantly lowering insertion loss and keeping loss variation small over phase states. A detailed analysis of the design tradeoff between insertion loss and phase resolution is also presented. A prototype 5-bit digital phase shifter that operates with 11.25° steps over 360° tuning range at 140 GHz was implemented using a 45-nm RF silicon-on-insulator (SOI) technology and occupies only 0.04 mm^2. On-wafer measurements report an rms phase error of 1.2° without calibration, which is the lowest among published phase shifters in similar frequency bands. The prototype IC achieved the measured insertion loss of 11.5 ± 0.8 dB and IP1dB of >12.9 dBm with no dc power consumption.**

***Index Terms*— 6G, bi-directional, calibration-free, *D*-band, millimeter-wave (mmWave), passive, phase shifter, phased array.**

I. Introduction

THE abundant spectrum available at millimeter-wave (mmWave) frequency bands can deliver extreme channel capacity for communications and ultrahigh resolution for radar sensing. This motivated the recent deployment of the fifth-generation (5G) mmWave mobile network in the range of 24–40 GHz (FR2) [1], [2], [3] and the commercialization of high-resolution mmWave radar sensors at 60 and 76–81 GHz for industrial and automotive applications [4], [5]. To overcome severe path loss and limited performance of silicon-based Radio Frequency Integrated Circuits (RFICs) at mmWave frequencies, the use of a large-scale phased array transceiver is essential [6].

To accommodate explosively increasing wireless data capacity beyond 5G and emerging sensing applications, the *D*-band frequency spectrum (110–170 GHz) has attracted considerable interest [7]. The very small size of antennas at the *D*-band enables a huge number of antenna elements to be integrated into a massive multiple-input multiple-output (MIMO) array module as shown in Fig. 1. This enables multiple signals to be sent and received simultaneously, dramatically boosting spectral efficiency. However, it also poses a fundamental challenge for the implementation of a large-scale phased array: the area of antenna-in-package (AiP) scales down with λ^2 due to a fixed half-wavelength antenna spacing ($\lambda/2 \approx 1$ mm at 140 GHz) [6]. The resulting small AiP dimensions make *D*-band beamformer IC design difficult, requiring a compact IC area per element, low power consumption for the mitigation of increased heat density, and simple array calibration for orchestrating many front-end elements in real time. In addition, a large-scale phased array with narrow beamwidth requires accurate beam-pointing capability to avoid SNR degradation [8], [9]. These beamformer IC requirements lead to the design of *D*-band phase shifters with the following features as described in Fig. 1. First, bi-directional phase control with a compact chip area is necessary so that TX and RX front-ends can share a single phase shifter. Second, a passive phase shifter with low insertion loss is desirable to reduce power consumption. Finally, calibration-free, accurate phase control and constant insertion loss over phase tuning are required.

Although several *D*-band phase shifters have recently been proposed, none have achieved all of the above-mentioned design requirements. A *D*-band true-time delay type phase shifter based on cascaded switched transmission lines was proposed for a wide-band beamformer, which reported high insertion loss (>20 dB) and nonuniform delay steps [10]. *D*-band vector modulator-based phase shifters were proposed for lower insertion loss at the cost of power consumption, comprehensive calibration, and uni-directional operation [11], [12], [13]. Additionally, hybrid phase shifter topologies were proposed that combine passive and active phase shifters for the compromise of insertion loss and power consumption [14], [15], [16]. However, the hybrid topologies still have similar limitations to the vector modulator approach.

To address the limitations of the prior approaches, we propose a new *D*-band passive phase shifter design, which achieves bi-directional and calibration-free operation with low insertion loss, high phase control accuracy, and compact area. The proposed phase shifter has a simple architecture that can manipulate propagation delay through two parallel transmission lines periodically connected via transistor switch networks. We implemented a prototype phase shifter using the proposed concept, which operates with 11.25° steps over 360° at 140 GHz, in a 45-nm RF silicon-on-insulator (SOI) process. The measured rms phase error

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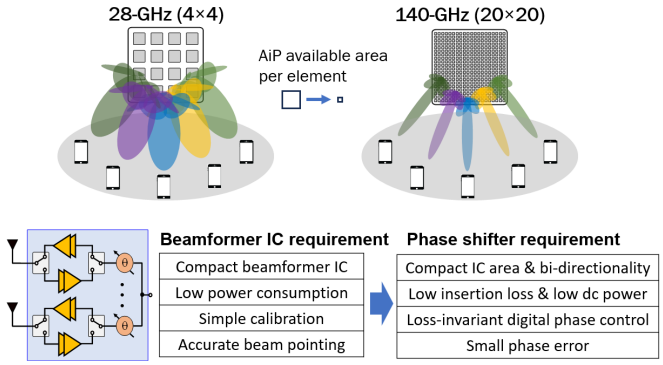


Fig. 1. Phase array AiP scaling from 28 to 140 GHz and the design requirements of a *D*-band beamformer IC and phase shifter.

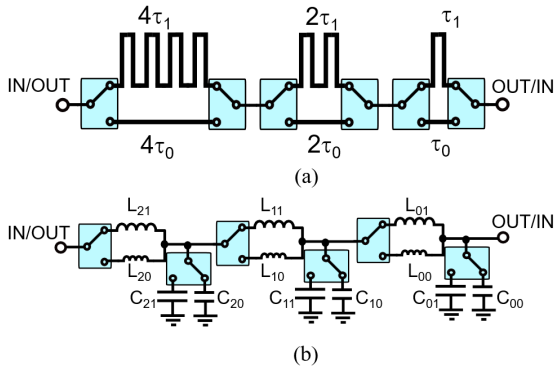


Fig. 2. Prior arts of digitally controlled passive phase shifters using (a) switched transmission lines [10] and (b) switched *L* and *C* [18], [19].

is 1.2° without calibration, which is the lowest among published phase shifters in similar frequency ranges. The measured insertion loss is 11.5 dB with $<$ ±0.8-dB variation. This article presents an extended version of the research work originally presented in [17]. Beyond the brief description reported in the conference article, this article provides: 1) a discussion of *D*-band phase shifter design requirements; 2) theory and circuit implementation details; 3) a discussion of design tradeoffs; and 4) measurements of linearity, rms gain, and phase errors across frequency for multiple IC samples, and performance variation over power supply voltages. This article is organized as follows. Section II discusses the principle of the proposed phase shifter, Section III describes the details of the 45-nm RFSOI IC implementation of the design, Section IV shows on-wafer measurement results, and Section V provides a summary and conclusion.

II. Proposed Phase Shifter Principle

For the implementation of digitally controlled passive phase shifters, multiple switched transmission lines or *L*–*C* sections can be cascaded as shown in Fig. 2. Each stage of the switched transmission line consists of two single-pole double-throw (SPDT) switches and two transmission lines with different lengths as shown in Fig. 2(a) [10]. Each section can be binary-weighted to minimize the number of switches for a given resolution and tuning range. The switched transmission line can be replaced with lumped *L*–*C* sections to reduce the chip area as shown in Fig. 2(b). The phase shift of each section can be tuned by switching only capacitance [20], only

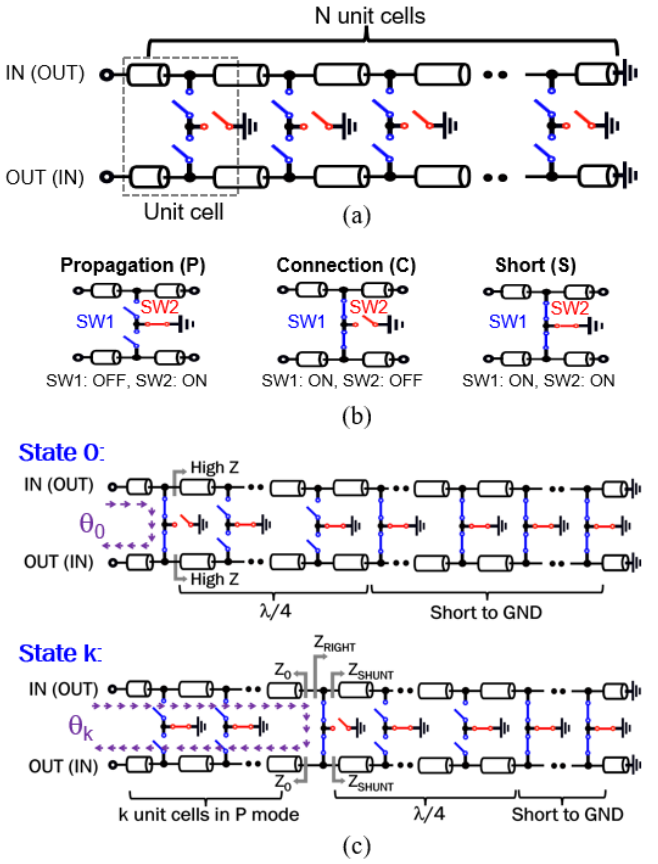


Fig. 3. (a) Proposed phase shifter concept consisting of cascaded *N* unit cells, (b) different configurations of the unit cell, and (c) operation principle of the proposed phase shifter implemented with ideal switches.

inductance [21], or both inductance and capacitance [18], [19], [22]. The phase shift of each section can be binary-weighted or uniform depending on the required area, insertion loss, and phase step uniformity. In these types of passive phase shifters, a signal goes through several switched paths where the number of the switched paths generally increases with phase resolution and tuning range. The switched path loss, which increases with frequency due to the limited $r_{ON}C_{OFF}$ of transistors, is accumulated over stages, significantly increasing the overall insertion loss.

To overcome the fundamental limitation of the prior switched phase shifters, we propose a new phase shifter with only one switched signal transition for all phase states as shown in Fig. 3. It consists of two parallel transmission lines periodically connected via switch networks, which can be considered *N*-cascaded unit cells. Each unit cell is formed with two switches that connect the two parallel transmission lines (SW1) and one shunt switch (SW2) that connects the middle node to the ground. The unit cell can be configured in three different modes for the proposed phase shifter operation: propagation mode, connection mode, and short mode as shown in Fig. 3(b). Fig. 3(c) illustrates the operation principle of the proposed phase shifter when the switches are ideal ($r_{ON} = 0$ and $C_{OFF} = 0$). For the *k*th phase state, an input signal propagates along the upper transmission line formed with *k* unit cells in *propagation* mode until it reaches the one in *connection* mode. Then, the signal is redirected and propagates

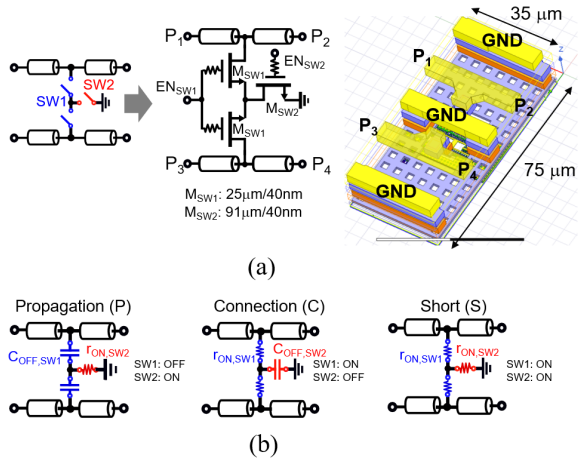


Fig. 4. (a) Schematic and 3-D layout view of the unit cell implemented with NMOS transistors and coplanar waveguides and (b) different configurations of the unit cell with the *RC* models of ON/OFF state transistors.

along the lower transmission line toward the output port in the opposite direction. The total phase shift between the input and output ports is given by $\theta_k = (2k+1)\tau_0 \cdot \omega$, where τ_0 is the propagation delay per unit cell. The phase shift between the input and output ports is programmable by selecting different k with phase steps of $2\tau_0\omega$. To ensure that an input signal travels toward the output port without disruption after the transition, the impedance seen after the unit cell in the connection mode, Z_{SHUNT}, should be ∞ so that the signal sees only the characteristic impedance Z_0 continuously ($Z_{\text{RIGHT}} = Z_0$) from the lower transmission line. To this end, a quarter-wave impedance transformer terminated by a short is formed by: 1) having j unit cells in *propagation* mode after the connection for 90° phase shift at the operation frequency and 2) having the rest of the unit cells in the *short* mode. The proposed phase shifter has only a single unit cell in the *connection* mode for all phase states; the overall insertion loss remains constant across different phase settings, as it is dominated by the transition loss at the unit cell in the *connection* mode (which will be discussed in Section III-C). This feature addresses the tradeoff between insertion loss and phase resolution/tuning range as well as large loss variation across different phase states, as exhibited by prior switch-based passive phase shifters [10].

III. IC Implementation in 45-nm RFSOI Process

We designed a prototype phase shifter based on the proposed topology operating at 140 GHz using a 45-nm RFSOI process. This section discusses the design details of the key building blocks and important design tradeoffs.

A. Unit Cell Design

The proposed phase shifter consists of N cascaded unit cells. Fig. 4 shows the schematic of the unit cell with the 3-D layout view along with the equivalent circuits in three different operation modes. It is designed with NMOS transistors and parallel transmission lines implemented with coplanar waveguides. The transistor switch layout is *RC*-extracted using PVS-QRC, and the surrounding electromagnetic (EM) structure is modeled by EMX. The switch network that connects the two coplanar waveguides is implemented with two transistors (M_{SW1}) in series and one shunt transistor (M_{SW2}) in the middle. M_{SW2} is turned on for the propagation mode as well as the short mode to minimize capacitive coupling between the forward and reverse signal paths through $C_{\text{OFF,SW1}}$. Fig. 5 shows the effect of isolation between the two transmission lines on phase steps and insertion loss for different k by turning on and off M_{SW2} in the propagation mode. The improved isolation with the ON-state M_{SW2} enhances the uniformity of phase steps and insertion loss for different k. The phase shift per unit cell in the propagation mode is given by

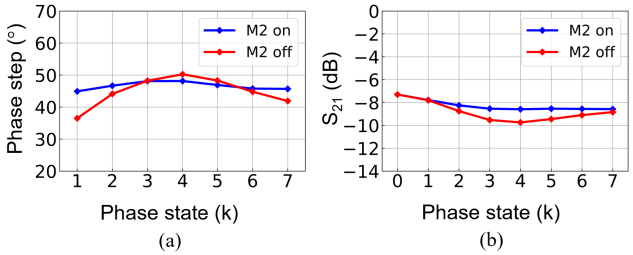


Fig. 5. Simulated effect of improved isolation with M_{SW2} between the two parallel transmission lines on (a) phase steps and (b) insertion loss at 140 GHz.

$$\Delta\theta \simeq \omega\sqrt{L_0(C_0 + C_{\text{OFF,SW1}})} \tag{1}$$

where L_0 and C_0 are the inductance and capacitance of the transmission line per unit cell, respectively, and $C_{\text{OFF,SW1}}$ is the parasitic capacitance of M_{SW1}. The effective characteristic impedance for cascaded unit cells in the propagation mode is given by

$$Z_{0,\text{eff}} = \sqrt{\frac{L_0}{C_0 + C_{\text{OFF,SW1}}}}. \tag{2}$$

For a higher phase resolution (smaller $\Delta\theta$), the size of M_{SW1} needs to be reduced for smaller $C_{\text{OFF},SW1}$, while the reduced size of M_{SW1} increases $r_{\text{ON,SW1}}$, thereby increasing the signal loss at connection and short modes. Based on the tradeoff between the phase resolution and insertion loss, the selected $\Delta\theta$ and $Z_{0,\text{eff}}$ for the prototype IC are 22.5° at 140 GHz for 45° phase steps and 22 Ω, respectively. The detailed optimization of $\Delta\theta$ and $Z_{0,\text{eff}}$ will be discussed in Section III-B.

B. Impedance Matching Condition and Loss at the Transition

For uniform phase steps and low insertion loss over phase settings, signal reflection at the transition where the signal is redirected to the other transmission line needs to be minimized. Fig. 6 illustrates the impedance matching condition ($Z_{\text{RIGHT}} = Z_{0,\text{eff}}$) for the minimum reflection with ideal switches ($r_{\text{ON}} = 0$ and $C_{\text{OFF}} = 0$) and transistor switches, where Z_{RIGHT} is the impedance seen at the transition to the right. With ideal switches, Z_{RIGHT} is equal to the parallel combination of two quarter wavelength transmission lines with the short termination ($Z_{\text{SHUNT}}/2$) and $Z_{0,\text{eff}}$ presented from the lower transmission line. This leads to the impedance matching condition, $Z_{\text{RIGHT}} = Z_{0,\text{eff}}$, since $Z_{\text{SHUNT}} \gg Z_{0,\text{eff}}$. For transistor switches with finite $r_{\text{ON}}C_{\text{OFF}}$, Z_{RIGHT} is determined by $Z_{0,\text{eff}}$, Z_{SHUNT}, $r_{\text{ON,SW1}}$, and $C_{\text{OFF,SW2}}$. For given switch and transmission line dimensions, Z_{RIGHT} can be tuned with Z_{SHUNT} by changing the number of the unit cells in the propagation mode after the connection node, j. Fig. 7 shows the simulated Z_{RIGHT}, Z_{SHUNT}, and transition loss for different j. $j = 2$ is chosen based on the simulated matching condition

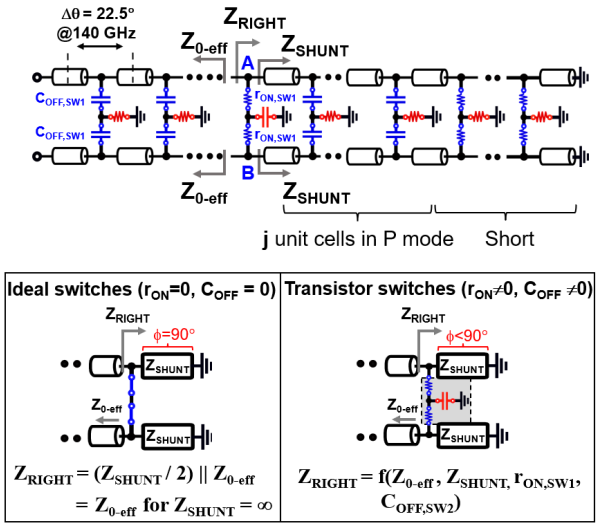


Fig. 6. Impedance matching condition at the transition with ideal switches ($r_{\rm ON} = 0$ and $C_{\rm OFF} = 0$) and transistor switches.

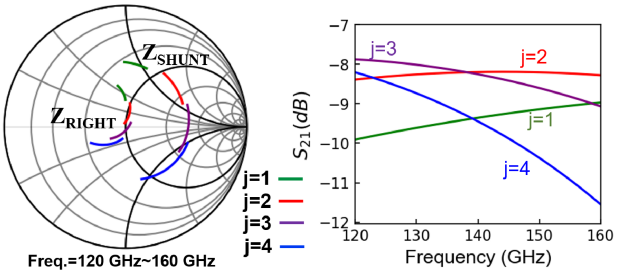


Fig. 7. Impedance matching condition ($Z_{\rm RIGHT} = Z_{0,\rm eff}$) at the connection node with tuning $Z_{\rm SHUNT}$ by selecting the number of the unit cells, **j**, between *Connection* and *Short*.

on the Smith chart, achieving the lowest insertion loss over a wide bandwidth. It is noted that $j = 4$, which meets the quarter wavelength condition for $\Delta\theta = 22.5°$, is not optimal when the switch model based on transistors is taken into account.

Since $r_{\rm ON,SW1}$ is comparable to $Z_{0,\rm eff}$, there is a nonnegligible transition loss determined by the voltage ratio between nodes A and B shown in Fig. 6. The transition loss is approximated by

$$\frac{V_B}{V_A} \simeq \frac{(Z_{0,\rm eff}||Z_{\rm shunt})}{(Z_{0,\rm eff}||Z_{\rm shunt}) + 2r_{\rm ON,SW1}} \tag{3}$$

under the impedance matching condition at the transition.

Fig. 8 shows the calculated insertion loss with respect to the size of $M_{\rm SW1}$ for different $r_{\rm ON}C_{\rm OFF}$ values. We assume that: 1) the size of $M_{\rm SW2}$ is proportional to that of $M_{\rm SW1}$ to keep extra loss due to $C_{\rm OFF,SW2}$ constant; 2) $Z_{\rm SHUNT}$ is properly adjusted for the impedance matching condition; and 3) $\Delta\theta$ is kept to be 22.5° by adjusting L_0 and C_0 of the transmission lines for constant $Z_0 (= \sqrt{L_0/C_0} = 60\ \Omega)$. The calculated insertion loss decreases with a larger size of $M_{\rm SW1}$ and reaches a minimum value beyond a certain size of $M_{\rm SW1}$. The minimum insertion loss is determined by the intrinsic $r_{\rm ON}C_{\rm OFF}$ of transistors given by the process technology. For a 45-nm RFSOI process, $r_{\rm ON}C_{\rm OFF}$ is $\sim$ 180 (fS) for RC-extracted transistors with the minimum channel length. As shown in Fig. 8, smaller $r_{\rm ON}C_{\rm OFF}$ product lowers the transition loss; an advanced process node with a 50% lower $r_{\rm ON}C_{\rm OFF}$ than 45-nm RFSOI process can potentially reduce the insertion loss by 3 dB. For instance, the

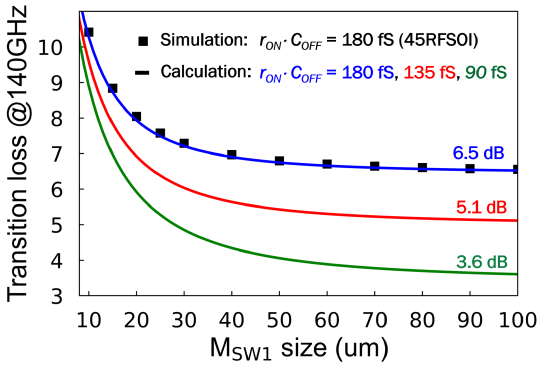


Fig. 8. Calculated and simulated transition loss with respect to $M_{\rm SW1}$ size for different $r_{\rm ON}C_{\rm OFF}$ values.

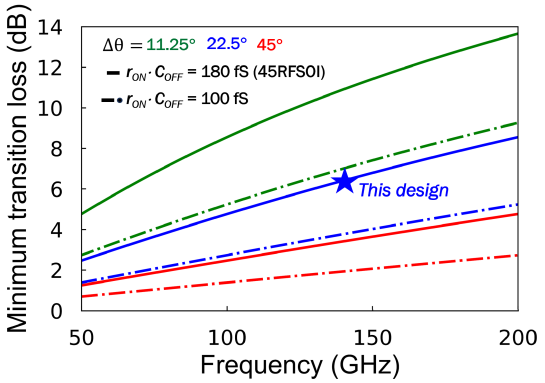


Fig. 9. Calculated minimum transition loss with respect to frequency for different $\Delta\theta$ and $r_{\rm ON}C_{\rm OFF}$ values.

process design kits (PDK) super-low threshold voltage (SLVT) NMOS devices in GF's 22FDX process exhibit an $r_{\rm ON}C_{\rm OFF}$ of $\sim$100 fS [23]. Note that PDK-based simulation results are matched with the calculation closely. Based on (3), the minimum transition loss (the maximum V_B/V_A) with respect to $M_{\rm SW1}$ size is approximately written by

$$\left(\frac{V_B}{V_A}\right)_{\rm MAX} = \frac{1}{\sqrt{1+K^2}+K} \tag{4}$$

where $K = (2\omega r_{\rm ON}C_{\rm OFF})/\Delta\theta$. Equation (4) implies that the minimum achievable transition loss increases with higher frequency and smaller phase steps (higher resolution), while a better process technology with lower $r_{\rm ON}C_{\rm OFF}$ can reduce it. Fig. 9 shows the calculated minimum transition loss with respect to frequency for different $\Delta\theta$ and $r_{\rm ON}C_{\rm OFF}$. The transition loss increases with a smaller $\Delta\theta$, implying the tradeoff between loss and phase resolution. A smaller $\Delta\theta$ reduces L_0 for a given switch size, reducing $Z_{0,\rm eff}$ and increasing the transition loss as implied in (3). For the prototype IC, $\Delta\theta$ of 22.5° is selected.

C. Overall Insertion Loss

As described in Fig. 10(a), the overall insertion loss of the proposed phase shifter is determined by: 1) the insertion loss of the input and output matching networks to transform $Z_{0,\rm eff}$ to 50 Ω; 2) the propagation loss that occurs when a signal propagates over cascaded unit cells in the propagation mode before/after transition; and 3) transition loss discussed in Section III-B. Fig. 10(b) shows the calculated overall insertion loss as well as individual loss contributions with respect to the

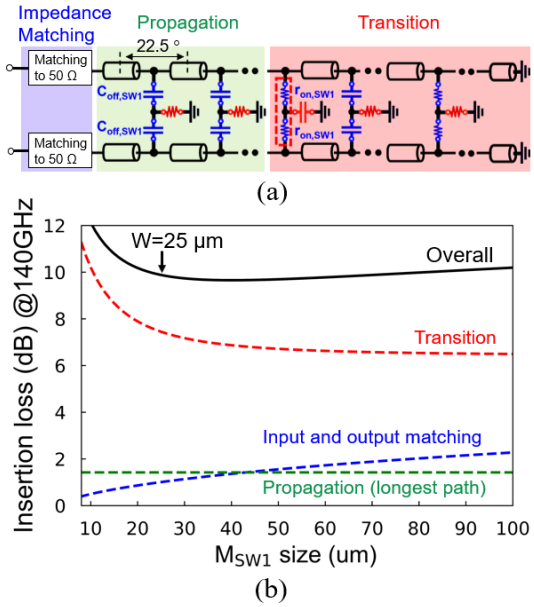
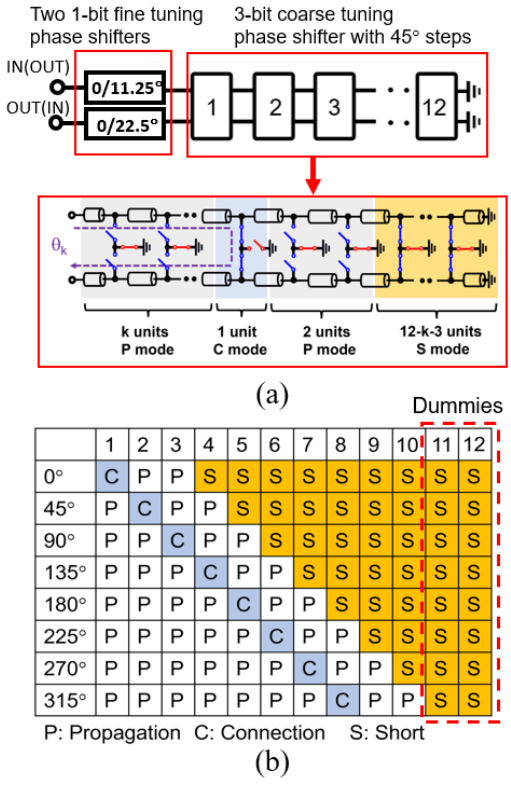


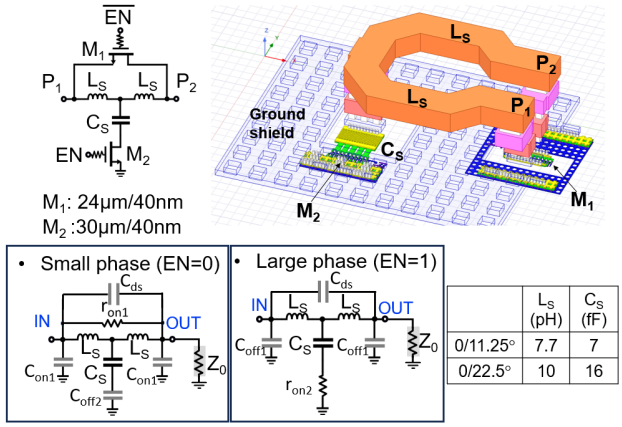
Fig. 10. (a) Overall insertion loss consisting of the losses of impedance matching network, propagation, and transition and (b) calculated overall insertion loss with respect to M_{SW1} size.



	1	2	3	4	5	6	7	8	9	10	11	12
0°	C	P	P	S	S	S	S	S	S	S	S	S
45°	P	C	P	P	S	S	S	S	S	S	S	S
90°	P	P	C	P	P	S	S	S	S	S	S	S
135°	P	P	P	C	P	P	S	S	S	S	S	S
180°	P	P	P	P	C	P	P	S	S	S	S	S
225°	P	P	P	P	P	C	P	P	S	S	S	S
270°	P	P	P	P	P	P	C	P	P	S	S	S
315°	P	P	P	P	P	P	P	C	P	P	S	S

Fig. 11. (a) Block diagram of the 5-bit phase shifter prototype and (b) configuration table of 12 cascaded unit cells to implement 3-bit course tuning phase shifter.

size of M_{SW1}. The overall insertion loss is mainly determined by the transition loss. The insertion loss of the matching networks increases with a larger M_{SW1} size. As the size of M_{SW1} increases, $Z_{0,eff}$ decreases for a given $\Delta\theta$, as L_0 needs to be reduced. The decrease in $Z_{0,eff}$ increases the impedance transformation ratio given by $Q = ((50/Z_{0,eff}) - 1)^{1/2}$ and



	LS (pH)	CS (fF)
0/11.25°	7.7	7
0/22.5°	10	16

Fig. 12. Schematic and 3-D layout view of the 1-bit fine-tuning phase shifters with equivalent circuit models in two different phase settings.

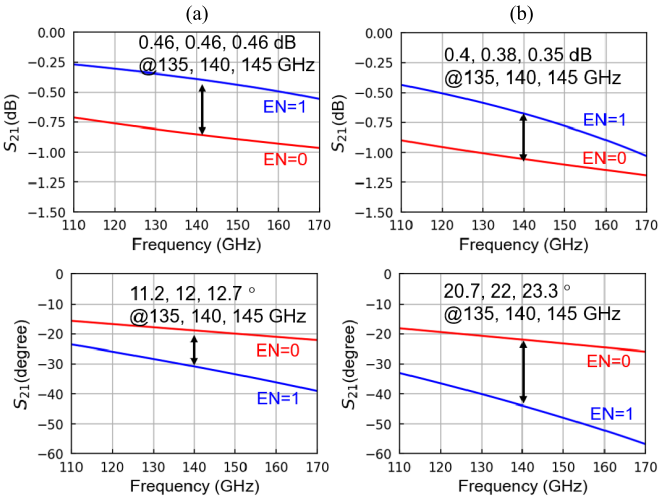


Fig. 13. Simulated phase shift and insertion loss of 1-bit fine tuning phase shifters with phase tuning of (a) 0°/11.25° and (b) 0°/22.5°.

increases the insertion loss of the matching network given by

$$IL = \frac{1}{1+\frac{Q}{Q_L}} \cdot \frac{1}{1+\frac{Q}{Q_C}} \tag{5}$$

where Q_L and Q_C are the quality factors of the inductor and capacitor that form the matching network [24]. For the loss calculation in Fig. 10, Q_L and Q_C are assumed to be 48 and 10 based on the simulation of the PDK components. It is noted that the simulated propagation loss is smaller than 1.4 dB for all phase shift states. Since only the propagation loss among the three loss contributors is dependent on the phase state that corresponds to k in Fig. 3, the variation of the overall insertion loss over phase states is kept low, which is a desirable feature to enable orthogonal phase and gain control in phased array front-ends. Based on: 1) the overall insertion loss in Fig. 10(b) and 2) the minimum inductance that can be reliably designed using a transmission line, the selected size of M_1 is 25 μm for the prototype IC.

D. 5-Bit Digital Phase Shifter Prototype

A 140-GHz prototype phase shifter is designed using 12 cascaded unit cells, which operate with 45° steps ($\Delta\theta = 22.5°$) over 360° tuning range as shown in Fig. 11. As illustrated in

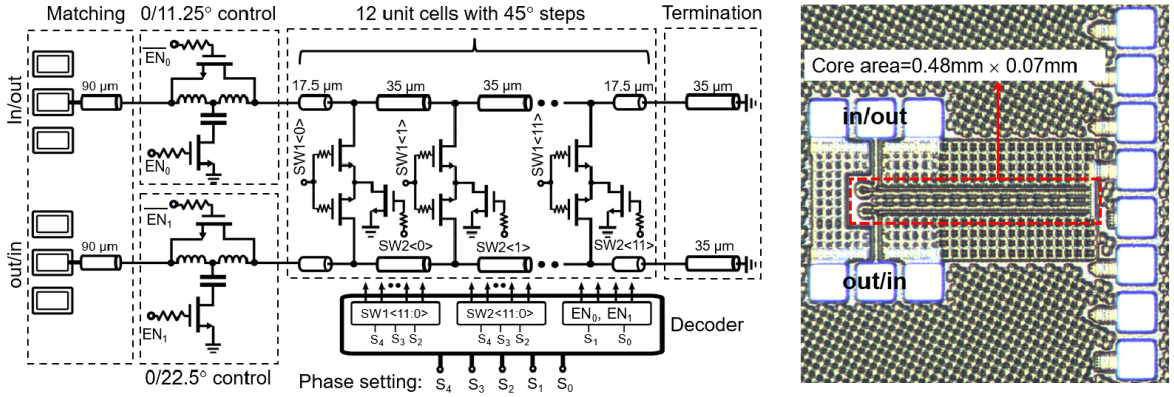


Fig. 14. Schematic and die photograph of the proposed phase shifter.

the configuration table, for each phase state, two unit cells are set to the propagation mode after the unit cell in the connection mode, and the rest of the unit cells are set to the short mode. Two dummies are added at the end to provide consistent Z_{SHUNT} for uniform phase steps and insertion loss. To improve the phase resolution to 11.25°, two 1-bit fine-tuning phase shifters based on a switched L–C topology are added to complete a 5-bit digital phase shifter. The schematic of the fine-tuning phase shifters with a 3-D layout view is shown in Fig. 12. The schematics for 0°/11.25° and 0°/22.5° phase shifters are identical with different L and C values with a 25-Ω interface as shown in the table. The capacitor is implemented with a vertical natural capacitor (VNCAP). A large phase shift occurs when M_1 is off and M_2 is on to switch to larger inductance and capacitance in the signal path. As shown in Fig. 13, the designed 1-bit fine-tuning phase shifters present a higher insertion loss for the small-phase states (EN = 0) than for the large-phase states (EN = 1). The insertion loss for the small-phase states is mainly determined by a voltage divider formed with the load impedance, Z_0, and the parallel impedance of $2L_S$ and r_{ON1} as shown in Fig. 12. It is noted that the effect of C_{ds} and $C_{\mathrm{ON1,2}}$ on the small-phase state is not significant for the selected size of M_1, where C_{ds} is a parasitic capacitance between the drain and the source of M_1 formed by the electrical coupling through the drain and source metal lines and via stacks. A larger size of M_1 reduces r_{ON1}, thereby improving the insertion loss for the small-phase states. However, an increase in the size of M_1 also increases C_{ds} and C_{off1}, degrading the linear phase shift and broad matching behavior determined by a T-section formed with L_S and C_S for the large-phase state. Based on the tradeoff between small and large phase state performances, the selected size of M_1 is 24 μm with r_{ON1} of ~14 Ω, achieving an insertion loss lower than 1 dB for the small-phase states along with L_S (j13.5 Ω for 0°/11.25° and j17.7 Ω for 0°/22.5° at 140 GHz). The selected size of M_2 is 30 μm, considering that: 1) a larger size of M_2 reduces the insertion loss for the large phase state and 2) the insertion loss variation between the small and large phase stages should be smaller than 0.5 dB. The simulated phase shift and insertion loss variation between the two states are 12° (22°) and 0.5 dB (0.4 dB) at 140 GHz for the designed 0°/11.25° (0°/22.5°) phase shifter as shown in Fig. 13.

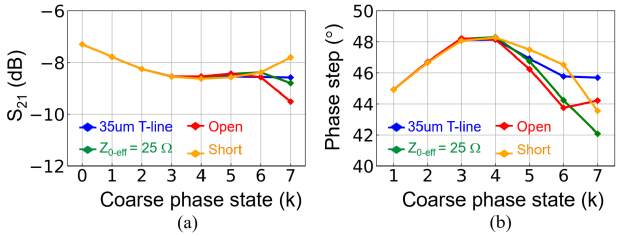


Fig. 15. Simulated (a) insertion loss and (b) phase steps at 140 GHz with respect to phase setting for different terminations.

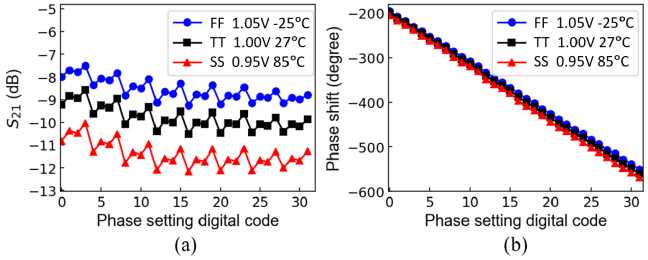


Fig. 16. (a) Simulated insertions loss and (b) phase shift at 140 GHz with respect to phase settings over PVT variations.

Fig. 14 shows the full schematic of the prototype 140-GHz phase shifter integrated with an ON-chip decoder. The pad capacitance and 90-μm transmission line form an L-matching network to transform $Z_{0,\mathrm{eff}}$ = 22 to 50 Ω. It is noted that the termination of 12-cascaded unit cells is carefully selected for uniform phase and insertion loss over phase states. Fig. 15 shows the simulated insertion loss and phase shift at 140 GHz with respect to phase setting for different types of termination such as short, open, $Z_{0,\mathrm{eff}}$, and shorted 35-μm transmission line. Based on the simulation results, a shorted 35-μm transmission line is chosen for the termination.

Fig. 16 shows the simulated insertion loss and phase shift at 140 GHz with respect to phase settings over three different PVT corners: (TT, 1.0 V, 27 °C), (SS, 0.95 V, 85 °C), and (FF, 1.05 V, −25 °C). While the average insertion loss varies from 8.9 to 11.3 dB, the rms phase errors and gain errors are kept lower than 2.4° and 0.5 dB for all corners, respectively. The robust gain and phase error controls over different PTV corners demonstrate the calibration-free feature of the proposed phase shifter. Fig. 17 shows the simulated IIP3 and OIP3 with respect to phase states for linearity characterization. The simulated IIP3 ranges from 23.7 to 24.9 dBm and OIP3 varies from

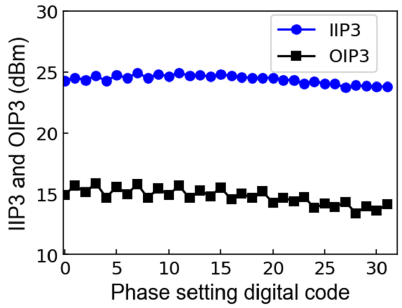


Fig. 17. Simulated IIP3 and OIP3 at 140 GHz.

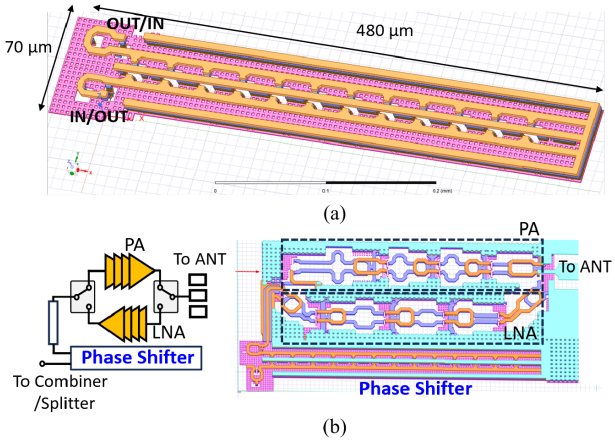


Fig. 18. (a) Three-dimensional layout view of the proposed phase shifter and (b) potential implementation example of a compact *D*-band TRX front-end integrated with the proposed phase shifter.

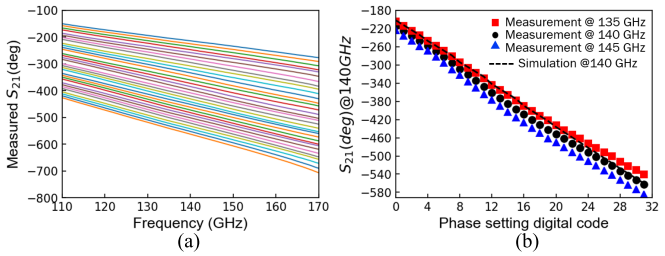


Fig. 19. (a) Measured phase shift over frequency for all phase states and (b) measured phase shift at 135, 140, and 145 GHz across phase settings.

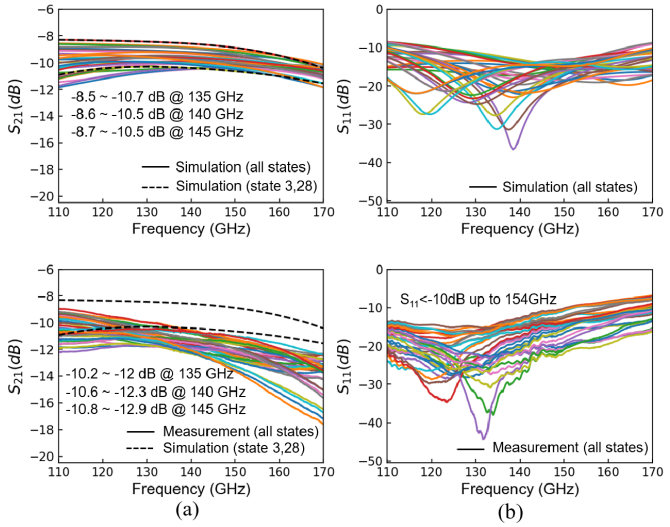


Fig. 20. Simulated and measured (a) insertion loss and (b) input return loss for all phase states.

13.6 to 15.9 dBm over different phase states, which presents the excellent linearity of the proposed phase shifter.

Fig. 18 shows the 3-D layout view of the proposed phase shifter and a potential implementation example of a compact *D*-band phased array transceiver integrated with the proposed phase shifter. A differential power amplifier (PA) and the low-noise amplifier (LNA) with single-ended input and output using baluns share the proposed phase shifter via a single-pole double-throw (SPDT) switch. The other port of the phase shifter is connected to a passive single-ended power combiner and splitter for a compact chip area [9]. The phase shifter is placed at the last stage of the receiver chain to minimize the noise contribution to the overall noise figure and at the first stage of the transmitter chain to minimize the degradation of the overall transmitter efficiency. As shown in Fig. 18, the proposed phase shifter will enable a compact phased array TRX frontend that can easily fit within a $\lambda/2$ (=1.07 mm at 140 GHz) lattice for a scalable AiP integration.

IV. Measurement Results

The prototype phase shifter was fabricated in GlobalFoundries' 45-nm RFSOI process. The chip photograph is shown in Fig. 14; the chip area is only 0.04 mm^2. The fabricated IC is characterized on a wafer for a VDD of 1.0 V by measuring *S*-parameters with Keysight N5242B PNA-X, N5292A mmWave test controller, and N5262BW06 *D*-band VNAX modules. An input power level applied to the IC from the VNAX module is calibrated with a VDI-Erickson PM5B power meter. The RF input and output GSG pads are probed with 100-μm pitch Cascade Infinity WR6 waveguide probes. The system was calibrated to the probe tips using the two-port short-open-load-through method using a Cascade Microtech 138–357 calibration substrate.

Fig. 19(a) shows the measured phase shift for all phase states with respect to frequency. The measured phase steps are uniform over a wide bandwidth and the phase tuning range increases with frequency due to the true time delay nature of the proposed phase shifter, reporting a phase tuning range greater than 360° at frequencies higher than 140 GHz. Fig. 19(b) shows the measured phase shift at 135, 140, and 145 GHz across phase settings in comparison to the simulation to present a linear phase control feature achieved by the proposed phase shifter. While the phase shift between the simulation and measurement are matched closely, there is some discrepancy in the middle of the curves due to the nonuniform steps of the measured phase shift. The potential source of such discrepancy is an imperfect impedance matching condition at the transition in Fig. 6. When some portion of an input signal is reflected from the transition due to imperfect impedance matching, the phase might not linearly increase with propagation distance due to standing-wave formation.

Fig. 20 shows the measured insertion loss and input return loss for all phase states in comparison to the simulation results. The measured insertion loss ranges from 10.6 to 12.3 dB at 140 GHz. The insertion loss variation across different phase settings is less than ±0.8 dB. The measured average insertion

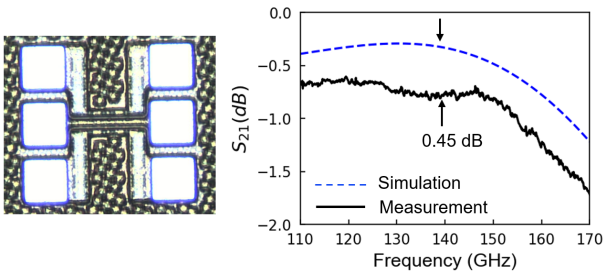


Fig. 21. Pad and interconnect breakout measurement.

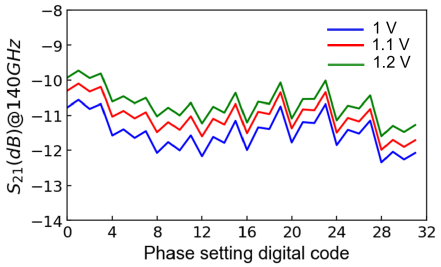


Fig. 22. Measured insertion loss at 140 GHz for different V_{DDs} with respect to phase settings.

loss is ∼1.7 dB higher than the simulated value at 140 GHz. The potential sources of such discrepancies are inaccurate modeling of pads, transistor switches, and electromagnetic coupling at high frequencies. The loss from the pads and interconnects is characterized using a breakout as shown in Fig. 21. The discrepancy between the simulation and measurement is 0.45 dB at 140 GHz. The measured input return loss of the proposed phase shifter is greater than 10 dB at frequencies up to 154 GHz for all phase states. The increase in VDD decreases the insertion loss further due to smaller r_{ON} as shown in Fig. 22. The measured insertion loss is reduced to 9.7∼11.6 dB for a VDD of 1.2 V. Fig. 23 shows the measured rms phase and gain errors for 15 IC samples in comparison to the simulation results. The rms phase error is lower than 2.4° from 130 to 150 GHz for all samples and reports the mean of 1.3° at 140 GHz which is the lowest among published phase shifters in similar frequency ranges. The rms gain error with respect to the average gain is lower than 1 dB from 130 to 150 GHz for all samples and the mean of the rms gain error is 0.52 dB at 140 GHz. Fig. 24 shows the histograms of the measured rms phase errors, rms gain errors, and average insertion loss at 135, 140, and 145 GHz for 15 IC samples. The small variation over different samples demonstrates the calibration-free feature of the proposed phase shifter. The demonstrated high phase control accuracy, uniform insertion loss over phase states, and small chip-to-chip variation are highly desirable features to reduce the complexity of the front-end control and calibration in a large-scale phase array.

Fig. 25 shows the measured large-signal gain with respect to input power at 140 GHz for different phase settings. Since the nonlinearity of transistor switches determines the overall linearity and it varies for ON and OFF states, four different phase states are selected based on the possible combinations of the minimum and maximum phase states of coarse and fine-tuning phase shifters. The measured input P1dB ranges from 12.9 to 14 dBm, which is greater than the simulation

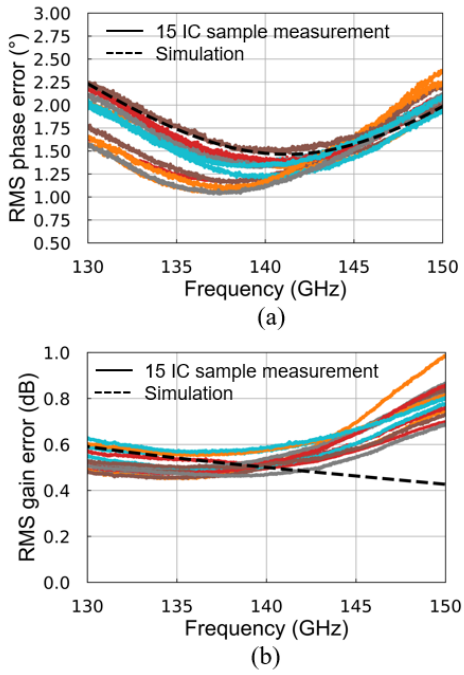


Fig. 23. Measured (a) rms phase errors and (b) rms gain errors with respect to frequency for 15 IC samples.

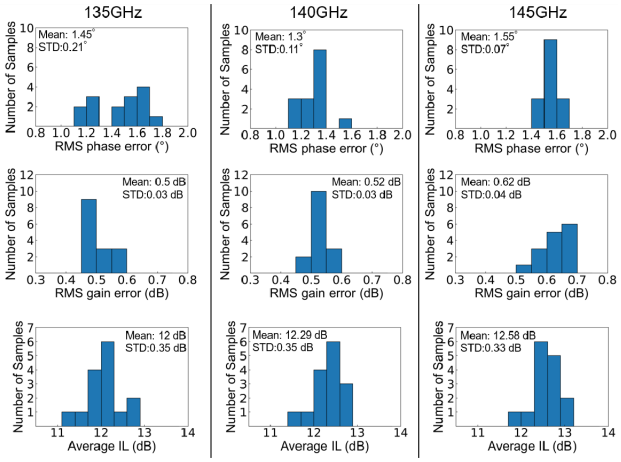


Fig. 24. Histograms of the measured rms phase errors, rms gain errors, and average insertion loss at 135, 140, and 145 GHz for 15 IC samples.

	Phase settings	
	Coarse	Fine
State0	000	00
State3	000	11
State28	111	00
State31	111	11

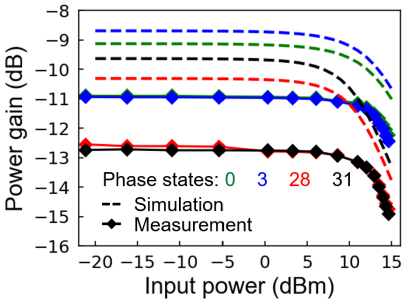


Fig. 25. Measured large-signal gain at 140 GHz with respect to input power for different phase states in comparison to simulations.

results (10–12.5 dBm). The discrepancy is due to higher insertion loss of the fabricated ICs and large-signal modeling inaccuracy of passive transistors. The measured linearity is superior to those reported in the active-type modulators in similar frequency bands.

TABLE I
PERFORMANCE SUMMARY IN COMPARISON WITH OTHER PUBLISHED PHASE SHIFTER ABOVE 100 GHZ

Metric	This work			IMS 2020[10]	MWCL 2018[11]	MWCL 2021[12]	SSCL 2023[13]	IMS 2018[14]	MWCL 2022[15]	SSCL 2023[16]
Frequency(GHz)	**135-145**			110-170	115	140-160	140-220	116-128	110-145	127.5
Type	**Passive**			Passive	Active	Active	Active	Active+ Passive	Active+ Passive	Active+ Passive
Phase range(°)	**360**			TTD*	360	360	360	360	360	360
S_{21} (dB)	**-10.6 ~ -12.3 (VDD=1V) -9.7 ~ -11.6 (VDD=1.2 V)**			-20 ~ -22	0.5	-4.5	-8.7	-5.8	< -5.5	1.5
RMS Gain error(dB)	**135GHz**	**140GHz**	**145GHz**	1.4	1.6	1.1~1.4	0.68~1.48	0.1~0.5	0.2~1.25	0.25~1.2
	0.47	**0.5**	**0.57**							
RMS Phase error(°)	**135GHz**	**140GHz**	**145GHz**	N.A.	5.5	1.6~7.5	12~16.2	2.2~12.5	3.5~13	<8.5
	1.25	**1.2**	**1.57**							
Number of states	**32**			16	16	32	4	32	16	16
IP1dB (dBm)	**12.9-14**			N.A.	-22$^{\$\#}$	2	-5.7	N.A.	-4.8	-9
P_{dc}(mw)	**0**			6.22	33	50	5.4	30	21	20.3
Bidirectional	**Yes**			Yes	No	No	No	No	No	No
Calibration requirement for the reported gain and phase errors	**No**			N.A.	Yes	Yes	Yes	Yes	Yes	Yes
Area(mm^2)	**0.04**			1.16	NA	0.05	0.02	0.405	0.572$^{\%}$	0.81
Multi-sample measurement	**Yes (15 samples)**			No	No	No	No	No	No	No
Process	**45RFSOI**			130-nm SiGe	130-nm SiGe	55-nm SiGe	90-nm SiGe	0.12um SiGe	90-nm SiGe	90-nm SiGe

* TTD (True-time delay) with the maximum delay of 6.64 ps, $: simulation, #: including LNA, %: including pads

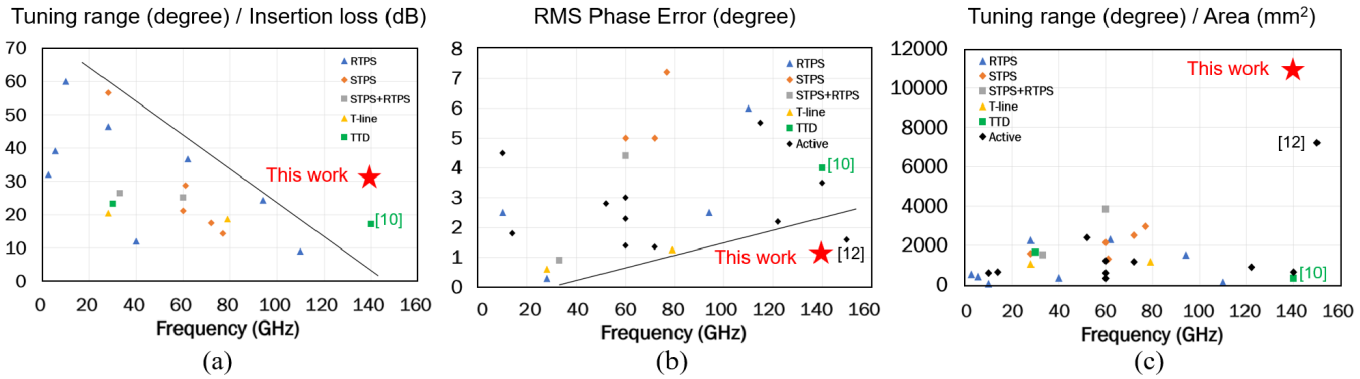


Fig. 26. Comparisons of this work to published phase shifters across different frequencies in terms of (a) phase tuning range per insertion loss, (b) rms phase error, and (c) phase tuning range per chip area.

Table I summarizes the performance of the proposed phase shifter in comparison to other published phase shifters in similar frequency ranges. The proposed phase shifter presents superior phase accuracy, low loss variation over phase states, high linearity, and compact chip area, while still providing the highest phase resolution and low insertion loss. This work also reports the first bi-directional, calibration-free phase shifter among the phase shifters reported at *D*-band. It is noteworthy that the reference active phase shifters with higher gain in Table I are implemented in a SiGe process that generally provides higher maximum available gain (G_{MAX}) than a CMOS process. Compared to [12] with a similar frequency range and resolution, the proposed work has ~6 dB lower gain, which can be compensated by adding a single-stage CMOS amplifier. It is reported that G_{MAX} of a 24-μm/40-nm differential pair is ~7 dB at 140 GHz with a bias current density of 0.3 mA/μm using a 45RFSOI process, which consumes much lower than 50 mW reported in [12].

Fig. 26 compares this work to published phase shifters across different frequencies in terms of three different figure of merits (FoMs). Phase tuning range per insertion loss [25] and phase tuning range per chip area are plotted for a fair comparison of insertion loss and chip area for different tuning ranges, considering that larger tuning range generally comes with higher insertion loss and larger chip area for passive phase shifters. The achieved FoMs are well beyond the performance envelope lines with respect to frequency.

V. CONCLUSION

This work demonstrates a low-loss passive phase shifter with calibration-free, precise phase control by exploiting a digitally programmable trombone-like passive network. The prototype 140-GHz phase shifter fabricated in a 45-nm RFSOI technology achieves the lowest rms phase error (1.2°) without calibration and the first bi-directional 360° tuning with no dc power consumption among state-of-the-art *D*-band phase

shifters. The prototype IC also exhibits low insertion loss and compact chip area. The proposed phase shifter is expected to motivate further development of large-scale *D*-band beamformers for next-generation communications and sensing.

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