# A 114–126-GHz Frequency Doubler With >10 dBm Output Power and >12% Efficiency in 45 nm RFSOI

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***Abstract*— This letter presents a D-band frequency doubler integrated with a power amplifier to achieve high output power and efficiency in 45 nm RFSOI. The proposed frequency doubler generates a broadband fully differential output by extracting the second-order harmonic from the shared source and drain nodes of a push-push differential pair and amplifying it through a common gate (CG) stage. The power amplifier exploits a novel device, the ADNFET developed by GlobalFoundries, which exhibits improved breakdown voltage for higher output power and efficiency. The fabricated IC integrates the proposed frequency doubler and power amplifier and reports the measured saturation output power greater than 10 dBm (11.7 dBm at 116 GHz) with a peak drain efficiency higher than 12% (15% at 116 GHz) from 114 to 126 GHz.**

***Index Terms*— ADNFET, CMOS, *D*-band, differential, frequency doubler, mm-wave, power amplifier, radar transmitter.**

## I. Introduction

THE *D*-band frequency spectrum (110–170 GHz) provides abundant available bandwidth for next-generation communications and high-precision sensing. By exploiting a wide bandwidth and small wavelength for high resolution, a compact *D*-band frequency-modulated continuous wave (FMCW) imaging radar technology in silicon enables a wide range of applications including industrial, automotive, infrastructure, IoT, security, and healthcare applications. One of the challenges in a silicon-based *D*-band FMCW radar is to generate a wideband frequency-modulated signal with high transmitter output power and efficiency. Voltage-controlled oscillators used for frequency modulation have a limited-frequency tuning range and phase noise above 100 GHz. To avoid this problem, a frequency multiplier can be placed after an oscillator operating at a moderate frequency [1], [2], [3], [4], [5]. A common frequency multiplier topology is a push-push frequency doubler based on a differential pair with a shared drain connection [6]. However, the output of the push-push frequency doubler is intrinsically single-ended, which poses a challenge to generate a fully differential output to drive a subsequent differential amplifier. A Gilbert-cell frequency doubler can generate a wideband fully differential output at the cost of high dc power consumption [7].

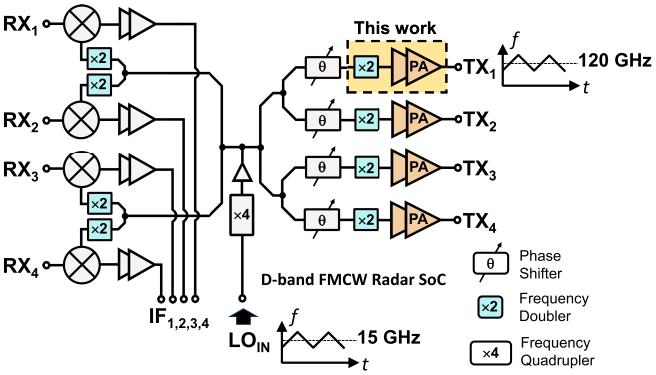


Fig. 1. *D*-band imaging radar SoC using the proposed radar transmitter.

On the other hand, the generation of high output power with good power efficiency above 100 GHz is limited by $f_{max}$ and the breakdown voltage of silicon transistors. To address this challenge, GlobalFoundries recently developed a novel device, the ADNFET, optimal for designing a mmWave power amplifier in a 45-nm RFSOI process [8]. The ADNFET optimizes the source and drain junctions, channel doping, and gate length to achieve an increased maximum allowable voltage and $f_{MAX}$. This letter proposes a 120-GHz frequency doubler with a fully differential output followed by an ADNFET-based power amplifier for a high-power, high-efficiency *D*-band radar transmitter front-end. The proposed radar transmitter reports a measured output power greater than 10 dBm (11.7 dBm at 116 GHz) and drain efficiency >12% (15% at 116 GHz) from 114 to 126 GHz in a 45 nm RFSOI process.

## II. Proposed Frequency Doubler

Fig. 1 shows the block diagram of a four-channel 120-GHz imaging radar system-on-chip (SoC) where the proposed transmitter can potentially be used. The radar SoC consists of four phase-shifting transmitters, four mixer-first receivers, and LO generation circuitry. An input LO signal at 15 GHz is up-converted to 60 GHz with a frequency quadrupler and distributed to the transmitter and receiver front-ends. The LO signal distributed to each transmitter front-end is then phase-shifted, up-converted to 120 GHz, and amplified for transmission at each element. To realize this architecture, we propose a power-efficient, high-power 120-GHz transmitter that consists of a frequency doubler with a differential output followed by a power amplifier. Fig. 2(a) shows the proposed frequency doubler with a broadband fully differential output.

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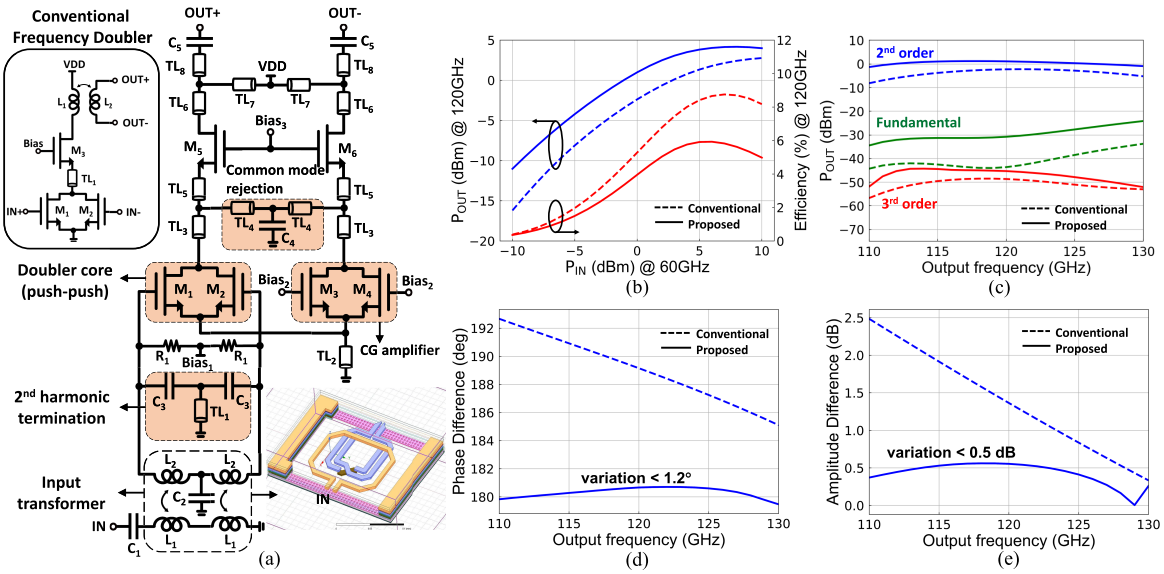


Fig. 2. (a) Schematic of the proposed fully differential frequency doubler and simulations of (b) $P_{OUT}$ and drain efficiency at 120 GHz versus $P_{IN}$, (c) $P_{OUT}$ versus output frequency for different harmonics for $P_{IN}$ of 0 dBm, (d) phase difference between OUT+ and OUT− across frequency, and (e) amplitude difference between OUT+ and OUT− across frequency.

It is based on a push-push topology consisting of $M_1$ and $M_2$ driven by a differential input signal at 60 GHz. A differential input signal is generated from a single-ended input through a transformer shown in the inset of Fig. 2. $M_1$ and $M_2$ share drain and source nodes to extract the second-order harmonic ($2\omega$) while suppressing the fundamental frequency ($\omega$). To improve the conversion gain of the frequency doubler, a $2\omega$ harmonic termination input network formed with $C_3$ and $TL_1$ is designed to provide a short at $2\omega$ (common mode) due to a series resonance of $TL_1$ and $C_3$. For a differential input signal at $\omega$, only $C_3$ is present due to the virtual ground and absorbed as a part of the input matching network. The gate voltage of $M_{1,2}$ is biased around 0.2 V for the maximum conversion gain. The proposed frequency doubler extracts the second-order harmonic ($2\omega$) with an opposite phase from the shared source node of $M_{1,2}$ to generate a differential output. The extracted $2\omega$ current from the shared source node is applied to the input of a common-gate (CG) amplifier. A similar topology was proposed for an $E$-band frequency doubler in a SiGe process [9]. The main transistors $M_{3,4}$ of the CG amplifier copy the $M_{1,2}$ push-push differential pair in transistor size and layout for a balanced differential signal. $TL_2$ resonates out the device capacitance of $M_{1,2,3,4}$ at the second-order harmonic frequency to provide a high impedance at the common node, thereby ensuring that the $2\omega$ current from the shared source of $M_{1,2}$ flows into $M_{3,4}$. The output currents from $M_{1,2}$ and $M_{3,4}$ at $2\omega$ flow to the cascode devices $M_5$ and $M_6$, respectively, for improved conversion gain and isolation. To improve the amplitude and phase balance for the differential signal, a multifunctional network formed with $TL_4$ and $C_4$ is placed between the two drain nodes of $M_{1,2}$ and $M_{3,4}$. This network provides a short for a common-mode signal at $2\omega$ due to a series resonance of $TL_4$ and $C_4$ for common-mode rejection. On the other hand, for a differential signal at $2\omega$, only $TL_4$ is present to the virtual ground and absorbed into a part of the matching network. $TL_{6,7,8}$ and $C_5$ form the output network.

Fig. 2(b)–(e) shows the simulated performance of the proposed frequency doubler in comparison to its conventional counterpart. Note that the conventional frequency doubler has the same differential pair $M_{1,2}$ and input matching network, including the $2\omega$ harmonic termination (omitted in the schematic for simplicity) as the proposed one. The schematic is shown in the inset of Fig. 2. To generate a differential output signal in the conventional push-push frequency doubler, a balun is placed at the output. The proposed frequency doubler exhibits a simulated saturation output power at 120 GHz greater than 4 dBm with a peak conversion gain higher than 1 dB (~3 dB higher than the conversion gain of the conventional one). The peak drain efficiency of the proposed frequency doubler is 5.9%, while the drain efficiency of the conventional doubler is 8.7%. The efficiency of the proposed design is slightly lower due to the dc power consumption of the auxiliary CG amplifier ($M_{3,4}$) to generate a balanced differential output. Note that the overall power efficiency of the proposed transmitter is dominated by the subsequent power amplifier. The transistor size of the frequency doubler is selected to generate enough output power that the power amplifier can operate close to saturation. Fig. 2(c) shows the output power at $2\omega$ for an input frequency from 55 to 65 GHz when the input power is 0 dBm. The output power of the proposed frequency doubler is $-0.5 \pm 0.5$ dBm from 112 to 126 GHz. Fig. 2(d) and (e) shows the simulated phase and amplitude imbalances of the proposed frequency doubler in comparison to the conventional one. The simulated phase and amplitude imbalances of the proposed doubler are less than 1.2° and 0.5 dB, respectively, from 110 to 130 GHz, which are superior to those of the conventional frequency doubler.

To achieve an output power greater than 10 dBm, a two-stage power amplifier is designed as shown in Fig. 3(a). Each stage is based on a differential nMOS pair with neutralization capacitors implemented with vertical natural capacitors (VNCAPs). The output differential pair is implemented with ADNFETs for a higher output swing enabled by an increased power supply, improving the output power and efficiency. The frequency-staggering technique, tuning each stage of a multistage amplifier to slightly different frequencies around

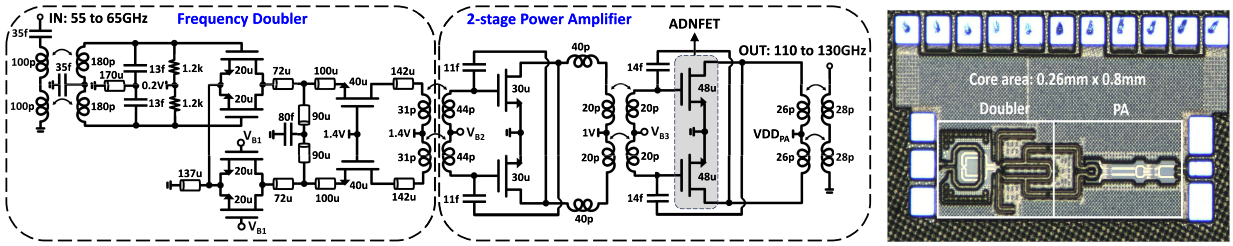


Fig. 3. (a) Schematic of the proposed radar front end that integrates the frequency doubler and two-stage power amplifier. (b) Chip photo of the proposed radar transmitter front-end.

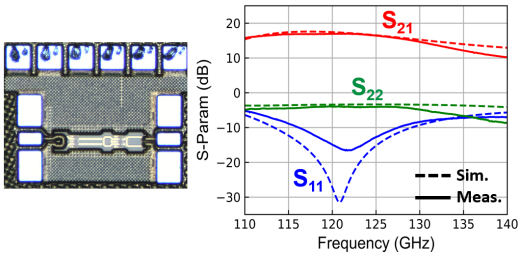


Fig. 4. PA breakout die photo and measured *s*-parameter.

TABLE I

PERFORMANCE SUMMARY IN COMPARISON WITH OTHER PUBLISHED FREQUENCY DOUBLERS

| | **This work** | [1] | [2] | [3] | [4] | [5] |
|---|---|---|---|---|---|---|
| Frequency (GHz) | **114-126** | 100-123 | 125-145 | 96-134 | 126-146 | 95-150 |
| Output buffer | **Y** | Y | N | N | N | N |
| $CG_{max}$ (dB) | **13.3** | 17.2 | -5.5 | -6.2 | -4.5 | -8 |
| $P_{sat}$ (dBm) | **> 10 (11.7 @ 116 GHz)** | 5.5 | 4.1 | 1.8 | 0.5 | 3 |
| $P_{DC}$ (mw) | **103** | 116 | 24.7 | 12 | 12 | 19.2-22.8 |
| $DE_{Peak}$ (%) $=P_{OUT}/P_{DC}$ | **>12 (15 @ 116 GHz)** | 3 | 11.8 | 8.3 | 7.4 | 8.75 |
| Area ($mm^2$) | **0.2** | 0.832* | 0.081 | 0.19 | 0.49 | 0.24 |
| Technology | **45nm RFSOI** | 65nm CMOS | 22nm FDSOI | 28nm CMOS | 28nm CMOS | 65nm CMOS |

* including pads

the center frequency, is used to extend bandwidth. The output transformer is designed using a load-pull analysis to achieve maximum output power. The PA breakout circuitry is fabricated and measured as shown in Fig. 4. The measured peak gain is 17.5 dB at 118 GHz with a 3-dB bandwidth greater than 22 GHz. The simulated OP1dB and $P_{sat}$ are 8.8 and 12.8 dBm, respectively, at 120 GHz. The simulated peak PAE is 20.4% at 120 GHz.

## III. MEASUREMENT

The proposed radar transmitter front-end was fabricated in GlobalFoundries' 45-nm RFSOI process. The chip photograph is shown in Fig. 3(b); the chip area is 0.2 $mm^2$. The fabricated IC is characterized on a wafer by measuring output power and dc power consumption for different input power levels and frequencies. An input signal is generated using a Keysight E8257D signal generator, and output power is measured using a VDI-Erickson PM5B power meter. Fig. 5(a) shows the measured output power $P_{OUT}$ and drain efficiency given by $P_{OUT}/P_{DC}$ versus input power at 58 GHz, where $P_{DC}$ is the total dc power consumption. The saturation output power and peak drain efficiency are improved from 10.5 dBm and 14% to 11.7 dBm and 15% as $VDD_{PA}$ increases from 1.0 to 1.2 V,

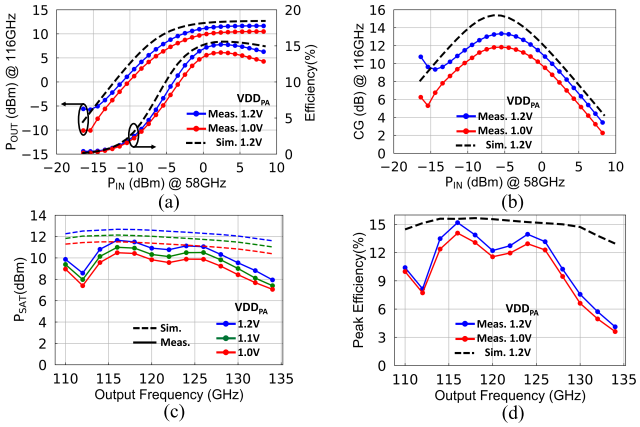


Fig. 5. Measured performance of (a) $P_{OUT}$ and drain efficiency at 116 GHz versus $P_{IN}$, (b) conversion gain at 116 GHz versus $P_{IN}$, (c) $P_{SAT}$ versus output frequency, and (d) peak drain efficiency versus output frequency.

respectively. Fig. 5(b) shows the measured conversion gain versus input power at 58 GHz, which reports a peak conversion gain of 13.3 dB for $VDD_{PA}$ of 1.2 V. Fig. 5(c) shows the measured saturation output power $P_{SAT}$ versus output frequency for different $VDD_{PA}$. The saturation output power is greater than 10 dBm for $VDD_{PA}$ of 1.2 V at output frequencies from 114 to 128 GHz with a peak $P$ of 11.7 dBm at 116 GHz. Fig. 5(d) shows the measured peak drain efficiency versus output frequency. The peak drain efficiency is greater than 12% from 114 to 126 GHz and has a maximum of 15% at 116 GHz for $VDD_{PA}$ of 1.2 V. Table I summarizes the performance of the proposed frequency doubler along with other published mmWave frequency doublers in similar frequency bands.

## IV. CONCLUSION

This work demonstrates a power-efficient, high-power frequency doubler integrated with a power amplifier for a *D*-band FMCW imaging radar transmitter. The proposed frequency doubler exhibits a fully differential output by extracting the second-order harmonic from both the shared source and drain nodes of a push-push differential pair and amplifying it through a CG amplifier. The power amplifier exploits ADNFETs for high output power and efficiency. Fabricated in a 45 nm RFSOI, the proposed transmitter achieves a saturation output power greater than 10 dBm and drain efficiency higher than 12% from 114 to 126 GHz.

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