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Extension Doping with Low-Resistance Contacts for P-Type Monolayer WSe_2 Field-Effect Transistors

Sihan Chen, Yue Zhang, William P. King, Rashid Bashir,* and Arend M. van der Zande**

Source/Drain extension doping is crucial for minimizing the series resistance of the ungated channel and reducing the contact resistance of field-effect transistors (FETs) in complementary metal–oxide–semiconductor (CMOS) technology. 2D semiconductors, such as MoS_2 and WSe_2, are promising channel materials for beyond-silicon CMOS. A key challenge is to achieve extension doping for 2D monolayer FETs without damaging the atomically thin material. This work demonstrates extension doping with low-resistance contacts for monolayer WSe_2 p-FETs. Self-limiting oxidation transforms a bilayer WSe_2 into a hetero-bilayer of a high-work-function WO_xSe_y on a monolayer WSe_2. Then, damage-free nanolithography defines an undoped nano-channel, preserving the high on-current of WO_xSe_y-doped FETs while significantly improving their on/off ratio. The insertion of an amorphous WO_xSe_y interlayer under the contacts achieves record-low contact resistances for monolayer WSe_2 over a hole density range of 10^{12} to 10^{13} cm^{-2} (1.2 ± 0.3 kΩ μm at 10^{13} cm^{-2}). The WO_xSe_y-doped extension exhibits a sheet resistance as low as 10 ± 1 kΩ $\square^{-1}$. Monolayer WSe_2 p-FETs with sub-50 nm channel lengths reach a maximum drain current of 154 μA μm^{-1} with an on/off ratio of 10^7–10^8. These results define strategies for nanometer-scale selective-area doping in 2D FETs and other 2D architectures.

1. Introduction

Doping the source/drain extensions is essential for optimizing the performance of field-effect transistors (FETs) in complementary metal–oxide–semiconductor (CMOS) technology. In CMOS, the top-gate underlaps the source/drain to minimize parasitic capacitance for fast operation. The source/drain extensions are ungated and must be heavily doped to minimize their series resistance.[1] Additionally, extension doping lowers the metal-semiconductor contact resistance[2,3] and adjusts the threshold voltage.[4,5] Monolayers of 2D semiconductors, including transition metal dichalcogenides (TMDs) such as MoS_2 and WSe_2, represent the ultimate channels in transistor scaling, due to their atomically thin bodies and dangling-bond-free surfaces.[6] However, contact resistance remains one of the major technical hurdles to realizing 2D FETs in CMOS,[6] and more broadly across applications in electronic and optoelectronic devices from 2D materials and heterostructures.[7] While n-type contacts to TMD monolayers close to the quantum limit have been demonstrated,[8] achieving low-resistance contacts to p-type monolayer 2D semiconductors remains challenging, especially when approaching nanometer-scale dimensions.[9] Developing new strategies to design nanometer-scale extension doping into monolayer 2D

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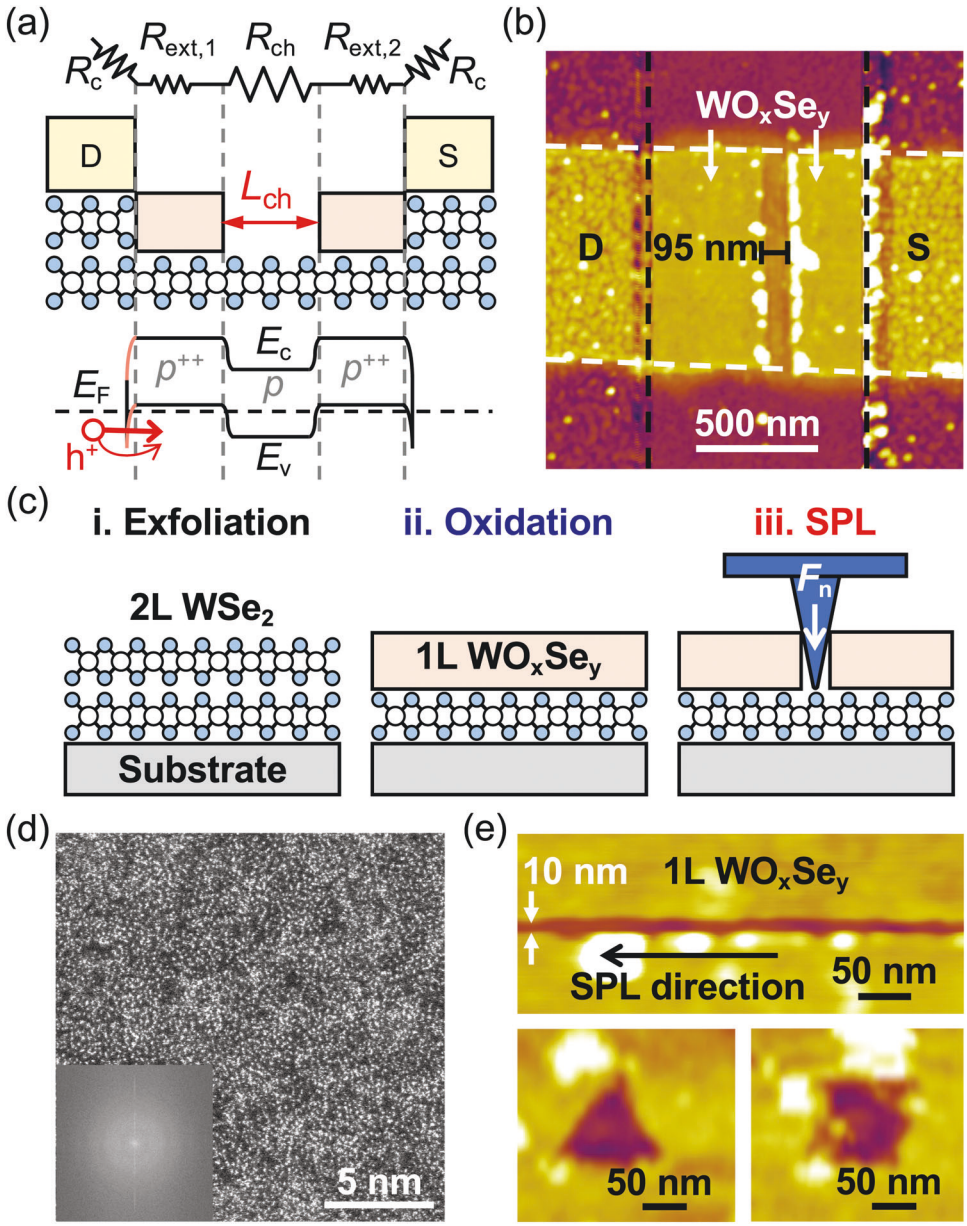

Figure 1. Concept of a monolayer WSe_2 p-FET with doped extensions based on self-limiting oxidation and nanolithography. a) Equivalent circuit (top), schematic (middle), and band diagram (bottom) of a monolayer WSe_2 p-FET with WO_xSe_y-doped extensions. b) AFM topography of a monolayer WSe_2 p-FET with WO_xSe_y-doped extensions. The dashed black lines delineate the boundaries of the source (S) and drain (D), while the dashed white lines outline the edges of the WSe_2. c) Schematic showing the fabrication process of selectively WO_xSe_y-doped monolayer WSe_2. d) HAADF-STEM image of a freestanding monolayer WO_xSe_y film and the corresponding FFT pattern. e) Examples of nanopatterns of 1L WO_xSe_y on 1L WSe_2 created by mechanical SPL.

semiconductors is a critical step in minimizing source/drain extension resistance and contact resistance, thereby realizing the potential of 2D semiconductors as channel materials in beyond-silicon CMOS.

Unfortunately, conventional doping techniques used in CMOS, such as ion implantation or substitutional doping, do not work well with 2D monolayer semiconductors, because of the creation of defects that damage the delicate atomic structure,[10–12] the difficulty of achieving selective doping,[13–16] or elevated processing temperatures that surpass the thermal budget of silicon back-end-of-line integration (< 400 °C).[17–19] Surface charge transfer doping (SCTD), which relies on the charge transfer between the channel material and the surface dopant is a promising approach for extension doping in 2D FETs, due to its low processing temperature and effectiveness to dope surface materials without inducing defects.[20] Various chemical and physical deposition based SCTD methods have been explored for TMDs.[21–29] One particularly promising strategy is oxidizing the surface of TMDs like WSe_2 with O_2 plasma or UV/ozone to form a self-limiting oxide layer

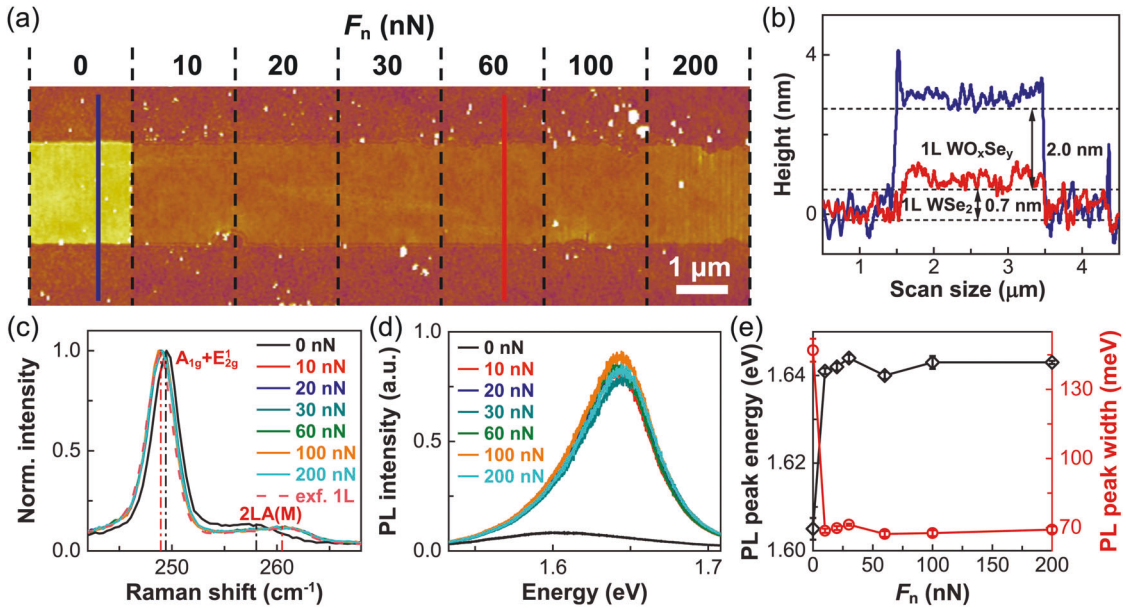

Figure 2. Exploring the optimal SPL force for AFM scratching of 1L WO_xSe_y on 1L WSe_2. a) AFM topography of 1L WO_xSe_y on 1L WSe_2 after SPL with a normal force F_n of 0 to 200 nN. b) Line scans along the solid blue and red lines in (a). c) Normalized Raman spectra and d) PL spectra of 1L WSe_2 from different regions in (a). The dashed pink line corresponds to the normalized Raman spectrum of pristine as-exfoliated (exf.) 1L WSe_2. e) PL peak energy and peak width extracted from the PL spectra in (d) versus F_n.

such as WO_x and WO_xSe_y on top of undamaged layers.[30–36] These high-work-function oxides generate strong hole doping in the underlying channel material,[30–33] yet are stable in air for months,[31–33] and are CMOS-compatible.[33,37,38] Key questions include how to realize oxidation-based selective-area doping for TMD monolayers, and how extension doping impacts the sheet and contact resistances and the overall FET performance in the technology-relevant short channel limit.

In this study, we demonstrate extension doping with low-resistance contacts for p-type monolayer WSe_2 FETs by combining self-limiting oxidation with nanolithography. Using damage-free nanolithography, we create short-channel monolayer WSe_2 p-FETs with doped extensions, preserving the high on-current of WO_xSe_y-doped FETs while significantly improving their on/off ratio. We systematically characterize the sheet resistance of doped extensions and contact resistance using the transfer length method. We find that inserting a monolayer of amorphous WO_xSe_y between evaporated metal contacts and monolayer WSe_2 reduces the contact resistance by over an order of magnitude. One monolayer WSe_2 p-FET reaches a record-high drain current of $> 150\ \mu A\ \mu m^{-1}$ under a 1 V drain-source bias at a hole density below $10^{13}\ cm^{-2}$. These achievements the performance gap between p-type and n-type 2D monolayer transistors, demonstrating a promising route to realizing beyond-silicon electronics and optoelectronics with 2D monolayers and heterostructures.

2. Results and Discussion

2.1. Extension Doping

Figure 1 illustrates the concept of extension doping for monolayer WSe_2 FETs by integrating self-limiting oxidation with nanolithography. Figure 1a depicts a monolayer WSe_2 p-FET with WO_xSe_y-doped extensions. The total resistance consists of the channel resistance (R_{ch}), source/drain extension resistances ($R_{ext,1}$ + $R_{ext,2}$), and contact resistances ($2R_c$) in series. The monolayer WSe_2 channel exhibits light p-doping,[39] while the source/drain extensions are degenerately p-doped due to the high-work-function WO_xSe_y withdrawing electrons from the underlying monolayer WSe_2.[31,32] This results in energy bands bending near the metal-semiconductor junction, reducing the Schottky barrier width. Extension doping with WO_xSe_y serves to reduce both extension and contact resistances, enhancing the electrical performance of monolayer WSe_2 p-FETs. Figure 1b shows the atomic force microscopy (AFM) topography of an example monolayer WSe_2 p-FET with WO_xSe_y-doped extensions. The channel length L_{ch} is 95 ± 5 nm, and the sum of the lengths of the source/drain extensions L_{ext} is 740 ± 20 nm. The electrical characteristics of the FET are discussed in detail in Figure 3.

Figure 1c illustrates the fabrication process for selectively doping monolayer WSe_2 with WO_xSe_y. All process details are in the Methods. First, bilayer (2L) WSe_2 is exfoliated onto a substrate (i). The topmost layer of WSe_2 is then oxidized using a controlled remote O_2 plasma process, forming a monolayer (1L) p-dopant WO_xSe_y on top of 1L WSe_2 (ii). Finally, mechanical scanning probe lithography (SPL) is used to selectively remove 1L WO_xSe_y from 1L WSe_2 (iii). In mechanical SPL, an AFM probe scratches the surface material in contact mode with a normal force F_n.[40–42] As we will show in **Figure 2**, the significant difference in mechanical strength between WO_xSe_y and WSe_2 allows for precise patterning by removing the top WO_xSe_y without damaging the underlying WSe_2. The removed WO_xSe_y accumulates along the boundaries of the scanned region. We choose mechanical SPL over additive lithography methods, such as optical and e-beam lithography, because the resist materials used in additive

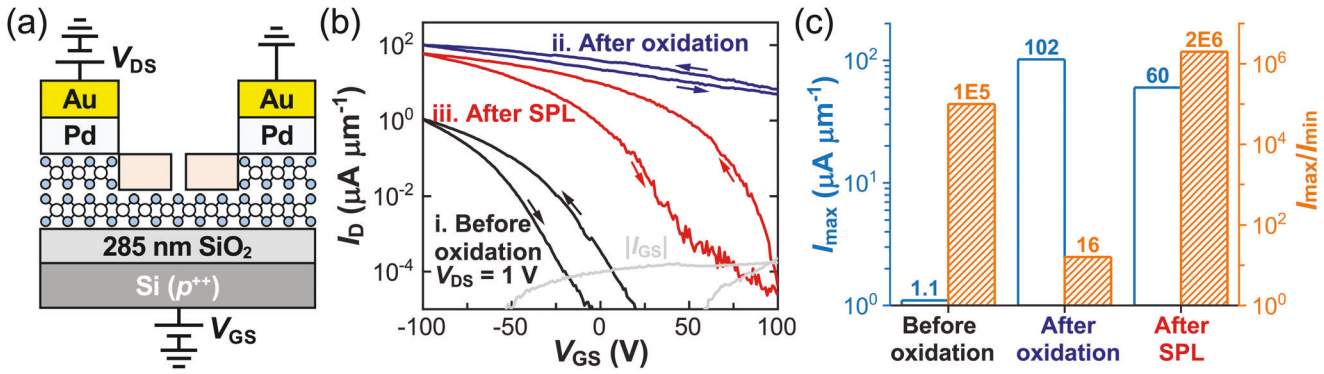

Figure 3. Example monolayer WSe_2 p-FET (Device A) with WO_xSe_y-doped extensions. a) Schematic of the electrical connections used to characterize the FET. b) Transfer curves of the FET before oxidation, after oxidation, and after SPL. V_{DS} = 1 V. The gray line plots the gate leakage $|I_{GS}|$ of the FET measured after SPL. c) I_{max} and I_{max}/I_{min} at each stage of fabrication.

lithography are difficult to remove and degrade the p-doping effect of oxidized TMDs.[43,44]

Spectroscopy measurements in Figure S1 (Supporting Information) confirm the oxidation process is self-limiting to the topmost layer of WSe_2. X-ray photoelectron spectroscopy (XPS) spectra in Figure S2 (Supporting Information) reveal the appearance of both W—O and Se—O bonds after oxidation, indicating the formation of WO_xSe_y rather than pure WO_x. Figure 1d shows a high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image and the corresponding fast Fourier transform (FFT) pattern of monolayer WO_xSe_y, which appears amorphous and homogeneous. The amorphous monolayer WO_xSe_y is insulating.[45] Figure 1e shows AFM topography images of nanopatterns of 1L WO_xSe_y on 1L WSe_2 fabricated using mechanical SPL with an F_n of 130 nN, with the narrowest constriction being ≈10 nm. Figure S3 (Supporting Information) shows a scanning electron microscopy (SEM) image of a typical SPL probe with a tip radius of 14 ± 1 nm.

A key fabrication challenge for achieving extension doping with mechanical SPL is to determine the applied force capable of removing WO_xSe_y without damaging the underlying monolayer WSe_2. The mechanical properties of amorphous 2D monolayers remain largely unexplored.[46,47] In Figure 2, we combine AFM with Raman and photoluminescence (PL) spectroscopy to investigate the optimal force for SPL. Raman and PL spectra of TMD monolayers are sensitive to defects, doping, and strain,[48–54] making them reliable indicators of the material properties of the underlying monolayer WSe_2.

Figure 2a shows an AFM topography image of a single WSe_2 (bottom)/WO_xSe_y (top) hetero-bilayer microribbon, patterned with rectangles of sequentially increasing F_n from 0 to 200 nN. This data shows that even a moderate F_n of 10 nN is sufficient to scratch amorphous WO_xSe_y. We note that multiple SPL scans are required for complete removal. Five scans were needed to entirely remove WO_xSe_y with an F_n of 10–20 nN, and only 1–2 scans with an F_n of 30 nN or larger. Figure 2b shows the height profile from regions corresponding to F_n = 0 nN and F_n = 60 nN and reveals a thickness of 0.7 ± 0.1 nm for 1L WSe_2 and 2.0 ± 0.1 nm for 1L WO_xSe_y.

Figure 2c shows the normalized Raman spectra of monolayer WSe_2 from different regions in Figure 2a. The presence of both A_{1g}+$E_{2g}{}^1$ and 2LA(M) peaks suggests the preservation of the crystalline structure of the underlying 1L WSe_2 after SPL with an F_n of 10–200 nN. With the removal of WO_xSe_y, the A_{1g}+$E_{2g}{}^1$ peak redshifted by 0.5 cm^{-1} while the 2LA(M) peak blueshifted by 2.5 cm^{-1}, indicating reduced p-doping in WSe_2.[51,52] These Raman peaks of 1L WSe_2 obtained after the removal of WO_xSe_y exhibit no shift compared to those of pristine as-exfoliated 1L WSe_2, confirming that the WSe_2 remains undamaged by the self-limiting oxidation and SPL processes. Raman peak positions exhibit no additional dependence on F_n after SPL within the 10–200 nN range, suggesting negligible variations in material quality, doping, and strain.[51–54]

Figure S4 (Supporting Information) shows a map of the PL peak intensity corresponding to Figure 2a. Figure 2d presents the averaged PL spectra from the center of each region, while Figure 2e plots the fitted PL peak energy (black) and PL peak width (red) as a function of F_n. Figure 2e reveals that the PL peak blueshifted by 37 ± 1 meV and the peak width decreased by 78 ± 1 meV after SPL, reconfirming reduced p-doping to 1L WSe_2 following the removal of WO_xSe_y.[32] PL peak intensity, position, and width also exhibit no discernible dependence on F_n between 10 and 200 nN.

In summary, a normal force as small as 10 nN could scratch amorphous monolayer WO_xSe_y, but effective removal of WO_xSe_y begins at ≈30 nN. There is no noticeable damage to the underlying monolayer WSe_2 up to 200 nN, suggesting a much weaker shear strength of amorphous TMD monolayers compared to crystalline TMD monolayers, as well as weak adhesion between crystalline TMDs and their surface oxide. Hereafter, we used F_n = 40–60 nN for SPL in the FET fabrication shown below.

In **Figure 3**, we demonstrate the enhanced electrical performance of a WSe_2 FET with extension doping by comparing its transport characteristics at key steps of the fabrication process: i) as a bilayer WSe_2 FET before oxidization, ii) as a WSe_2 (bottom)/WO_xSe_y (top) hetero-bilayer after oxidization, and iii) after SPL patterning of the undoped nanochannel and extensions. Figure 3a illustrates the electrical connections used to characterize the FET. This FET corresponds to the device shown in Figure 1b. Figure 3b presents the I_D–V_{GS} sweeps of the FET at keys steps through the fabrication process. Figure 3c highlights two key metrics of a field-effect transistor at each key step: the maximum drain current I_{max}, and the maximum-to-minimum current ratio I_{max}/I_{min}. As expected, the FET could not be turned

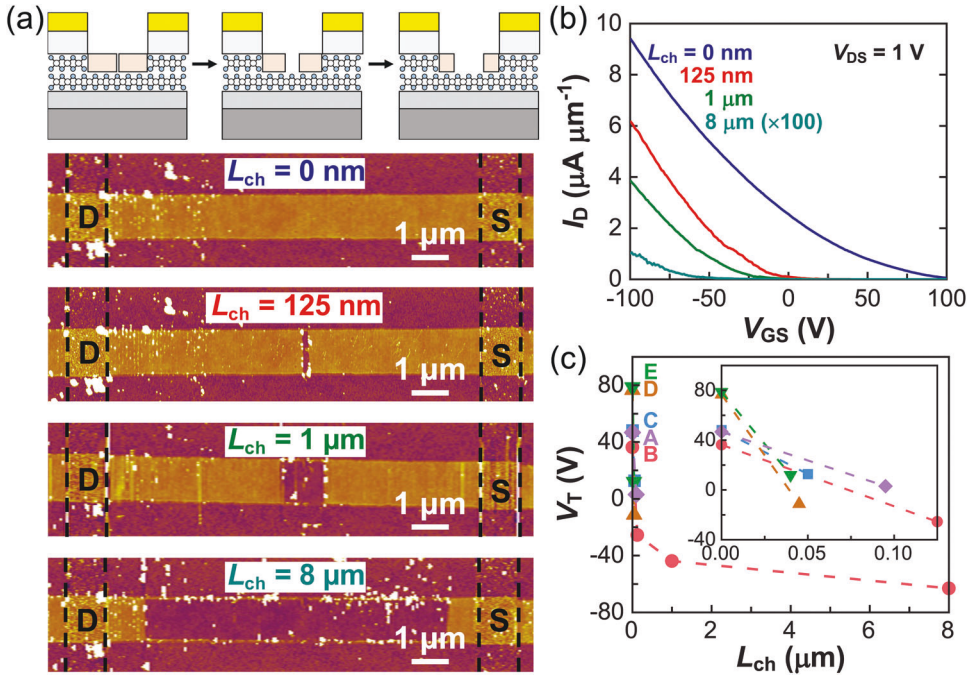

Figure 4. Tuning the threshold voltage. a) Schematic (top) and AFM topography (bottom) of a WO_xSe_y-doped monolayer WSe_2 p-FET (Device B) with sequentially increased L_{ch} (from top to bottom). The dashed black lines delineate the edges of the source and drain. b) Transfer curves of the FET with different L_{ch}. c) V_T versus L_{ch}. The V_T versus L_{ch} data of other Devices reported in this work (Devices A, C–E) are also included in this plot for analysis.

off after oxidation, with I_{max} increasing by 100 times and the I_{max}/I_{min} ratio decreasing by 10^4. SPL with an L_{ch} of 95 ± 5 nm improved the I_{max}/I_{min} ratio by 10^5, while slightly decreasing I_{max} by 40%. Overall, the monolayer WSe_2 p-FET with WO_xSe_y-doped extensions exhibited an over one order of magnitude improvement in both I_{max} and I_{max}/I_{min} compared to the initial bilayer WSe_2 FET. The hysteresis was 13.1 V before oxidation, 21.7 V after oxidation, and 38.9 V after SPL. The soft dipoles formed between WO_xSe_y and WSe_2 may be affected by the backgate electric field, producing a large hysteresis loop during the backgate sweep.[23] In comparison, top-gated multilayer WSe_2 FETs with WO_xSe_y-doped extensions have achieved negligible hysteresis, where the top-gate field was not applied to WO_xSe_y dopants.[33]

Achieving a threshold voltage V_T close to 0 V is crucial in CMOS. Many studies on 2D FETs have shown V_T values significantly deviating from 0 V, preventing the device from turning off at a gate voltage of 0 V.[55] Therefore, strategies to develop 2D n-FETs with a slightly positive threshold voltage and 2D p-FETs with a slightly negative threshold voltage are needed.[9] **Figure 4** explores the proximity effects that tune the threshold voltage of a monolayer WSe_2 p-FET by successively removing the surface dopant WO_xSe_y from the channel with SPL, which concurrently increases L_{ch} and decreases L_{ext}. Figure 4a presents the schematic and corresponding AFM images of the same FET, with L_{ch} increased from 0 nm to 8 μm. Figure 4b compares the transfer characteristics of the same FET with different L_{ch}. Figure 4c shows the V_T versus L_{ch}. An L_{ch} near 50–100 nm achieved a V_T close to 0 V. The maximum ΔV_T reached 99.4 V, demonstrating the potential to implement multiple V_T by adjusting L_{ch}. V_T decreased significantly when L_{ch} increased from 0 to 40–50 nm, suggesting that the effective lateral penetration depth of extension doping is much less than ≈20 nm. Figure S5 (Supporting Information) demonstrates that the WO_xSe_y doping was stable over several days in air, so the V_T drift during the experiment could be ignored.

2.2. Contact Engineering

Another crucial feature of extension doping is the contact resistance at the extension-electrode interface. Numerous studies have reported a significant reduction in contact resistance in TMD p-FETs following oxidation.[30–33,37,43,53,56] However, these studies typically involve the deposition of high-work-function metal contacts onto TMDs with high kinetic energy prior to oxidation, which inevitably causes defects at the metal/TMD interface and results in Fermi level pinning.[9,57] Introducing an ultrathin interlayer between evaporated metal contacts and the 2D semiconductors could mitigate metal-induced gap states, leading to Fermi level depinning.[58–62]

In **Figure 5**, we systematically compare different interface structures and processes to optimize the contacts. Figure 5a illustrates the out-of-plane structure and hypothesized band diagrams for two electrode contact configurations: one with a monolayer WO_xSe_y interlayer beneath the contacts and the other without. The former involves oxidizing WSe_2 before metallization, while the latter is achieved by oxidation after metallization. Both configurations rely on doping the channel region near the contacts to reduce the Schottky barrier width, facilitating charge carrier tunneling and reducing contact resistance. Additionally, inserting a monolayer WO_xSe_y between WSe_2 and the contacts diminishes metal-induced gap states, thereby lowering the

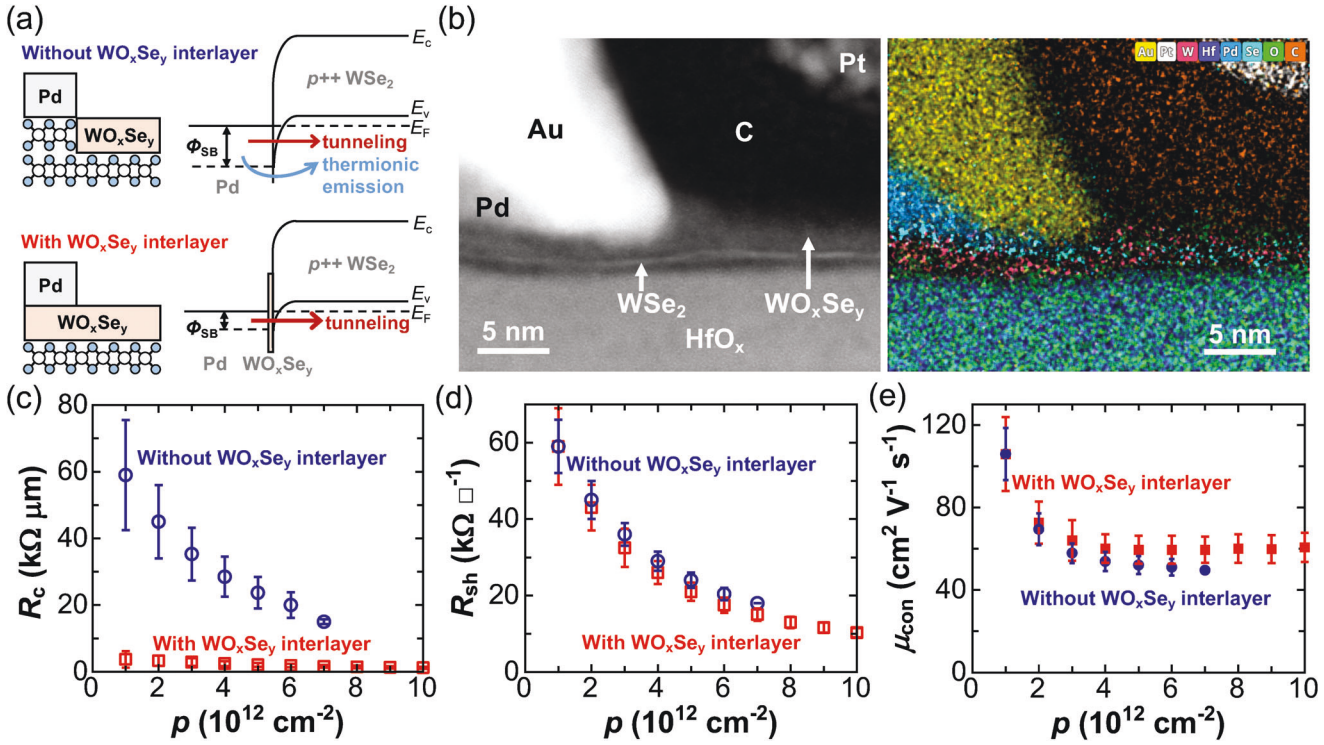

Figure 5. Contact resistance in WO_xSe_y-doped monolayer WSe_2 FETs with and without a WO_xSe_y interlayer. a) Schematics and band diagrams of WO_xSe_y-doped monolayer WSe_2 FETs without (top) and with (bottom) a WO_xSe_y interlayer between Pd and WSe_2. b) Cross-sectional HAADF-STEM image (left) of a WO_xSe_y-doped monolayer WSe_2 FET with a WO_xSe_y interlayer, and the corresponding STEM EDS image (right). Pt and C are used for protection during focused ion beam (FIB) cutting. c) Contact resistance R_c versus p. d) Sheet resistance R_{sh} of monolayer WSe_2 in source/drain extensions versus p. e) Conductivity mobility μ_{con} versus p.

Schottky barrier height. Figure 5b shows the cross-sectional HAADF-STEM and energy dispersive spectroscopy (EDS) images of a WO_xSe_y-doped monolayer WSe_2 FET with a WO_xSe_y interlayer. Interestingly, there is observable squeezing of the soft WO_xSe_y at the edge of the Pd/Au electrodes, suggesting that the amorphous WO_xSe_y interlayer also serves as a buffer that protects the underlying WSe_2 from distortion caused by the evaporated metal contacts. Figure S6 (Supporting Information) shows additional cross-sectional STEM images of the same FET, confirming complete and self-limiting oxidation of the topmost WSe_2 in both the channel and contact regions.

In comparison, a previous study found poor p-type performance in WO_x-doped WSe_2 FETs with oxidation before metallization.[43] Shown in Figure S7 (Supporting Information), we also observed inferior electrical performance of WO_xSe_y-doped monolayer WSe_2 FETs with oxidation before metallization, in agreement with that previous work. However, we leveraged the self-limiting nature of the oxidation process and re-oxidized these WO_xSe_y-covered monolayer WSe_2 FETs after metallization. This addition of the re-oxidization process fully restored the p-doping effect of WO_xSe_y and improved the electrical performance of WO_xSe_y-doped monolayer WSe_2 FETs with a WO_xSe_y interlayer beneath the contacts.

We used the transfer length method[63] (TLM) to extract and compare the electrode-extension contact resistances of WO_xSe_y-covered monolayer WSe_2 FETs with and without a WO_xSe_y interlayer under the contacts. Figure S8 (Supporting Information) shows the transfer curves, micrographs of the TLM structures, and the extraction of the contact resistance for each configuration. Figure 5c–e show the extracted electrode contact resistance R_c, extension sheet resistance R_{sh}, and conductivity mobility μ_{con} versus carrier density p, respectively.

Figure 5c shows that the R_c with interlayer WO_xSe_y ranged from 3.7 ± 2.5 kΩ μm to 1.2 ± 0.3 kΩ μm over a hole density of 10^{12}–10^{13} cm^{-2}, which is one order of magnitude lower than that without interlayer WO_xSe_y, ranging from 59 ± 17 kΩ μm to 15 ± 1 kΩ μm over (1–7)×10^{12} cm^{-2}. A separate study found an R_c of 40 kΩ μm for WO_xSe_y-doped monolayer WSe_2 at $p = 10^{13}$ cm^{-2} without interlayer WO_xSe_y,[32] aligning well with these results. Moreover, the R_c with interlayer WO_xSe_y shows a weaker dependence on carrier density compared to that without interlayer WO_xSe_y, indicating reduced Fermi-level pinning with a WO_xSe_y interlayer.[64]

In contrast, Figure 5d shows that R_{sh} of both configurations nearly overlap, with the same dependence on carrier density, despite the total resistances of these TLM structures differing by one order of magnitude (Figure S8, Supporting Information). This overlap indicates that i) the monolayer WSe_2 channel is pristine and homogeneous, and ii) the oxidation process is indeed self-limiting and does not damage the underlying layer. As shown in Figure 5e, the monolayer WSe_2 exhibited a high hole mobility of ≈60 $cm^2V^{-1}s^{-1}$ on a 3D oxide, suggesting minimal carrier scattering from WO_xSe_y doping and negligible damage to the underlying WSe_2 during oxidation.

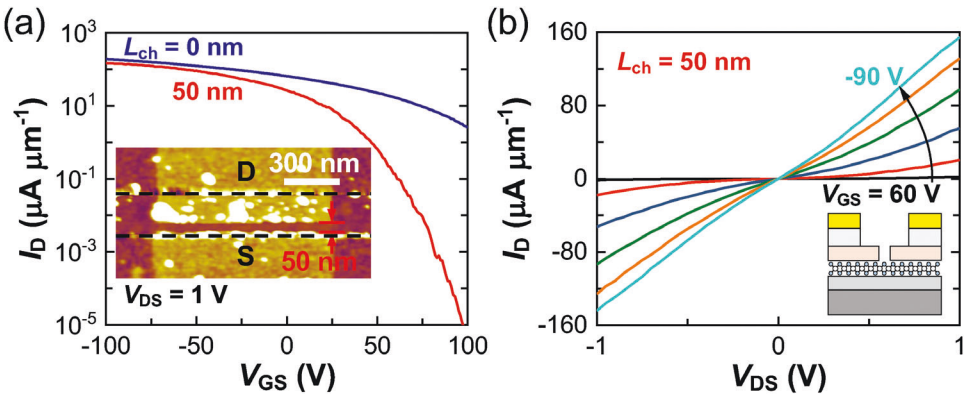

Figure 6. Electrical performance of a short-channel monolayer WSe_2 p-FET with WO_xSe_y-doped extensions (Device C). a) Transfer curves of the FET with L_{ch} = 0, 50 nm. V_{DS} = 1 V. Inset: AFM topography of the FET with L_{ch} = 50 ± 5 nm and L_{ext} = 150 ± 5 nm. The dashed black lines delineate the edges of the source and drain. b) Output curves of the FET with L_{ch} = 50 nm. Inset: Schematic of the FET.

Compared to other contact interlayers such as hBN,[59] TMD,[61] and amorphous TiO_2,[58] the WO_xSe_y interlayer is readily formed by CMOS-compatible self-limiting oxidation, with the potential to achieve wafer-scale uniformity. As shown in Figure S6 (Supporting Information), the WO_xSe_y contact interlayer was ≈1 nm thick, ≈1 nm thinner than the WO_xSe_y in the channel region. We hypothesize that the WO_xSe_y contact interlayer became thinner during the ebeam evaporation of Pd/Au contacts, as WO_xSe_y decomposes at elevated temperatures like 200 °C.[45,65] As with other ultrathin insulating contact interlayers,[58] the ≈1 nm WO_xSe_y contact interlayer still results in a Schottky barrier at the semiconductor-metal junction as a tunnel barrier. Further thinning of the WO_xSe_y contact interlayer is possible by in situ substrate heating or increasing the metal deposition power.

2.3. Short-Channel Monolayer WSe_2 p-FETs

Next, we combined extension doping with a WO_xSe_y interlayer under the contacts to fabricate high-performance short-channel monolayer WSe_2 p-FETs. **Figure 6** shows the a) transfer and b) output characteristics of an example FET with an L_{ch} of 50 ± 5 nm. Before SPL, the FET had an I_{max} of 189 μA μm^{-1}, an I_{max}/I_{min} ratio of 74, and a V_T of 48.1 V at V_{DS} = 1 V. After SPL, these values changed to an I_{max} of 154 μA μm^{-1}, an I_{max}/I_{min} ratio of 4 × 10^7, and a V_T of 12.8 V. As the channel length increased from 0 to 50 nm, I_{max}/I_{min} improved by 5 orders of magnitude, while I_{max} slightly decreased by 19%. Thus, the overall performance of the WO_xSe_y doped monolayer WSe_2 p-FET was optimized with sub-100 nm SPL. Figure 6b shows increased linearity of the I_D–V_{DS} curves as V_{GS} decreased from 60 to −90 V, suggesting a smaller Schottky hole barrier height with contact gating.

Figure S9 (Supporting Information) shows the transfer curves of two additional short-channel monolayer WSe_2 p-FETs with WO_xSe_y-doped extensions (Devices D and E), demonstrating similar performance.

2.4. Benchmarking

Finally, **Figure 7** benchmarks theses short-channel FETs (Devices C–E) against the state-of-the-art monolayer WSe_2 p-FETs, as summarized in Table S1 (Supporting Information).[3,8,23,32,57,66–72] Figure 7a shows the benchmarking of R_c versus p. In this work, WO_xSe_y doping with a WO_xSe_y interlayer reached a contact resistance to monolayer WSe_2 of 3.7 ± 2.5 to 1.2 ± 0.3 kΩ μm at a hole density of 10^{12}–10^{13} cm^{-2}. These values are about three times lower than the nearest comparisons, making them the lowest contact resistances at the same hole densities reported to date.

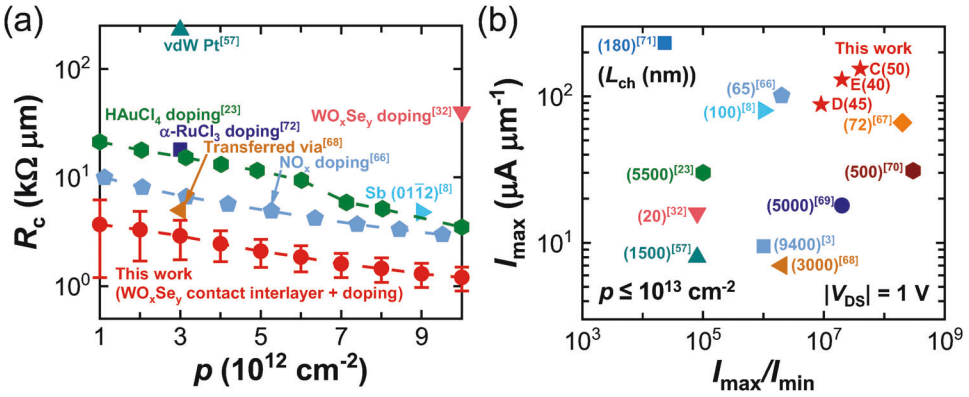

Figure 7. Benchmarking device performance of monolayer WSe_2 p-FETs. a) Benchmarking R_c versus p. b) Benchmarking I_{max} versus I_{max}/I_{min}. $|V_{DS}|$ = 1 V, and $p \leq 10^{13}$ cm^{-2}. L_{ch} is listed in parentheses for each data point.

Figure 7b benchmarks I_{max} at $|V_{DS}| = 1$ V versus I_{max}/I_{min}. To ensure a fair comparison, the upper limit of p was set to 10^{13} cm^{-2}. Devices C–E achieved performance comparable to the best monolayer WSe_2 p-FETs reported to date. To our knowledge, this study represents the first report of p-type extension doping for TMD monolayer FETs in the short-channel limit (Table S2, Supporting Information).

3. Conclusion

We demonstrated extension doping with low-resistance contacts for short-channel monolayer WSe_2 p-FETs by combining self-limiting-oxidation with damage-free nanolithography. WO_xSe_y doping, combined with an atomically thin amorphous WO_xSe_y contact interlayer, achieved record-low contact resistances for monolayer p-WSe_2 at a hole density ranged from 10^{12} to 10^{13} cm^{-2}. Short-channel monolayer WSe_2 p-FETs with WO_xSe_y-doped extensions exhibited some of the best I_{max} and I_{max}/I_{min} among TMD monolayer p-FETs.

To further enhance the performance of these short-channel monolayer WSe_2 p-FETs, several steps can be taken to potentially meet the technical targets for 2D transistors.[6] First, since R_c decreases with p, increasing p above 10^{13} cm^{-2} could reduce R_c below 1 kΩ µm. Second, the FET did not reach current saturation at a V_{DS} of 1 V even with an L_{ch} of 50 nm and an L_{ext} of 150 nm, suggesting the potential for higher current density by further reducing L_{ch} and L_{ext}. Finally, residue-contaminated WO_xSe_y exhibited restored p-doping through self-limiting re-oxidation, indicating the potential to implement WO_xSe_y-based extension doping in CMOS via resist-based lithography, including deep or extreme ultraviolet lithography, along with wafer-scale bilayer WSe_2 grown using chemical vapor deposition.[32]

4. Experimental Section

FET Fabrication: First, a WSe_2 flake (HQ Graphene) was obtained and transferred by gold-assisted large-area exfoliation[73] onto a 285 nm SiO_2/Si substrate. For all the FETs except the one shown in Figure 1c, SiO_2/Si was passivated with 5 nm HfO_x via atomic layer deposition before the transfer. HfO_x serves as an etch stop for the following channel patterning step. The contribution of 5 nm HfO_x to the gate capacitance is negligible (< 1%) compared to 285 nm SiO_2. Subsequently, the bilayer region of the WSe_2 was patterned into a 1-µm-wide ribbon using e-beam lithography (EBL) and XeF_2 etch. For the FETs without WO_xSe_y underneath the contacts, the contact electrodes consisting of 5 nm Pd/50 nm Au was deposited onto the bilayer WSe_2 using EBL, e-beam evaporation, and liftoff. Then we used tip-based cleaning to remove polymer residues on WSe_2 for homogeneous oxidation.[40,41] Afterward, a controlled remote O_2 plasma process (Tergeo plasma cleaner, PIE scientific; 50 W, 1 min, 0.5 sccm O_2; the same below) was used to convert the topmost layer of the WSe_2 channel into WO_xSe_y. For the FETs with WO_xSe_y underneath the contacts, the bilayer WSe_2 was oxidized before depositing the metal contacts. Finally, the FETs were re-oxidized after metallization to recover the p-doping of WO_xSe_y, using the same remote O_2 plasma recipe described above.

STEM Sample Fabrication and Measurements: Continuous and free-standing monolayer WO_xSe_y films were produced for STEM analysis by first transferring exfoliated monolayer WSe_2 onto holey TEM grids, and then oxidizing monolayer WSe_2 using remote O_2 plasma. Cross-sectional STEM samples were fabricated using standard FIB lift-out procedures with a FIB-SEM system (Helios 600i DualBeam, Thermo Fisher Scientific). The samples were imaged in an aberration corrected STEM (Themis Z, Thermo Fisher Scientific). The STEM imaging was operated at 300 kV at a semi-convergence angle of 18 mrad with a beam current of 30 pA for monolayer WO_xSe_y and 50 pA for cross-sectional STEM. Elemental maps were collected with a Super-X EDS detection system with a beam current of 200 pA.

XPS Measurements: XPS measurements were performed using a Kratos Axis Supra$^+$ Photoelectron spectrometer with an Al Kα X-ray source (1486.7 eV) and a concentric hemispherical analyzer. The analysis spot size was 55 µm in diameter. The carbon C 1s peak at 284.8 eV was used for binding energy calibration.

SPL and AFM Measurements: All SPL and AFM measurements were performed using an Asylum MFP-3D AFM system. For all SPL experiments with transistors, a normal force of 40–60 nN, and a tip speed of ≈10 µm s^{-1} was used. The SPL probes were single-crystal diamond probes (D80, Artech Carbon) with a tip radius of 10–30 nm and a spring constant of 3–4 nN nm^{-1}. Single-crystalline diamond probes were used for SPL to minimize re-deposition of WO_xSe_y. The density of scan lines was ≈1 nm per line, much smaller than the tip radius to ensure that the pile-ups of WO_xSe_y were completely removed from the scanned surface of WSe_2. After SPL, the SPL probe was replaced with a standard tapping-mode AFM probe (HQ:NSC15/AL_BS, MikroMasch) for imaging.

Raman and PL Measurements: Raman and PL measurements on a confocal Raman microscope (Nanophoton Raman 11) using a 532 nm laser with a 100× objective was performed. Raman spectra were obtained using a grating of 2400 l mm^{-1}. PL spectra were obtained using a grating of 600 l mm^{-1}.

FET Transport Measurements and Data Processing: We performed all FET transport measurements at room temperature in vacuum (10^{-4} Torr) using a semiconductor parameter analyzer (Agilent, 4155C). The threshold voltage V_T was extracted from the backward I_D–V_{GS} sweeps at V_{DS} = 1 V by linear extrapolation.[74] Hysteresis was calculated as the difference between the threshold voltages of backward and forward I_D–V_{GS} sweeps. Both TLM structures in Figure S8a,d (Supporting Information) have at least four channels and at least one each of the contact and channel resistance-dominated devices, validating the employment of TLM to extract R_c.[63] The overlap of R_{sh} in Figure 5d also confirms the extraction of R_c using TLM is accurate.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

S.C. conceived the project. Under A.M.v.d.Z., R.B., and W.P.K.'s supervision, S.C. performed material characterization, device fabrication, measurements, and data analysis. Under A.M.v.d.Z.'s supervision, Y.Z. prepared bilayer WSe_2. The manuscript was written through contributions

of all authors. All authors have given approval to the final version of the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

contact interlayer, contact resistance, scanning probe lithography, selective-area doping, short channel, tungsten oxyselenide, WSe_2

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