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Plasmonic Image Reproduction with Solid-State Superionic Stamping (S4)

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Abstract

Traditional top-down approaches for producing metallic nanostructures, despite being capable of producing arbitrary 2-D shapes, often use vacuum-based deep sub-micron lithographic fabrication technologies. This makes their use for single-use devices like chemical and bio-sensing substrates difficult to economically justify. Here, the authors demonstrate a manufacturing pathway that only uses such techniques to produce a master. This reusable master, coupled with a unique and facile electrochemical imprinting process, Solid-State Superionic Stamping (S4), is used to produce several replicated metallic nanostructures, thus demonstrating an economically feasible manufacturing pathway for single-use, nano-enabled devices.

This paper uses plasmonic image reproduction as an easy-to-visualize proxy for single-use devices such as plasmonic sensors and Surface Enhanced Raman Spectroscopy (SERS) substrates that require nanopatterned metallic structures. It demonstrates a process for replicating a picture by a set of metallic structures that plasmonically produce the desired colors locally. It uses a digitizing computational tool, direct-write Two-Photon Lithography (TPL) and a dry-etch process to rapidly produce a silicon master. This master is used to hot emboss nano-patterns in superionic glass blanks that, in turn, are used for electrochemical imprinting with S4 to reproduce the patterns on Ag substrates. The different steps in this process flow are described along with their role and effectiveness in contributing to a high-fidelity plasmonic image reproduction.

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Keywords: Plasmonics; Color generation; Metallic nanostructures; Hot embossing; Superionic conductor; Electrochemical etching; Nanoimprint lithography; Nanopatterning.

1. Introduction

With recent advances in nanofabrication technology, the possibility of generating colors by nano-scale structuring of a surface or plasmonic color generation has gained immense interest among researchers. In plasmonic color generation, color is generated by resonant interaction between the visible light and metallic nanostructures. Unlike conventional dye-based pigmentary coloring, plasmonic color generation approaches are not diffraction limited. Therefore, they are capable of very high spatial resolution. They are also less susceptible to aging. Plasmonic colors can be used in optical filters, high resolution microscopy, display technology, security and on-chip/board optical communications [1-3]. This paper uses plasmonic color generation as an easy-to-visualize proxy for exploring possibilities for economic manufacturing of single-use, sub-wavelength photonic sensing technology substrates [4, 5]. It reports a cost-effective and scalable CAD/CAM pathway for producing millimeter-scale images composed of a diverse set of colors generated plasmonically by metallic nanostructures. For such single-use, nano-patterned substrate manufacture, ultra-high vacuum processes like E-beam Lithography (EBL) or Focused-ion Beam (FIB) are not suitable because they are expensive, slow [6-11] and must be repeated in the fabrication of each unit produced. Solid-State Superionic Stamping (S4) is a facile and easy-to-implement ambient process, which is capable of high-throughput and low-cost production of centimeter-scale substrates with directly

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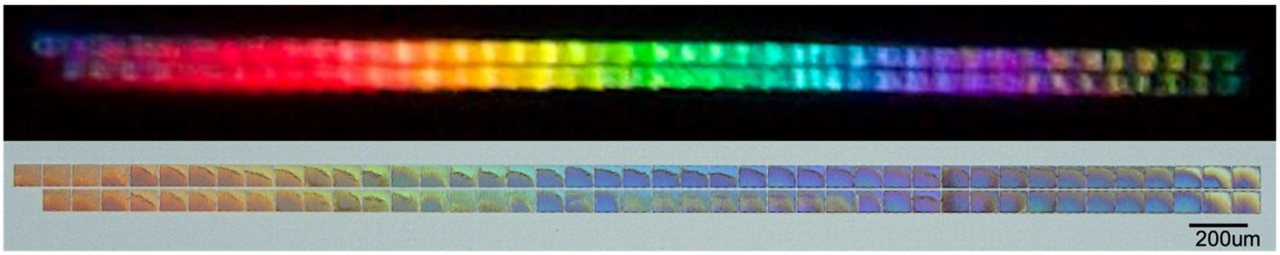

Figure 1. (Top) Optical image of the color palette and (bottom) confocal microscope image of these pixels with white light.

patterned transition metal (e.g., Ag and Cu) nanostructures [12-19]. Thus, S4 is well-suited for producing large-area plasmonic color generating substrates in a scalable, economical, and imprint-based manufacturing process.

In the S4 patterning process, an electrolytic cell is created with a cathode and an anode (the metal film to be patterned), and they are bridged by the superionic conductor (the stamp) whose nano-patterned surface is in contact with the anode. Anodic dissolution of the metal at the contact interface with the superionic conductor transfers the pattern from the stamp to the metal film (anode). A single nano-patterned stamp is thus capable of producing multiple replicas of the desired pattern in metal films. The detailed descriptions of stamp material and the plate-to-roll stamping set-up have been introduced in other papers [14-19].

The fabrication process for plasmonic color generating substrates begins with the production of a single master pattern in silicon (used for hot embossing the pattern into the superionic glass stamps). A commercial Two-Photon Lithography (TPL) platform is used to direct-write a mask on a silicon substrate. In this work, a python program for generating the mask for the master from a bit map of an arbitrarily selected image is introduced. This program file is used to drive Nanoscribe's Photonic Professional GT2 high-resolution TPL-based 3D printer to write a two-dimensional array of micron scale pixels. Each pixel consists of a grid of lines with nanoscale width, properly spaced to produce the corresponding color of the pixel. After that, this silicon substrate is etched using a dry etch process and used as a master for the reproduction process. The main advantage of using a computational approach is the flexibility it provides in transferring any selected image into a pixelated array of nanostructures. By changing the pixel size, the resolution and size of the master can also be changed. This work uses reproduction of an image (here, Henri Matisse's 'Cat with Red Fish', is taken as an example) as a 2.56 mm x 1.91 mm plasmonic image to describe the manufacturing pathway from the use of a software CAD/CAM tool for producing a silicon master to the use of the S4 process to electrochemically etch it into a thin silver film on a polymeric substrate.

Section 2 of the paper describes the software tool for generating line pattern program for the mask fabrication of the silicon master. Section 3 explains the transferring of the pattern from the silicon master to a solid electrolyte stamp by a hot embossing process. Section 4 of the paper is about the actual S4 stamping of plasmonic color generating substrates, and the fidelity analysis of the transferred patterns to produce the plasmonic replica. The number of stampings produced before the stamp shows signs of degradation and pattern deterioration is also analyzed. Finally, Section 5 provides the conclusions and directions for future research.

2. Computer Generation of Masters for S4 Image Replication

This section outlines the process of creating a silicon (Si) master for any chosen image. To achieve this, a python script is developed to import an image and generate a 'gwl' file, the format used for Nanoscribe's direct-write TPL machines. As previously mentioned, it maps the image into a two-dimensional array of micron scale pixels of straight lines with a predetermined spacing. When this array is printed by the Nanoscribe 3D printer, each pixel produces a specific color, based on the spacing of the lines within it. This is achieved in three steps: Image loader and pixel extraction, Color mapping, and Code file generation. The details of each step are as follows:

For the first task, using the *Image* module of Python Imaging Library (PIL), the python script imports the chosen image and converts it to an RGB bitmap. It then uses interval sampling to reduce the size of the image and map it to the desired pixel resolution. For example, for an original image of size 2118 x 1588 pixels, an interval of 17 pixels will produce a new image of size 126 x 94, and with a total of 11884 pixels. In the color mapping step, each pixel is mapped to a plasmonic pattern or 'plasmonic pixel' with the appropriate spacing of lines to generate the desired color. To achieve this, a color palette array, shown in Figure 1, is used. This color palette is generated using the same manufacturing pathway that is used for image reproduction. The color palette is comprised of 100 μm^2 plasmonic pixels with line spacings ranging from 230 nm to 430 nm in steps of 5 nm. As shown in Figure 1, this gives a palette of 40 different colors in the visible range, that are

Figure 2. (Left) Original Henri Matisse's "Cat with Red Fish" image, and (Right) simulated image using python codes.

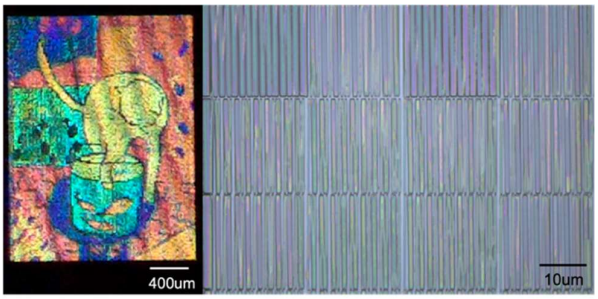

Figure 3. (Left) Optical white light image of the TPL pixelated photoresist masks after development. (Right) Optical microscope image of the patterns.

mapped to RGB using high resolution imaging. The python script performs color mapping by calculating the Euclidean distance in RGB space between a pixel in the picture and all the RGB colors present in the palette array, choosing the minimum as the match. To verify the working of this for the color approximation strategy, the script generates a new image (referred to as the simulated image) with selected color from the palette for each pixel. Figure 2 displays both the original image and the simulated image after the extraction and mapping processes has been completed.

For the code generation step, the script allows the user to input some initial parameters such as the pixel width and height, the separation between pixels, the laser power (for TPL writing), and initial stage positions, etc. With this information, the script creates the gwl program for TPL writing. The user-supplied information is used to first generate the initialization gwl code, and the pixels of the picture are scanned with the script using a pixel writing function to generate the gwl code for TPL writing of each plasmonic pixel with the appropriate line spacing. The Algorithm 1 shows the algorithm for the generation of Nanoscribe code (gwl file):

Algorithm 1 Generation of Nanoscribe code

masterGen($filename_i, filename_o, interval$)
  $I \leftarrow Image.open(filename_i)$
  $I_{RGB} \leftarrow I.convert(RGB)$
  $S \leftarrow I_{RGB}.size\ /\ interval$
  $I_{out} \leftarrow Image.new(S)$
  $x_{pos} \leftarrow gwl.WIDTH\_PIXEL + gwl.SPACE\_BTW\_PIXEL$
  $y_{pos} \leftarrow gwl.HEIGHT\_PIXEL + gwl.SPACE\_BTW\_PIXEL$
  $P_{img} \leftarrow open(filename_o, 'w')$
  $j \leftarrow 0$
  for $y \leftarrow 0$ to $I_{RGB}.height$ with $interval$ **do**
    $i \leftarrow 0$
    for $x \leftarrow 0$ to $I_{RGB}.width$ with $interval$ **do**
      $pixel \leftarrow I_{RGB}.getPixel(x, y)$
      $color_{pixel} \leftarrow color.closestColor(pixel)$
      $I_{out}.putpixel((i, j), color.COLORS[pixel])$
      $pitch \leftarrow color.COLOR\_SPACING[color_{pixel}]$
      $placed_{pixel} \leftarrow gwl.placePixel(x_{pos}, y_{pos}, pitch)$
      $P_{img}write(placed_{pixel})$
      $x_{pos} \leftarrow gwl.WIDTH\_PIXEL + gwl.SPACE\_BTW\_PIXEL$
      $y_{pos} \leftarrow 0$
      $i++$
    $x_{pos} \leftarrow -1 * (gwl.WIDTH_{PIXEL} + gwl.SPACE_{BTW_{PIXEL}}) * (i - 1)$
    $y_{pos} \leftarrow -1 * (gwl.HEIGHT_{PIXEL} + gwl.SPACE_{BTW_{PIXEL}})$
    $j++$
  $P_{img}.close()$
  $gwl.createFinalGWL(filename_o, S)$

For this work, a plasmonic pixel with dimension 20 μm x 20 μm and pixel separation of 0.3 μm was selected. The total dimension of the image is then 1.9079 mm x 2.5575 mm in length and width, respectively. TPL parameters selected were 24 mW laser power, and 7 mm/s writing speed. The generated code was directly input to the Nanoscribe 3D printer. The results of the mask-write process are shown in Figure 3.

A dry etch process, Reactive Ion Etch (RIE) was used to produce an all-silicon master. The detailed process is introduced in the previous research [20]. Figure 4 shows the image of master after 2 mins CF_4 dry etching in an Axic Reactive Ion Etching (RIE) system.

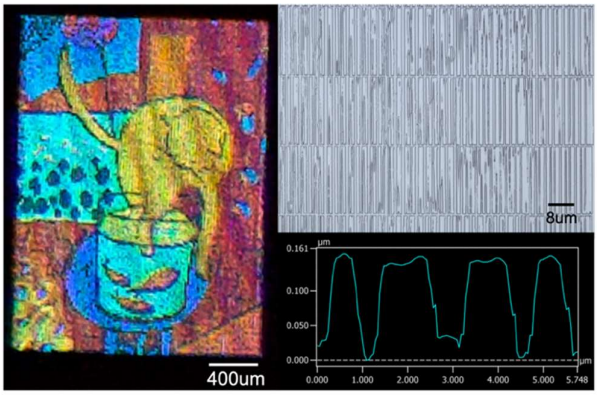

Figure 4. (Left) Optical white light image of the silicon master after RIE. (Right top) Confocal microscope image. (Right bottom) Line scanning of the pattern depth (150 nm).

3. Two-Steps Hot Embossing of S4 Stamps

Previous papers [14-19] has introduced the S4 process, the stamp materials, and different process formats. This process uses a superionically conducting glass mixture, Silver Iodide-Silver Metaphosphate mixture ((x)AgI-(1-x)$AgPO_3$, x=0.5) as the stamp material for S4 etching of silver because of its high faradaic efficiency and its ease of processing. This glassy electrolyte has good mechanical properties in terms of hardness and wear resistance, is transparent for overlay registration in imprinting, is chemically stable, and has a low glass transition temperature for easy processing into nano-patterned stamps. The S4 process has been implemented in different formats, as a pure stamping (Plate to Plate or P2P) or a roll-on (Plate to Roll or P2R) process to take advantage of the ability to make stamps in AgI-$AgPO_3$. Because the P2R process format relies on a moving line contact between the stamp and the silver film being etched, it is less demanding on stamp flatness than the pure stamping process with demands for conformal contact across the stamped surface. Producing flat stamps with a hot-embossing process is generally challenging. During subsequent cooling, the embossed surface develops a negative curvature (i.e., becomes concave) because of contraction of the interior, making conformal contact with the stamped substrate impossible. Previous papers [16, 19] report on techniques

developed for producing flat and large-area (10 mm diameter) stamps, that control the cooling rates and the temperature gradient within the stamp to improve the curvature of stamp surface. Here, a two-step hot-embossing process is developed to achieve more flat and even convex shaped stamp surfaces.

The first hot embossing is on the non-patterned (flat) prime wafer. The wafer is pre-heated to 100 °C, while the stamp holder with AgI-$AgPO_3$ stamp is brought to a temperature of 75 °C. Next, the stamp is pressed against the prime wafer with a force of 100 N (22.5 lbf) until the desired stamp surface area is achieved at the contact interface. During this time, the temperature of the wafer is maintained slightly above the glass transition temperature (~80°C) of AgI-$AgPO_3$ glass mixture, so that softening and viscoelastic spreading only occurs close to the stamp-wafer interface. Once the spread of AgI-$AgPO_3$ glass reaches the desired diameter (10 mm), the applied force is reduced to 2.2 N (0.5 lbf), and the whole system is allowed to relax at constant temperature for 3 minutes. This step is necessary for AgI-$AgPO_3$ glass to release the viscoelastic stresses developed in it before it is allowed to cool at a rate of 1.5 °C/minute. When the wafer temperature drops to 75 °C and the temperatures across the set-up equilibrate, the applied load is removed, and the stamp is retracted from the wafer and the entire set up is allowed to cool to room temperature. At this point, a pre-made flat stamp is achieved and is ready for the next stage where a pattern is embossed on its surface with a second hot embossing step.

The flat prime wafer is now replaced with the patterned master, which is now heated to a temperature of 90 °C. (slightly above the glass transition temperature of the stamp). And the stamp holder with AgI-$AgPO_3$ glass stamp, similar to the previous step, is heated to 75 °C. Then, a force of 22 N (5 lbf) is applied between the stamp and the master to make conformal contact between the two. After this, the stage holding the stamp is gradually and precisely moved through a range of 2 μm, pressing the stamp into the master, since the pattern depth is only 150 nm. Next, the applied force is reduced to 2.2 N (0.5 lbf), and the whole system is set to relax for 5 minutes. Then, the master is cooled at the same rate of 1.5 °C/minute and retracted from master when the temperature drops to 75 °C. The second hot embossing step is effective in releasing the viscoelastic stresses that accumulate in the stamp during the flattening step. Figure 5 shows transition of stamp surface shape from concave to flat to mildly convex for single and two-step hot embossing. Also, higher master temperature and longer relaxation time have been observed to help improve the surface curvature more.

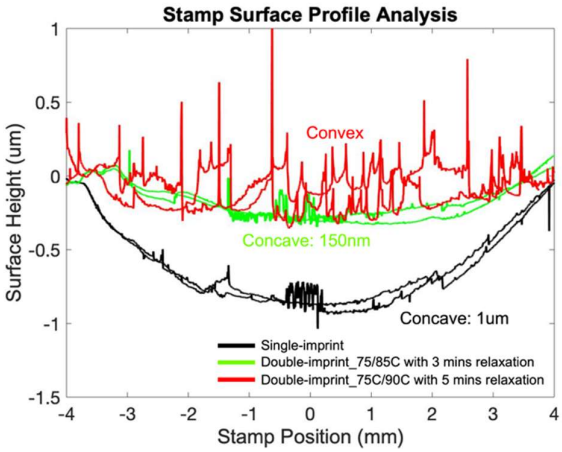

Figure 5. Stamp surface shape profile transition from concave to convex for the single and double hot embossing process.

Figure 6 shows a white light image of the stamps made using this new protocol. The stamp surfaces clearly shows that the 'Cat with Red Fish' pattern is transferred from the silicon master to AgI-$AgPO_3$ glass stamp surface with a high degree of fidelity and the pattern depth is around 150 nm.

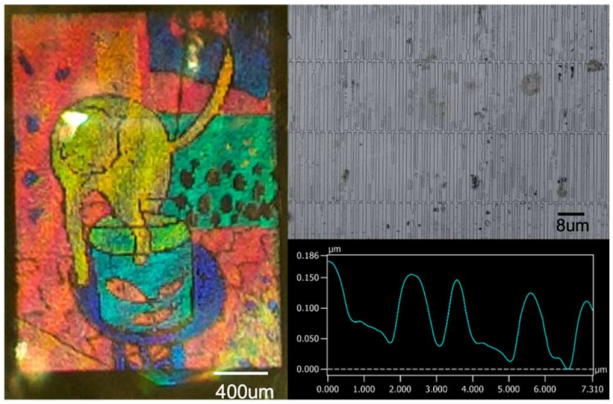

Figure 6. (Left) Optical white light images of the stamp surfaces that result from using the S4 hot embossing. (Right top) Confocal microscope image. (Right bottom) Line scanning of the pattern depth (150 nm).

4. Stamping Plasmonic Images on Silver Substrates with P2P S4.

This section introduces a plate-to-plate S4 patterning configuration [14-19] (Figure 7) to reproduce the plasmonic image on a silver coated polyimide adhered to a glass slide. Polyimide tape is chosen as the flexible substrate because of its good flexibility, vacuum compatibility and chemical stability. Furthermore, it does not react with the AgI-$AgPO_3$, even at elevated temperatures. The single-sided polyimide adhesive tape is adhered to a glass slide and then cleaned with oxygen plasma to remove organic residue. A Thermionics 4-Pocket e-beam evaporator is used to deposit a 1 μm thick Ag film on the polyimide tape. A relatively slow deposition rate (< 0.3 nm/sec) is used to obtain a smooth and high-quality film.

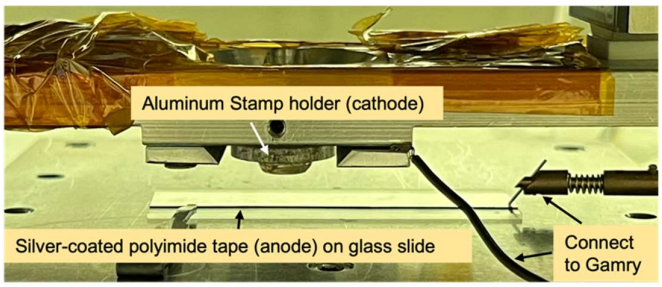

Figure 7. Schematic of S4 plate-to-plate (P2P) etching process.

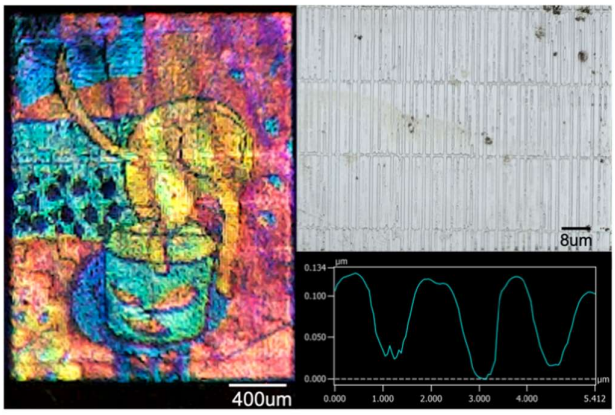

Figure 8. (Left) Optical white light images of the pattern on Ag substrate after S4 P2P etching with 0.5 V. (Right top) Confocal microscope image. (Right bottom) Line scanning of pattern depth (130 nm).

The plate-to-plate (P2P) process is implemented on an Aerotech precision 3-axis positioning stage. The silver coated polyimide substrate is mounted on the movable table of the stage and acts as anode. The AgI-$AgPO_3$ glass stamp is connected to the z-axis of the stage, with its aluminium holder acting as the cathode. The AgI-$AgPO_3$ glass stamp is lowered to the table, bringing it in contact to the silver film with the contact force of 30 N (6.5 lbf). A Gamry Reference 600 Potentiostat working in the galvanostatic mode is used to provide a controlled voltage input to the electrolytic cell developed between the aluminium stamp holder, the stamp and the silver film. A constant voltage supply of 0.5 V, which is slightly higher than the activation voltage (0.3 V) of AgI-$AgPO_3$ glass, is chosen to overcome voltage drops at contact interfaces. This voltage is not high enough to initiate side reactions in the glass. The overall P2P etching time is 15 minutes, and the process stops when the current in the cell drops to a value below 50 μA, indicating that most of the excess silver has been etched away and the contact interface has reached the polyimide tape surface. Figure 8 shows the result of the pattern on silver film after P2P process. The optical micrograph shows the plasmonic image transferred to the silver substrate with a high degree of fidelity. The confocal microscope image and the profile scan clearly show the line patterns of the pixels in the image. To assess the fidelity of pattern transfer, scanning electron micrographs (SEM) of similar regions of master and the stamped plasmonic image were compared. Figure 9 shows the SEMs comparison of the patterns on Si master and the stamped silver film. It is clearly seen that the line width and spacings are transferred with a high degree of fidelity.

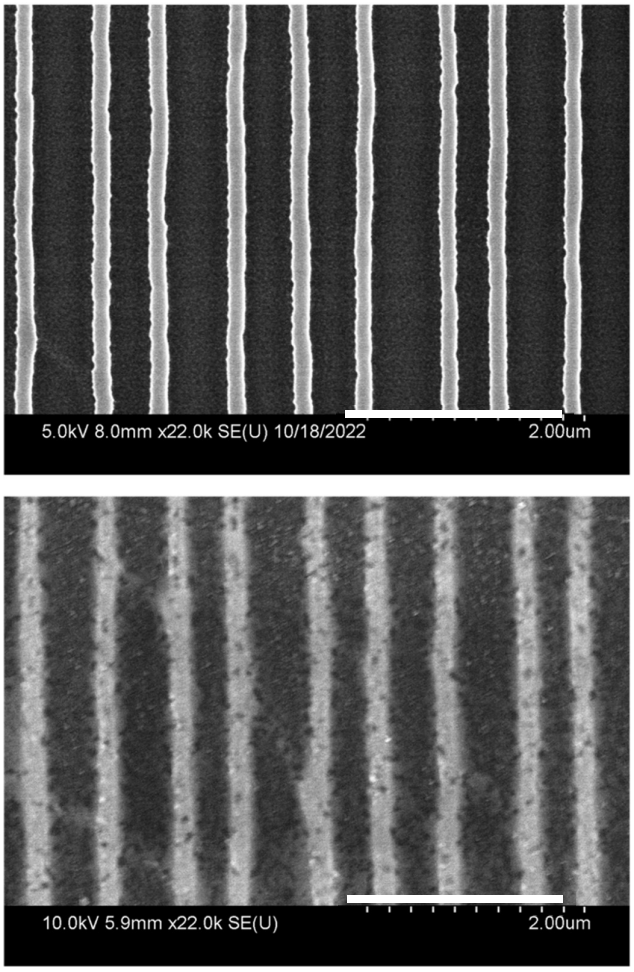

Figure 9. SEMs comparison of the line spacing on the Si master (top) and the stamped silver film (bottom).

Finally, to assess the durability of the stamps, several stamping cycles were conducted, and the resulting patterns were analysed. Figure 10 shows an optical image of the pattern produced in the fifth stamping cycle, which can be compared to that of the first stamping cycle shown in Figure 8. The details and resolution of the printed image have clearly been preserved. Some deterioration/blemishes are observable near the edges along with some darkening of the image. This is due to mechanical wear and environmental dirt. Proper selection of variables (lower voltages and etch rates, see ref [16, 20]) can slow down the stamp wear and permit around 30 stamping cycles.

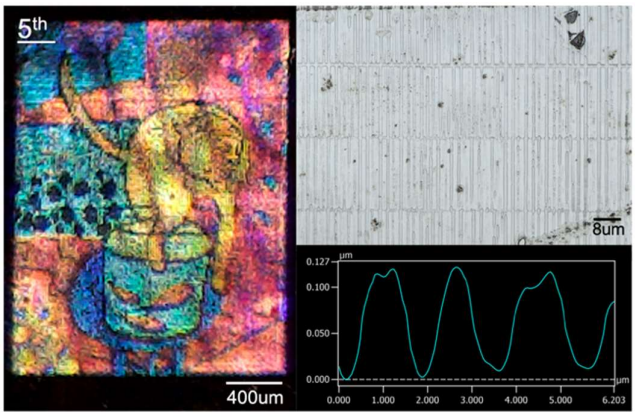

Figure 10. (Left) Optical white light image of the pattern on Ag substrate after S4 P2P etching with 0.5 V after 5th print. (Right top) Confocal microscope image. (Right bottom) Line scanning of the pattern depth (130 nm).

5. Conclusions and Future Work

This paper has demonstrated the feasibility of electrochemically ‘stamping’ plasmonic color images on to substrates with evaporated silver thin films. This is achieved by combining computational tools to transform an image to an array of plasmonic pixels with a novel manufacturing pathway

constructed around Solid-state Superionic Stamping (S4). The entire manufacturing pathway was developed, including tooling design to the production of the color stampings. This novel pathway has several important features:

- It uses a master, to decouple the actual production of color stampings from expensive, long lead-time cleanroom processes, thus enabling economical volume production.
- The making of the master uses a nanoscale direct-write process, Two-photon Lithography (TPL), making it possible to pattern and fabricate a master in a single day.
- The computational tool, coupled with the Nanoscribe 3D printer, greatly simplifies and automates the realization of the silicon master for making glass stamps.
- The two-step hot-embossing process to transfer the pattern from the master to the stamp, while keeping stamp surface profile flat permits a simple P2P (stamping format) and larger stamp area for S4 plasmonic image reproduction.
- The glassy superionic conductor (solid electrolyte), AgI-$AgPO_3$, as a stamp material, is chemically stable in ambient conditions, and has a low glass transition temperature permitting easy nano-patterning of its surface by hot embossing. It can be used for several stamping cycles and optimization of process parameters can lead to upwards of 30 stampings. Furthermore, the stamp surface can be flattened/resurfaced and re-patterned using the same hot-embossing process for reuse. Thus, a single stamp would be able to produce hundreds of stampings before it is fully consumed.
- Once the master is produced, the manufacturing pathway involves all solid-state processes. There are no process effluents and S4 has a high Faradaic efficiency, suggesting an environmentally friendly manufacturing pathway.

These features make the manufacturing pathway demonstrated in this paper economically and technologically scalable, suggesting the feasibility of its use for several high-value applications including plasmonic bio-sensing and SERS substrates.

In terms of future work, the fabricating higher resolution, larger area patterns using different plasmonic structures (pillar or pyramids) needs to be explored. Clearly, process optimization to obtain improved working life of the stamp is also an important next step. Finally, after the optimization of the process for stamp durability, it should be able to work out the economics of the entire manufacturing pathway to complete the development of this process and demonstrate its economic feasibility.

Acknowledgements

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