Heterogeneous Integration of Biasing Circuits for mmWave Reconfigurable Intelligent Surfaces

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***Abstract*—We present the design of a biasing circuit and interposer architecture for scalable millimeter wave (mmWave) reconfigurable intelligent surfaces (RISs). Specifically, a multi-layer biasing board is designed to provide the necessary excitation of a 1-bit RIS. Ball grid array (BGA) technology is leveraged to integrate heterogeneous technologies and materials to provide more real estate on the RIS metasurface and more design flexibility. Fabrication and assembly challenges associated with this novel technique have been identified and recommendations for future fabrication/assembly are provided.**

Keywords—reconfigurable intelligent surfaces, biasing circuits, mmWave, metasurface

I. Introduction

Reconfigurable intelligent surfaces (RISs) have gained a lot of attention in recent years due to their dynamic beamforming capabilities, low profile, and ease of implementation. Tunable devices, including PIN diodes, varactors, MEMS etc., are generally integrated within the metasurface unit cell to achieve electronic beam reconfiguration [1]. Such devices, however, need biasing circuitry to drive them. This can be accomplished with the use of a driver-integrated circuit controlled by a microcontroller unit (MCU) or Field Programmable Gate Array (FPGA). Additionally, shift registers are usually employed due to their ability to be cascaded in series and be controlled with common digital output pins from an MCU or FPGA. On the other hand, providing individual biasing control for every unit cell poses integration challenges due to the complex biasing circuitry required as well as the limited real estate per unit cell, especially at higher mmWave frequencies. Several approaches use a single multilayer PCB to integrate both the metasurface (typically on the top surface) and the biasing circuitry (bottom) [2]-[3]. The connection between the layers is facilitated through vias. Although this is an attractive approach from a complexity viewpoint, it limits the available area per unit cell because the metasurface components are located on the top side of the RIS (e.g., radiating patch, switch/varactor). This can be a bottleneck if more switches and associated circuitry are needed for multi-bit phase modulation.

In this work, we are using BGA technology to integrate the biasing board and metasurface, thus making the back side of the metasurface board usable to integrate more mmWave circuitry. Specifically, the metasurface consists of two Rogers R4003C low-loss substrates (ϵ_r = 3.55, tan δ = 0.0027, thickness = 0.508mm), radiating patches (top board) and biasing circuitry, and PIN diode switch on the back side [4]-[5]. MACOM MADP-000907-14020 PIN diodes are used as the active elements to control the beam scanning angle.

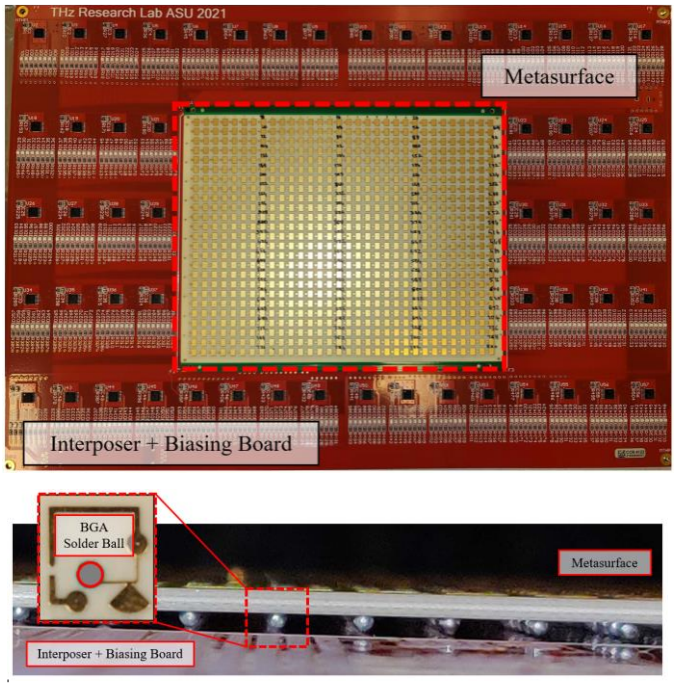

Figure. 1. The RIS consists of metasurface and biasing boards: Top view of the RIS (top), and the metasurface and biasing boards are integrated using BGA (bottom).

A 1-bit topology (1 PIN diode per unit cell) is adopted which reduces power consumption and losses. A six-layer FR4 board hosts an interposer and the biasing electronics (e.g., shift registers). The two boards are assembled together using BGA technology, as shown in Fig. 1. On the other hand, the biasing circuit board is implemented as a 6-layer board with all biasing components on the top and bottom layers, with the footprint of the metasurface on the top layer (as depicted in Fig 1), ground plane as the second layer, clocks and other signals routed on the third and fourth layer, and power plane in the fifth layer. To accommodate signal routing and maximize board space, all layers were utilized, and unique copper pours were created to allow routing in the power and ground plane layers.

II. RIS Biasing Board Design And Fabrication

We performed the design of the proposed biasing board in Altium Designer by expanding a recent work in [6]. The configuration is expanded to four shift registers in cascade, to control 800-unit cells and maximize switching speed. The biasing board is designed as a 6-layer board in FR4 substrate with the dimensions of 350 mm × 245 mm. The BGA pitch is 5 mm with 1 mm pads on the biasing board. A layout was

generated from Altium with all shift register drain outputs routed to all 800 unit cells on the metasurface and the clock signals were routed to interface to the MCU. Then the power signals were routed to the metasurface as signal planes. The metasurface and biasing boards were fabricated using standard PCB manufacturing processes. A custom assembly process was developed based BGA technology, to connect the boards together. To ensure proper alignment of the metasurface to the biasing board, mounting hardware (M0.6 screws and nuts) were utilized in the assembly process. The thin substrates (< 1.2 mm) combined with the large surface area of the metasurface lead to warpage and bowing after fabrication, which further worsened after the assembly process due to multiple passes through the reflow oven.

III. System Characterization

RF testing was carried out to evaluate the effect of BGA assembly on the RIS beamforming. To characterize the assembled prototype, the bistatic Radar Cross Section (RCS) is measured using a quasi-optical measurement setup. As shown in Fig. 2, the setup consists of mmWave transmitter (signal generator) and a receiver (spectrum analyzer) both coupled to horn antennas. To ensure constant phase front illumination of the electrically large RIS, we used a 20 cm Teflon collimating lens in front of the transmitter antenna. To capture the scattered fields the receiving horn antenna is fixed at 5 m in front of the RIS. The collimated beam from the lens is used to uniformly illuminate the metasurface. The transmitter is rotated radially from [-20˚, -70˚] to [+20˚, +70˚] around the center of the metasurface to measure the RCS. For accuracy and repeatability, the whole setup was mounted on an optical breadboard. The scan angle range is limited due to lens blocking the receiver near the broadside (indicated with grey area in Fig. 2). Fig. 2 shows the comparison between the analytical and measured normalized RCS pattern of the RIS at 28 GHz. As it can be observed, the proximity of the metasurface board to the biasing board as well as the BGA connecting them does not alter the beamforming characteristics. As expected, only one main beam appears at +30° direction and has good agreement with the analytical results. The discrepancy in the side lobe level is attributed to the multiscattering in the surrounding objects.

IV. Con clusion

We presented a novel approach for assembling the metasurface and biasing circuitry using heterogeneous technology which could reduce the complex wired connections. A six-layer biasing board was designed with a custom footprint to mount the metasurface board using BGAs. However, some challenges were encountered in terms of bow and warpages, suspected to be largely attributed to the size of the boards and the thin nature of the substrates employed in this work. Some countermeasures would be to use thicker substrates, and reduce the board size (e.g., splitting the design into multiple sub-arrays) could serve as potential alternatives for this promising approach, although, a thorough investigation is needed for future implementations. Furthermore, the footprint of the biasing board can be reduced to match the area of the metasurface with no troubleshooting components in future optimized layouts.

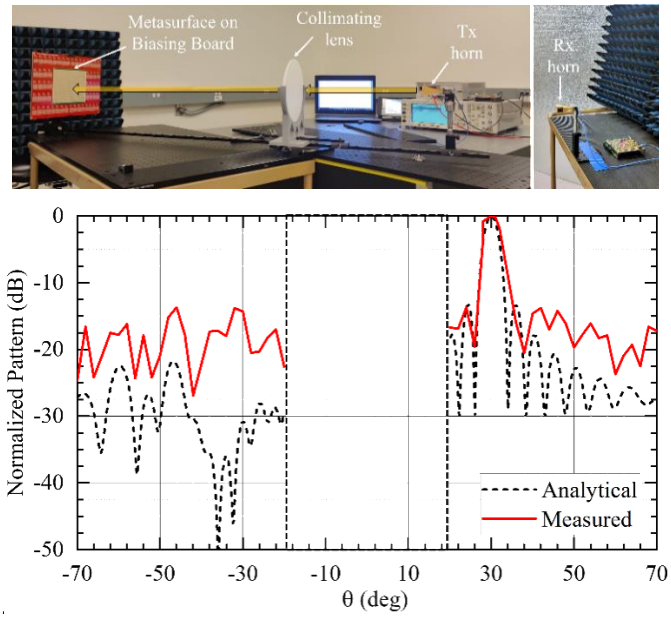

Fig. 2. (Top) Measurement setup used for the characterization of the 1-bit metasurface integrated on the biasing board. (Bottom) Comparison of analytical and measured results as a function of the scan angle θ at 28 GHz for a metasurface implemented with random pre-phasing technique [8].

Successful integration of the metasurface and biasing boards could provide sufficient real estate to accommodate multi-bit phase shifting using PCB-compatible fabrication methods.

References

[1] S. V. Hum and J. Perruisseau-Carrier, “Reconfigurable reflectarrays and array lenses for dynamic antenna beam control: A review,” IEEE Trans. Antennas Propag., vol. 62, no. 1, pp. 183–198, Jan. 2014.

[2] H. Kamoda, T. Iwasaki, J. Tsumochi, T. Kuki, and O. Hashimoto, “60-GHz electronically reconfigurable large reflectarray using single-bit phase shifters,” IEEE Trans. Antennas Propag., vol. 59, no. 7, pp. 2524–2531, 2011.

[3] J. -B. Gros, V. Popov, M. A. Odit, V. Lenets and G. Lerosey, "A Reconfigurable Intelligent Surface at mmWave Based on a Binary Phase Tunable Metasurface," in *IEEE Open Journal of the Communications Society*, vol. 2, pp. 1055-1064, 2021, doi: 10.1109/OJCOMS.2021.3076271.

[4] Aditya S. Shekhawat, Bharath G. Kashyap, Panagiotis C. Theofanopoulos, Anand Pratap S. Sengar and Georgios C. Trichopoulos, Compact Unit-Cell Design for mmWave Reconfigurable Intelligent Surfaces,” 2022 United States National Committee of URSI National Radio Science Meeting (USNC-URSI NRSM), 2022, pp. 1-2.

[5] A. S. Shekhawat, B. G. Kashyap, B. Tjahjadi and G. C. Trichopoulos, "Beamforming Characterization of a mmWave Single-bit Reflective Metasurface," 2022 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (AP-S/URSI), 2022, pp. 1608-1609, doi: 10.1109/AP-S/USNC-URSI47032.2022.9886912.

[6] G. C. Trichopoulos et al., "Design and Evaluation of Reconfigurable Intelligent Surfaces in Real-World Environment," in IEEE Open Journal of the Communications Society, vol. 3, pp. 462-474, 2022, doi: 10.1109/OJCOMS.2022.3158310.

[7] B. G. Kashyap, P. C. Theofanopoulos, Y. Cui and G. C. Trichopoulos, "Mitigating Quantization Lobes in mmWave Low-Bit Reconfigurable Reflective Surfaces," in IEEE Open Journal of Antennas and Propagation, vol. 1, pp. 604-614, 2020, doi: 10.1109/OJAP.2020.3034049.