Understanding Error Sensitivity of Quantum Circuits

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***Abstract*—Quantum computing is an emerging technology that is poised to revolutionize computational capabilities. However, errors from environmental noise and imperfect hardware can significantly affect the fidelity of the computational results of quantum circuits. In this paper, we put forth a hypothesis that similar to classical computers, not all errors have the same effect on the outputs.**

To study the error impact at different qubits and at different gates, we leverage the fault injection methodology from a recently proposed framework, QuFI [1], which was designed to produce a quantum vulnerability factor (QVF) heatmap based on all possible fault injections. In our work, we use a similar fault injection approach but focus on the impact of errors at different regions of a circuit. Then, we propose to apply error mitigation techniques selectively to protect the most vulnerable regions of a circuit so as to reduce the overhead of error mitigation schemes.

***Index Terms*—Quantum, Error Sensitivity, Fault Injection**

I. Introduction

Quantum computing represents a paradigm shift in computational theory and practice, promising unprecedented computational power and transformative capabilities for solving complex problems that are intractable for classical computers. At the heart of this revolutionary technology lies the qubit, the fundamental unit of quantum information. Unlike classical bits, which can only exist in one of two states (0 or 1), qubits exploit the principles of quantum mechanics to exist in a superposition of both states simultaneously, exponentially expanding the computational possibilities.

Quantum computers, however, are less reliable compared to classical computers. The first reason is that qubits are inherently vulnerable to retention error. This error is either caused by the qubit losing energy and decaying to the spin 0 state from the spin 1 state or by external interference like other qubits. Second, recent publications have shown that qubits constructed from superconducting technologies are also susceptible to external radiation [2], [3]. This reduces the reliability of quantum computers as ionizing particles reduce the noise tolerance [4], [5]. These kinds of external perturbations are not as sensitive in classical computers that employ CMOS transistors. Additionally, the qubit state is also modified by light particles like muons [5] and infrared lights [6]. Furthermore, errors in quantum computers are much more complex to resolve than in classical computers. While the classical computer has just 0 or 1 state for its bits, a qubit has its state situated in the Bloch sphere. A tiny amount of rotation in the Bloch sphere can be propagated along the circuit making it harder to pinpoint the issue. This means a simple fault injector to flip from state 0 to state 1 is not enough to gauge the effect on the quantum circuit.

Previous works on quantum fault injection tackle these issues by calculating a vulnerability score for the entire circuit based on a particular type of fault that is injected [1]. Our paper makes use of their fault injection methodology but focuses on vulnerability analysis of each region of the circuit instead of the whole circuit. By identifying the vulnerable regions of the circuit, measures can be taken to protect that region using error mitigation or error correction techniques. In this work, we employ Pauli Error Sandwiching to protect the vulnerable regions of the circuit. Additionally, we take a deep dive into some popular benchmarks to qualitatively reason the cause of their vulnerability.

In this paper, we make the following contributions: (1) We extend the idea from the existing work on quantum circuit fault injection [1] to examine the sensitivity of errors at different gates and different qubits in a quantum circuit. (2) We analyze the circuits under our study to reveal insights into why these circuits are vulnerable/robust to different errors. (3) We propose to apply error mitigation selectively to protect the most vulnerable part of the circuit.

The rest of the paper is organized as follows. Section II summarizes the noise encountered in quantum computers, provides the background on the error mitigation technique, Pauli Check Sandwiching, and discusses the related works. Section III describes our methodology for fault injection and selective error mitigation. Section IV presents our results for different types of faults injected in representative benchmarks and analyzes the reasons for their vulnerability. Section V concludes the paper.

II. Background and Related Works

A. Quantum Noise

The current capabilities of quantum computers are limited by the inherent noise in the quantum computer. The errors in a quantum computer can be divided into two categories:- Coherence errors [7] and Operation errors.

Coherence error is caused because a qubit can retain its state only for a limited amount of time. This retention issue can take one of two forms. Either a qubit in a high energy state loses its energy and transitions to a low energy state (T1 error) or other qubits and external environment can cause a qubit to change its state (T2 error) [8].

The relaxation time T_1 dictates the decay rate for a qubit in state $|1\rangle$ to state $|0\rangle$ and is given by the equation,

$$P_{|1\rangle}(t) = P_{|1\rangle}(0)e^{\frac{-t}{T_1}} \tag{1}$$

Here,$P_{|1\rangle}(t)$ is the probability of the qubit being in state $|1\rangle$ at time t [9]. At $t = \infty$ the probability that the qubit will decay to state $|0\rangle$ is 1. A similar equation is present for the T2 relaxation time, which dictates the change of the phase information for a quantum state.

To tackle these errors, work is done to improve the qubit technology and incorporate error mitigation and error correction techniques.

B. Pauli Check Sandwiching

As discussed in Section I, after we obtain an error map representing the vulnerability in the circuit, our next job is to protect those most vulnerable areas. For the purpose of this paper, we have employed Pauli Check Sandwiching (PCS) [10]. PCS provides multiple advantages, one of which is less resource overhead when we selectively protect a certain region of the circuit.

Consider the unitary operation U, which we aim to protect in the circuit, PCS requires an extra ancilla qubit and two controlled gates C_1 and C_2, such that :

$$C_1 = C_1' \otimes |1\rangle\langle 1| + I \otimes |0\rangle\langle 0| \tag{2}$$

$$C_2 = C_2' \otimes |1\rangle\langle 1| + I \otimes |0\rangle\langle 0| \tag{3}$$

and

$$C_2' U C_1' = U. \tag{4}$$

The ancilla qubit is sandwiched between two Hadamard gates and the result of the measurement is discarded when the ancilla qubit reads 1. This is because if there is an error present in the region that we are protecting, the ancilla qubit will read 1 as the two controlled gates and the two Hadamard gates do not cancel each other and will change the state of the ancilla qubit. An example of the PCS-protected region in a QAOA circuit is shown in Figure 2.

C. Related works

Previous works on quantum fault analysis focused on noise and fault modeling. Recently, a fault injector framework, QuFI [1], was proposed to track the effect of fault propagation. To model the fault injector, the U gate was used as the injector as it is the most flexible when it comes to modeling phase shifts of different magnitudes. QuFI provided a Quantum Vulnerability Factor (QVF) score to the entire circuit for different configurations of the U gate.

In our work, we adopt this fault injection methodology to assign an error sensitivity score to each region (e.g., one gate upon a single qubit) of the circuit. This helps pinpoint the most vulnerable region of the circuit. Upon identifying the vulnerable region, we use PCS to detect and mitigate the errors in this particular region.

III. Methodology

In this section, we describe the workflow of the fault injector framework and how PCS can be used to mitigate errors selectively.

A. Fault Injector

We first need to decide upon the type of faults we will be introducing to our circuits. We adopt the same approach as QuFI, i.e., using the U rotation gate to model a single-qubit fault.

$$U(\theta, \phi) = \begin{pmatrix} \cos\frac{\theta}{2} & -\sin\frac{\theta}{2} \\ \sin\frac{\theta}{2} & e^{i\phi}\cos\frac{\theta}{2} \end{pmatrix} \tag{5}$$

Here, ϕ is the angle defined in the XY plane of the Bloch Sphere or is a rotation angle in the Z-axis. And θ is the angle defined in the plane that includes the Z-axis.

Our fault injector framework takes as input a *Quantum-Circuit* object of the Qiskit framework. For this circuit, we collect all the unique positions in the circuit where a single-qubit fault can be injected. For example, a simple circuit with one qubit and one Hadamard gate has two positions where a fault can be placed. One is before the Hadamard gate and the other is after the Hadamard gate. Once the unique positions are determined, we inject an error by adding a U gate there. We repeat this procedure for each unique fault injection site. Then we measure the outcome probability distribution from these circuits and compare the probability distribution of the faulty circuit with the ideal error-free circuit and give a vulnerability score to the place where the error was placed. The vulnerability score is determined using either Hellinger fidelity or Total Variation Distance(TVD).

Hellinger fidelity is a measure of the similarity between two probability distributions. It quantifies how close one distribution is to another by comparing their shapes and magnitudes. Specifically, Hellinger fidelity measures the square of the overlap between the square roots of the probability distributions. It is a symmetric measure that ranges from 0 to 1, where a value of 1 indicates that the distributions are identical and a value of 0 indicates that the distributions have no overlap. If P and Q are discrete distributions over the same set of outcomes X, the Hellinger fidelity is computed as:

$$H(P, Q) = \left(\sum_{x \in X} \sqrt{P(x) \cdot Q(x)} \right)^2$$

where $P(x)$ and $Q(x)$ are the probabilities assigned by distributions P and Q to outcome x, respectively.

Total Variation Distance (TVD) is a measure of the difference between two probability distributions. It quantifies how much one distribution diverges from another by calculating the total absolute difference between their probability mass functions or probability density functions. A smaller TVD

indicates that the distributions are more similar or closer to each other, while a larger TVD indicates greater dissimilarity or distance between the distributions. If P and Q are discrete distributions over the same set of outcomes X, the TVD is computed as:

$$\text{TVD}(P, Q) = \frac{1}{2} \sum_{x \in X} |P(x) - Q(x)|$$

where $P(x)$ and $Q(x)$ are the probabilities assigned by distributions P and Q to outcome x, respectively.

As an example, consider a 5 qubit GHZ circuit as shown in Figure 1a. With a single-qubit fault being modeled as the U gate with $\theta = \pi$ and $\phi = 0$, after injecting this fault at different locations in the circuit, we contain an error map for the circuit in Figure 1b. Here, each square in the grid represents the unique point in the circuit where a U gate is placed. Since there are 5 qubits in the GHZ circuit, the height of the error map is 5. The width of the error map denotes the depth of the circuit. Since the circuit consists of one Hadamard gate, four CNOT gates, and one extra slot between the last CNOT gate and the measurement register, the depth is six. The green color signifies that the Hellinger fidelity is close to 1, meaning that the region of the circuit is more robust, whereas the red region represents that the Hellinger fidelity is close to 0 and the region is vulnerable to this particular fault. By changing θ and ϕ, we can obtain a set of error-sensitivity maps, one for each (θ, ϕ) combination, as shown in Figure 1c. From the figure, we can see that (1) the same fault injected at different locations has different impacts. In particular, Figure 1b shows that the fault injected before and after the Hadamard gate has no impact on the output (as the fault is essentially a bit flip error) while the same fault injected at other locations is much more severe. (2) Different faults have different impacts. For the GHZ circuit, the output is not sensitive to certain types of faults, e.g., θ being either 0 or 2π, but is more sensitive to others, e.g., θ being close π.

B. Making use of Error-Sensitivity Information

Based on the vulnerability analysis, we propose to apply mitigation techniques selectively to protect the most vulnerable regions. One option is to use PCS for such a purpose. For PCS, the key is to find the operators C_1 and C_2. For each vulnerable region we choose to protect, there will be also an overhead of one ancilla qubit.

We demonstrate the use of PCS for the 3-qubit QAOA circuit in Figure 2. In this example, we choose to protect the second Rz gate for qubit q2. As $U = Rz$, C_1 and C_2 are controlled-Z gate as $ZRzZ = Rz$. Any error that does not satisfy this relation would be detected using PCS. For example, consider a bit flip error occurred in this region. Since the bit flip does not satisfy the commutation relation $ZXRzZ \neq Rz$, the ancilla qubit will be state 1 when the error occurs. We can post-select only the results for which the ancilla qubit is measured 0.

There are two reasons why we choose to protect the most vulnerable region rather than the entire circuit. First, finding

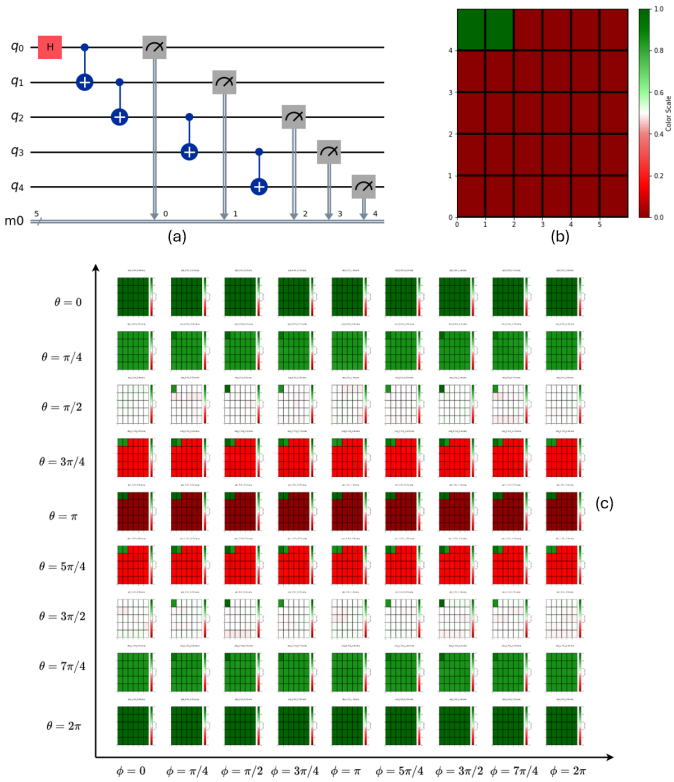

Fig. 1. Error-Sensitivity map for a 5-qubit GHZ circuit. (a) The 5-qubit GHZ circuit. (b) The error sensitivity map of an error, modeled as the U gate with $\theta = \pi$ and $\phi = 0$, injected at different depths (X-axis) and different qubits (Y-axis) in the circuit. The error impact is quantified using the Hellinger Fidelity w.r.t. to the error-free case. The fidelity value of 1 (green color) means the injected error has a negligible impact on the output state while the fidelity value of 0 (red color) means a high impact on the output state. (c) The collection of error sensitivity maps of different single-qubit faults, modeled with different combinations of θ and ϕ, injected at different sites.

C_1 and C_2 that satisfy $C_2' U C_1' = U$ would be easy when U is a small region, e.g., one or few gates. In comparison, if we use PCS to protect the entire circuit, calculating C_1 and C_2 that commute with the entire circuit is usually much more difficult and sometimes impossible. Second, the more latency between C_1 and C_2, which would be the case for protecting the entire circuit, the more likely an idling error may happen on the ancilla qubit, affecting the mitigation capability of the PCS circuit.

IV. Results

We run our fault injection and analysis framework upon the SuperMarQ benchmarking suite [11] and custom circuits. The benchmarks include GHZ, QAOA, QFT, and a Full-Adder. Our experiments are performed at the logical level (i.e., not specific to the target device) on the IBM Qiskit QASM simulator. The number of shots is set to 2048.

A. Understanding the results

As illustrated in Fig. 1, for each benchmark, we get a LxL matrix of subimages. Here, L is the number of the angles for each θ and ϕ from the range [0,2π]. On the horizontal axis,

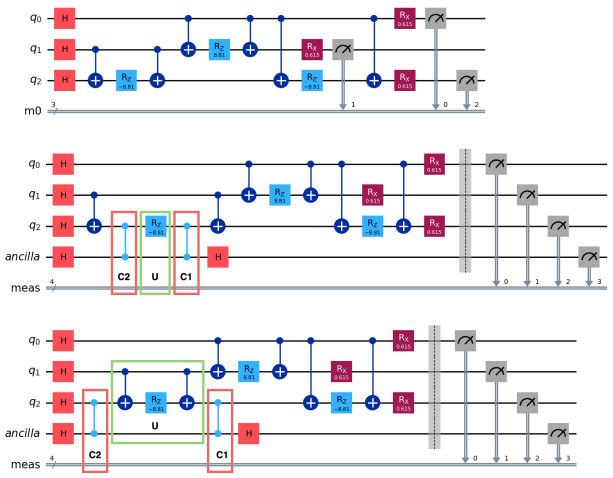

Fig. 2. An illustration of using PCS to protect a region in a circuit. The top circuit shows a 3-qubit QAOA circuit. The middle circuit shows the same circuit with gate U (an RZ gate) being protected using PCS. The gate to be protected is highlighted in the green box. The ancilla qubit is the extra qubit we will need to carry out PCS. We selected $C_2$and C_1 such that $C_2' U C_1' = U$ where $C_2$and C_1 are the controlled gate versions of C_2' and C_1'. In our case U = Rz; therefore, C_2 and C_1 will be the controlled-Z gates as shown by the box highlighted in red as $ZRzZ = Rz$. We post-select only those measurements for which the ancilla qubit measures 0. The bottom circuit shows the same circuit but in this case, we are protecting the region highlighted in green consisting of 2 CNOT gates and one RZ gate. In this case, U becomes $U = X.Rz.X$. The C_1 and C_2 are again the controlled-Z gates since the Z gate commutes with U.

angles of ϕ are increasing and θ is constant. On the vertical axis, angles of θ are increasing and ϕ is constant.

Each sub-image is a further grid of M rows and N columns. M represents the M qubits in the circuit. and each column represents the unique positions for the placement of the fault injection gate.

One observation from our experiments is that Hellinger Fidelity and TVD essentially convey similar error sensitivity although the exact values would differ. Therefore, we only report Hellinger Fidelity in this section.

*1) **GHZ**:* The error sensitivity of GHZ is shown in Figure 1c. From the results, we observe that ϕ or the rotation around the Z axis has no effect on the result. Only rotation around the X axis in the Bloch sphere causes significant errors. Additionally, we observe that the first two positions for the first qubit are robust to errors. That is because if we place an X gate in front of the Hadamard gate there is only a change in the phase, not the magnitudes. And if the gate is placed after the Hadamard gate, then there is no change to the qubit state. This is not the case for the other qubits due to the entangling CNOT gates.

*2) **Adder Circuit**:* The 3-qubit Adder circuit has its most vulnerable region when there is considerable rotation around the X-axis as we can see in Figure 3. And the most vulnerable regions are around the CNOT gates. Rotation around the Z-axis has minimal effect on the result as it only causes a change in phase and does not affect the measurement result. The errors are caused because of entanglement due to the numerous

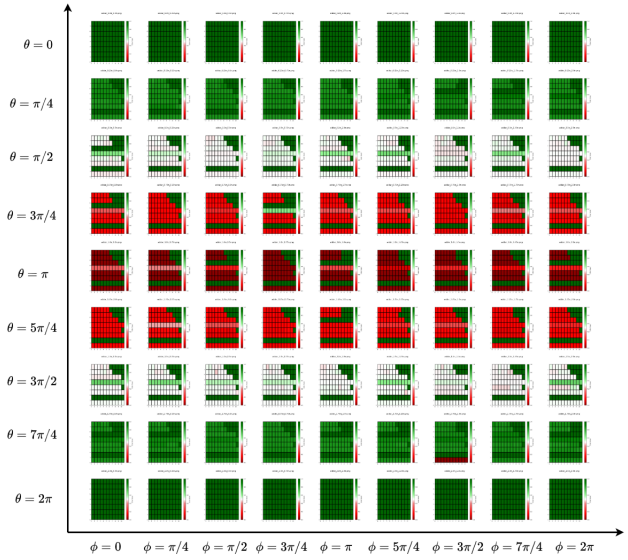

Fig. 3. Error-Sensitivity map for a 3-qubit full-adder circuit with Hellibger Fidelity as the metric. The X-axis shows the values for ϕ and the Y-axis shows the values for θ for a particular image. The green boxes imply a value close to 1 and the red boxes imply a value of 0.

CNOT gates which propagate the error to other qubits in the circuit.

*3) **QFT Circuit**:* The error sensitivity map for the 4-qubit QFT circuit is shown in Figure 4. We can see that the most vulnerable region is when ϕ = [3π/4,5π/4]. And the most vulnerable points are the Controlled Phase gates. Any rotation around the Z-axis in around them will cause erroneous results. QFT is unsurprisingly more robust to X rotation errors because there are only Hadamard gates in the circuit that are robust to X rotation errors.

*4) **QAOA**:* The error sensitivity of a 3-qubit and a 4-qubit QAOA circuit is shown in Figure 6 and Figure 5, respectively. The 3-qubit QAOA becomes vulnerable to faults where θ = [3π/4,5π/4] or ϕ = [3π/4,5π/4]. On the other hand, as the number of qubits increases to 4, the QAOA circuit becomes much more robust as can be seen in Figure 5. We further confirm this observation on a 10-qubit QAOA circuit when the fault is modeled with $\theta = \pi$ and $\phi = \pi$.

There are two reasons for this pattern. First, as the number of qubits increases the circuit depth increases and the rotation around the X-axis increases whereas the rotation around the Z-axis reduces. So any error introduced in front of these rotation gates is getting more time to be corrected and is having relatively less effect on the result as compared to a smaller circuit. Second, larger QAOA circuits have a more extensive solution space due to the additional qubits, allowing them to explore alternative solutions and potentially find more robust outcomes despite the fault.

B. Protecting QAOA using PCS

We use the 3-qubit QAOA circuit to showcase how we apply PCS to protect its most vulnerable regions. The 3-qubit QAOA

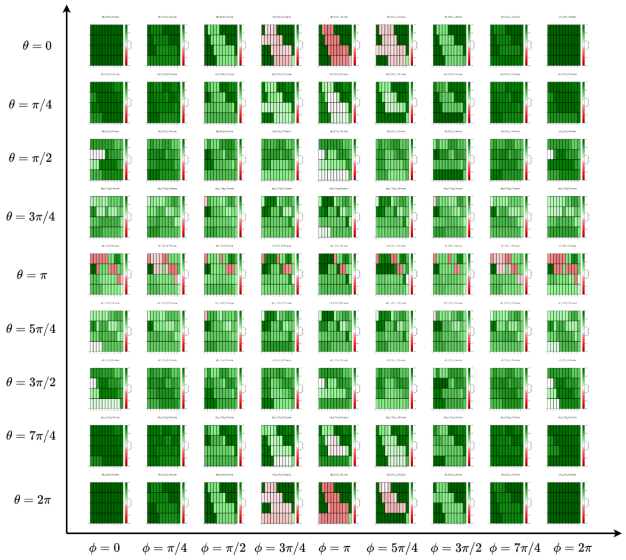

Fig. 4. Error-Sensitivity map for a 4-qubit QFT circuit with Hellibger Fidelity as the metric. The X-axis shows the values for ϕ and the Y-axis shows the values for θ for a particular image. The green boxes imply a value close to 1 and the red boxes imply a value of 0.

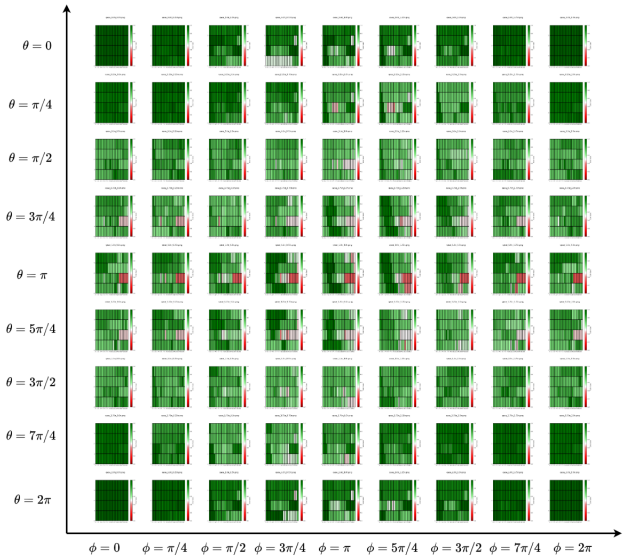

Fig. 5. Error-Sensitivity map for a 4-qubit QAOA circuit with Hellibger Fidelity as the metric. The X-axis shows the values for ϕ and the Y-axis shows the values for θ for a particular image. The green boxes imply a value close to 1 and the red boxes imply a value of 0.

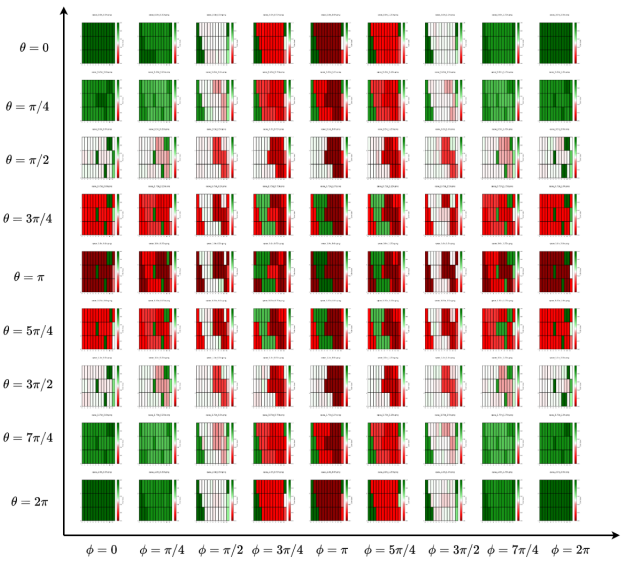

Fig. 6. Error-Sensitivity map for a 3-qubit QAOA circuit with Hellibger Fidelity as the metric. The X-axis shows the values for ϕ and the Y-axis shows the values for θ for a particular image. The green boxes imply a value close to 1 and the red boxes imply a value of 0.

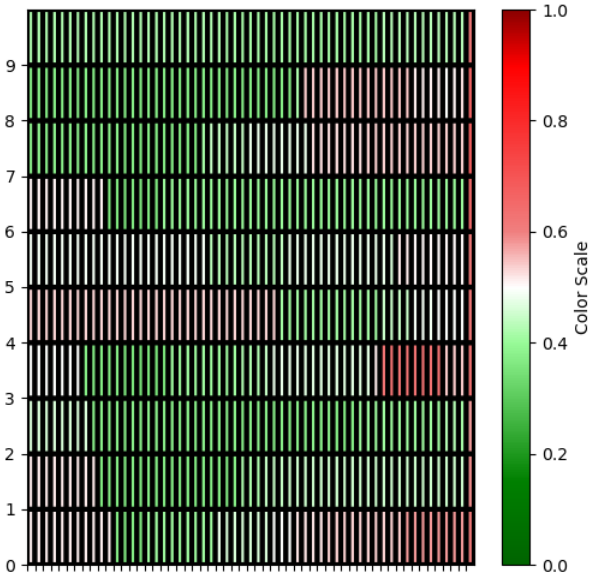

Fig. 7. Error-Sensitivity map for a 10-qubit QAOA circuit with Hellibger Fidelity as the metric. The map is generated for the case when U gate has $\theta = \pi$ and $\phi = \pi$. The green boxes imply a value close to 1 and the red boxes imply a value of 0.

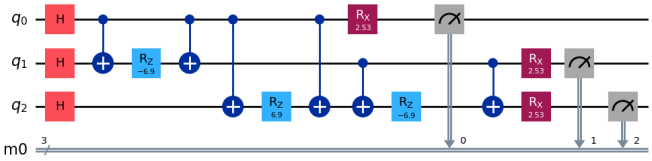

Fig. 8. 3 qubit QAOA circuit.

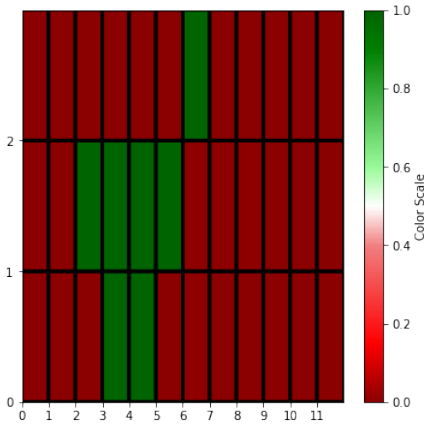

Fig. 9. Error-Sensitivity map for the initial QAOA circuit with Hellinger Fidelity as the metric. The map is generated for the case when the U gate has $\theta = \pi$ and $\phi = \pi$. The circuit in general is quite vulnerable. The cause can be pinpointed to the latter rotation gates.

circuit is shown in Figure 8.

According to our previous analysis, the circuit is most vulnerable to faults when the U gate has $\theta = \pi$ and $\phi = \pi$. Also, the most vulnerable position is the Rz and the Rx gates. The Rz gates, in the beginning, are relatively robust as the rotation errors are overshadowed by the latter rotations in the circuit. This can be observed in the error map shown in Figure 9.

Now, we use PCS to protect all the rotation gates one at a time and see their effect on the vulnerability of the circuit. For the Rz gates, C_1 and C_2 are selected to be the Controlled-Z gates. For the Rx gates, C_1 and C_2 are also the Controlled-X gates. This is because Z gate commutes with Rz gates and X gate commutes with Rx gates.

The error sensitivity map of the PCS-protected QAOA circuits is shown in Figure 10. We see that the coordinates corresponding to the first Rz gate for qubit q2 do not show considerable improvement in fidelity. However, for subsequent rotation gates, there is a strong improvement in the fidelity. The most fidelity gain can be observed for the Rx gates at the end of each qubit. This confirms that latter rotation gates are more vulnerable as any rotation error introduced around them has a lesser chance of being corrected. These gates benefit the most from the PCS protection.

V. Conclusion

In this paper, we have introduced a fault injector system that assesses the vulnerability of each region of the circuit. We

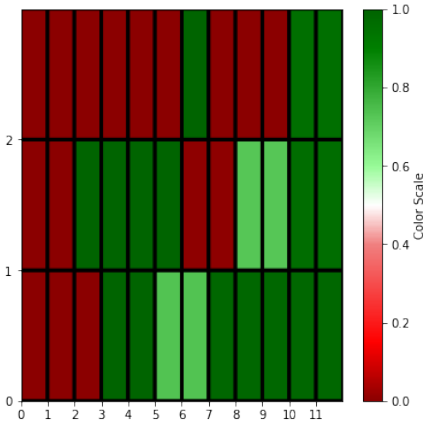

Fig. 10. Error-Sensitivity map for the PCS-protected QAOA circuit with Hellibger Fidelity as the metric. The map is generated for the case when the U gate has $\theta = \pi$ and $\phi = \pi$. After protecting the rotation gates one at a time, we see that the circuit becomes relatively more robust as indicated by the new green boxes in the error map.

proceed to identify the most vulnerable regions in the benchmarks of the SuperMarQ framework and analyze the reason for their vulnerability. The fault injector system provides a vulnerability map for each circuit to quantify which regions are more prone to errors. Such information can be used to guide the automatic insertion of error mitigation schemes like PCS to protect the most vulnerable regions in the circuit. In this paper, we mainly focus on PCS for selective error mitigation. Another possible option is to leverage circuit cutting [12] or knitting [13] technique so that the most vulnerable regions are carried out on classical computers. Such exploration is left as our future work.

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