A Near-Sensor Image Processing Accelerator for Low-end FPGA Design

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***Abstract*—This abstract proposes a lightweight near-sensor image preprocessor for video data. The hardware system design targets low-power devices with constrained power and hardware resources. Our approach is a two-stage hierarchical architecture consisting of saliency-based generators that feed a saliency filter. Preliminary results demonstrated significant energy and hardware optimization compared to previous work in this field. Specifically, the proposed architecture uses 0.24%, 0.60%, and 9% of the total processing elements used by examined related work. Similarly, the total on-chip power usage of 0.686W, which is 34.5 % and 5.3% less for the same baseline. This motivates the integration of our near-sensor logic into a system where a high-level algorithm can benefit from data filtering.**

***Index Terms*—Near-sensor processing, Image processing**
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I. Problem and Motivation

Previous research has shown the profound benefits of near-sensor processing in edge computing. Some of these advantages include real-time operations and limited security concerns. However, there is a trade-off for long battery life, especially when good quality is required [1]. As ongoing research strives to bring some level of data processing and inference closer to sensory units, there exist some wavering shortcomings like; high energy and hardware logic requirements due to complex circuit designs and algorithms [2], [3].

Our contributions include preliminary findings of power and hardware overhead optimizations brought about by reconfigurable near-sensor processing architecture. We propose a novel near-sensor processing logic with highly optimized processing element usage and power draw. In short, our contributions can be summarized as follows:

- Proposed a novel approach for light-weight near-sensor processing; Power and hardware optimizations.
- Characterized basic building circuits used in filters for saliency-based image processing.

II. Concept of Proposed Design

The flowchart in Fig 1 explains our near-sensor design concept. The first stage generates the spatial (SS) and temporal saliency (TS) flags needed for further pixel filtering in stage two. Active pixel data are selected in the second stage of the near-sensor processing. The saliency-based filter module uses the SS and TS flag values to filter out redundant pixel data in the pixel stream. An active area is only ensured when there exists both spatial and temporal saliency. Both SS and TS flags are generated by using logic circuits that compare pixel data with hardware ”change thresholds”. If the pixel data exceed the threshold, then high SS and TS values pulse out.

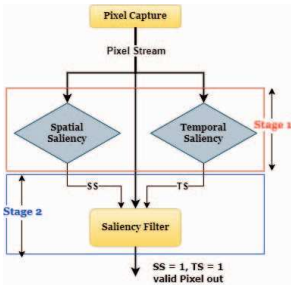

Fig. 1: Simplified flowchart of Near-sensor Processing.

III. Results

Experimental results from a low-end FPGA setup show significant optimizations which can be seen in the abstract. This results reflect considerable acceleration potentials that can benefit high-level processing for applications like object detection and gist-based recognition.

References

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