A Modulation Scheme for Differential-Mode ZVS Resonant-Switched-Capacitor Rectifier

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***Abstract*—This article proposes a predictive modulation scheme for a differential mode resonant switched capacitor rectifier (DMRSCR) to achieve high efficiency and power factor correction (PFC) for wide voltage gain. The modulation scheme ensures extensive zero-voltage switching (ZVS) turn-ON on all the switches under varying sinusoidal input voltage without requiring additional circuits or sensors. Four key control parameters, namely, phase shift ratio, duty cycle ratios, and switching frequency, are controlled for the converter to maintain ZVS turn-ON, PFC, output voltage regulation, and reduced resonant inductor current ripple. The article outlines a detailed DMRSCR model to deduce the dependency of the four control and converter design parameters on the converter operation. Based on the model, a complete converter design process is provided. A DMRSCR prototype rated at 1.1 kW was built using the underscored design methodology to validate the proposed modulation scheme, reaching a peak efficiency of 98.27%.**

***Index Terms*—Modulation, power factor correction (PFC), rectifier, resonant switched capacitor converter (RSCC), zero-voltage switching (ZVS) region.**

I. Introduction

A POWER factor correction (PFC) converter is commonly utilized for rectification in power converters, such as LED drivers and electric vehicle (EV) chargers [1]. Its primary purpose is to generate a smooth sinusoidal input current in the same shape as the input voltage that complies with established standards. PFC is essential for improving the power factor (PF), minimizing harmonics, and ensuring more efficient utilization of electrical power from the grid [2]. This helps meet regulatory requirements and enhances the overall performance of the power conversion system. [2]

The conventional PFC circuit contains a diode bridge (DB) and a dc/dc converter [1], [2], [3]. As diodes are passive components, there is limited control over the DB. In addition, the diodes incur higher losses due to forward voltage drop. To overcome this, bridgeless (BL) PFCs are introduced. BL PFC converters are widely used topologies used in rectifier converters due to better controllability and ability to achieve higher efficiency [4]. A BL boost PFC design is proposed in [5]. In this design, the switching frequency is maintained low to avoid high switching losses, allowing high efficiency. However, the size of the passive components is high due to the low switching frequency operation of the converter. In contrast, the switching frequency is relatively high in [6], resulting in reduced size of the passive components. Nevertheless, the efficiency of the converter is affected by high switching losses incurred due to hard-switching and core losses. The converter proposed in paper [7] achieves ZVS turn-ON on the switches, resulting in reduced switching loss and better efficiency. The control system in this approach requires an additional control parameter, which necessitates more tuning, and the topology requires three magnetic cores.

As discussed earlier, high switching frequency operation of a converter can give a design with small-size components with minimal losses if the ZVS turn-ON is ensured. The approaches proposed in papers [8], [9], and [10] can operate at a relatively high switching frequency with high efficiency. In these approaches, the switching frequency varies in a wide range, from several kHz to several MHz, to achieve ZVS turn-ON for a wide instantaneous input voltage variation. The ZVS realization for the wide switching range necessitates a high-speed digital controller to control the operation. In addition, this converter solution also needs a zero-crossing detection circuit and a high-speed current sensor to detect the input current for the ZVS realization.

Other contenders of high-density BL PFCs are switched capacitor converters (SCCs), flying capacitors, and resonant switched capacitor converters (RSCCs) [11], [12], [13]. Typically, SCCs contain switches and capacitors without magnetics, allowing high-density design [14], [15]. However, they are suitable for low-power applications as the switches undergo hard-switching, resulting in significant losses because of current spikes on switches during the switching. To mitigate the switching losses and allow high-power application, a partial-charge-capacitor [16] or peak-current-control [17] technique is generally used to reduce losses; however, these techniques result in lower power density. To mitigate current spikes during the switching and reduce the switching losses and electromagnetic interference [18], an inductor can be connected to the input of the converter [19]. However, a large size inductor is required due to dc bias input current. Alternatively, the inductor can be in series connection with the flying capacitor, allowing the converter to operate as a resonant converter [20], [21], known as the RSCC.

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Depending on the location of the input voltage source, the RSCC can operate as a step-up or step-down converter. It can be used in different applications due to its notable attributes of high voltage ratio, lightweight, high efficiency, and scalability [22], [23].

Soft switching techniques are utilized in RSCC to increase its efficiency. They are generally employed to mitigate switching losses and increase efficiency in power converters [24]. Zero current switching [25] and ZVS [26] are the techniques that are usually utilized to achieve soft switching for all the switches in RSCC using a specific modulation and strategy. Therefore, the RSCC can operate in high switching frequencies to reduce the component size which soft switching is used to increase efficiency. However, it is essential to note that high efficiency is confined to a narrow range of input or output voltage variations as reported in previous works [27], [28].

The RSCC can be controlled with four different control parameters, namely, dead-time [29], phase shift [28], switching frequency [30], and duty cycle [31]. These control parameters are used to modulate and control the RSCC to regulate the output voltage and achieve soft switching. These parameters must be varied as per the load, input voltage, and/or output voltage [32].

Optimizing the RSCC performance involves pinpointing the ideal region for the mentioned control parameters. This region is crucial for achieving ZVS turn-ON and is dependent on the input voltage, the output voltage, the load conditions, and the *LC* resonance link. Careful analysis of dependency based on the specifications of the converter help to identify the optimal operational zone [33], [34]. Therefore, depending on the variations of each input voltage, output voltage, or load, the ZVS region changes [31], [27]. Hence, careful modulation of the control parameter is required based on the varying instantaneous input voltage for the PFC operation. Numerous studies have provided a dc/dc RSCC model within a narrow input voltage or load range. However, there is a lack of a full-model which successfully accounts for the dependency on the mentioned control parameters.

As mentioned above, the RSCC offers two main advantages: high efficiency due to soft switching on all the switches [27] and increased power density by operating the converter at high switching frequencies [23]. Therefore, RSCC can be used in some applications that require high power density and higher efficiency, such as PFC rectifiers in EVs.

This article proposes a new resonant switched capacitor rectifier consisting of two RSCCs that are connected differentially [35], [36], as shown in Fig. 1. This structure is referred to as DMRSCR. To achieve high-efficiency PFC operation, and output voltage regulation (VR), the RSCC is operated with four control parameters: phase shift ratio, duty cycle ratios, and switching frequency. A closed-form model of the RSCC is developed to account for the dependency on these control parameters and the resonant circuit. Hence, the model can be used to facilitate an optimal converter design. The proposed model is able to accurately predict the converter's behavior and allows formulation of modulation scheme which allows ZVS turn-ON on all the switches. Therefore, it does not need any additional sensors or circuit to detect the converter's behavior in each switching period to achieve soft switching. Using this model, the DMRSCR can operate for a wide voltage gain while

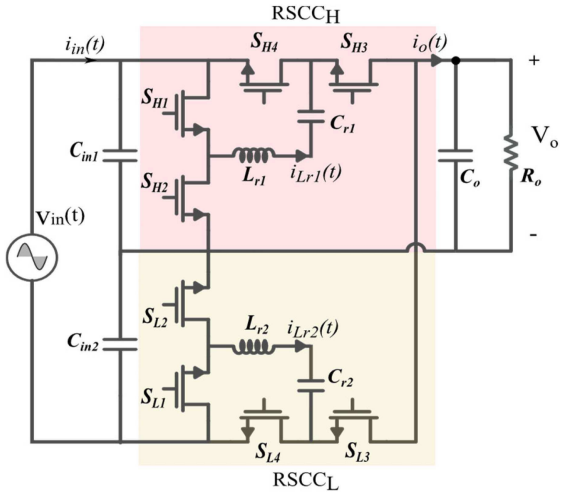


Fig. 1. Proposed DMRSCR topology.

maintaining ZVS for all the switches. It is shown that the ZVS region is primarily dependent on the duty cycle and is not impacted by the switching frequency. Therefore, the switching frequency does not need to be wary in a wide range. It must only vary in range to keep the VR and reduce the resonant inductor current ripple. Therefore, a low-speed digital controller is needed to operate in this switching frequency range. A control structure is proposed for DMRSCR to have the mentioned goals simultaneously. This control structure is simple and mainly based on converter modulation.

The main contributions of this study are summarized as follows.

1) In the proposed DMRSCR, a comprehensive model has been introduced. This model takes into account the dependency of four control parameters: phase shift ratio, two duty cycle ratios, and switching frequency. It requires more degrees of freedom to achieve PFC, ZVS turn-ON for all switches, voltage regulation, and reduced resonant inductor current ripple across a wide load range.
2) A modulation scheme is presented to allow high-efficiency operation in DMRSCR. The modulation scheme is derived based on the proposed model, which ensures ZVS turn-ON for all active converter switches while performing PFC rectification over a wide load range. As a result, ensuring ZVS is model-based and does not require additional circuitry to detect the converter's behavior regarding ZVS, and thus, the converter can operate with a simple control system.

The rest of this article focuses on analyzing and operating the dc/dc RSCC and DMRSCR in Section II. Section III delves into the ZVS region, power transfer, VR, and PFC in DMRSCR. The converter's design considerations are detailed in Section IV, followed by hardware results based on the designed parameters in Section V. Finally, Section VI concludes this article.

II. Operation and Analysis of a DMRSCR Module

A. Operation of DMRSCR

As illustrated in Fig. 1, the DMRSCR comprises two step-up dc/dc RSCC modules, namely RSCC$_H$ and RSCC$_L$. These

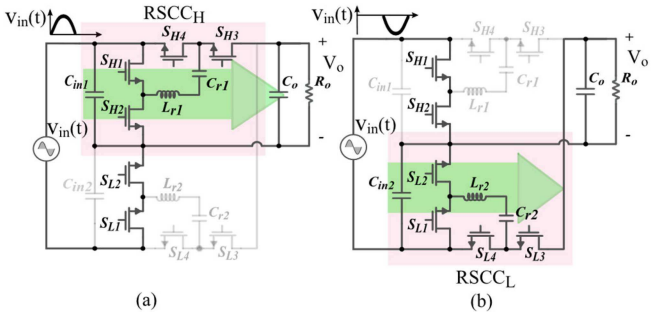


Fig. 2. Operation mode of the DMRSCR. (a) Positive half cycle. (b) Negative half cycle of the input voltage.

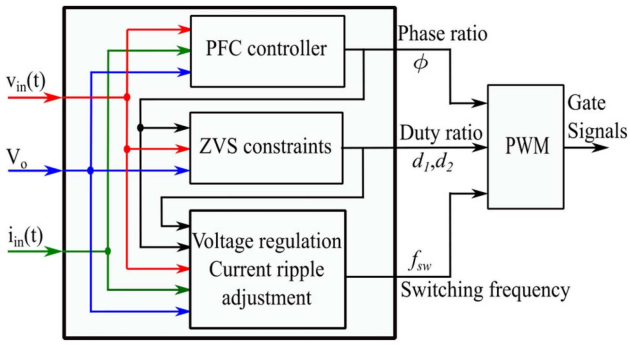


Fig. 3. Modulation scheme for the DMRSCR.

modules are connected in series at the input and parallel at the output. As shown in Fig. 2, the DMRSCR operates using a discontinuous modulation scheme [36], which yields the operation of RSCC_H and RSCC_L, respectively, during the positive and negative half cycles of the input voltage. That is, during the positive (negative) line cycle, switches. $S_{H1} - S_{H4}$ ($S_{L1} - S_{L4}$) of RSCC_H (RSCC_L) operate at high switching frequency while ensuring complementarity and switches S_{L1} and S_{L2} (S_{H1} and S_{H2}) are turned ON during the entire period. The operating modes are detailed in Section II-B.

As depicted in Fig. 2(a), during the positive half cycle of the input voltage, the RSCC_H operates. Functioning as a dc/dc RSCC with a variable input voltage in which the input voltage changes from zero to its peak positive value. Simultaneously, the RSCC_L needs to complete the route of current for the RSCC_H, as illustrated in Fig. 2(a), switches S_{L1} and S_{L2} need to be conducted to complete the current route. In the case of MOSFET switches, the body diodes automatically conduct, eliminating the necessity to turn on the low-side switches. However, with gallium nitride (GaN) switches, it is necessary to turn the switches on to prevent reverse conduction losses in GaN switches. This operational pattern is mirrored for the RSCC_L when the input voltage is in its negative half cycle. As portrayed in Fig. 2(b), when the low-side module is operating, the switches S_{H1}, S_{H2} need to conduct to complete the current route. The RSCC_L also operates as a dc/dc RSCC when the input voltage changes from zero to its negative peak value. Consequently, each RSCC operates as a dc/dc converter with a variable input voltage from zero to a peak value. Moreover, in the PFC rectifiers, the power transfer to the output is variable with twice the input voltage frequency. This implies that the load is also variable in each RSCC. Hence, each RSCC in the DMRSCR operates with variable input voltage and variable load.

PFC, efficiency, and VR are necessary for paying attention to each PFC rectifier. Fig. 3 shows the modulation scheme for the DMRSCR. Notably, the phase shift serves the purpose of PFC because its variations are aligned with the input voltage changes. Moreover, using a simple linear controller ensures that selecting the phase shift to track sinusoidal variations maintains linearity in the controller's operation. By varying the phase shift under PFC requirements, the duty cycle is determined to achieve ZVS across the entire or wide range of the input voltage because the value of the resonant inductor current is

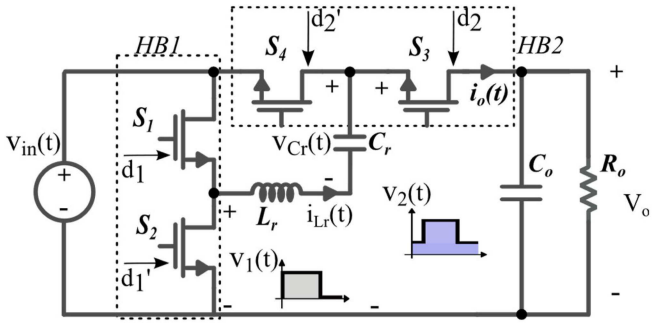


Fig. 4. Schematic of a DMRSCR module (i.e., a dc/dc RSCC).

the key to attaining ZVS in both RSCC and DMRSCR in each switching period and the duty cycle is the remaining parameter that can specify the proper value of the resonant inductor current in each switching period. The switching frequency is computed by the specified phase shift and duty cycle to attain VR and adjust the resonant inductor current ripple (Δi_{Lr}) based on the input-voltage variation and power transfer to mitigate conduction losses around the zero crossing (ZC). The switching frequency inversely affects the power transfer, allowing for the regulation of output voltage by controlling the transferred power to the load. Therefore, by controlling the switching frequency, the minimum power can be transferred near the ZC, which will need a lower inductor current ripple, and the maximum value will be at the peak of the input voltage.

B. DMRSCR Module (dc/dc RSCC) Modes of Operation

The operation of the DMRSCR is based on the operations of two dc/dc RSCCs. Consequently, the model for the DMRSCR is attainable through the modeling of a single dc/dc RSCC with variable input voltage. Therefore, Fig. 1 can be summarized as Fig. 4. The RSCC consists of two half bridges (HB), which are HB1 and HB2, as delineated in Fig. 4. Switches S_1 and S_2 belong to the HB1, which are input-side switches and S_3 and S_4 belong to the HB2, which is connected between the input and the output. Two distinct duty ratios, namely d_1 and d_2 are specified for each HB, showcasing their differentiation throughout the converter operation to achieve ZVS across a wide input voltage range.

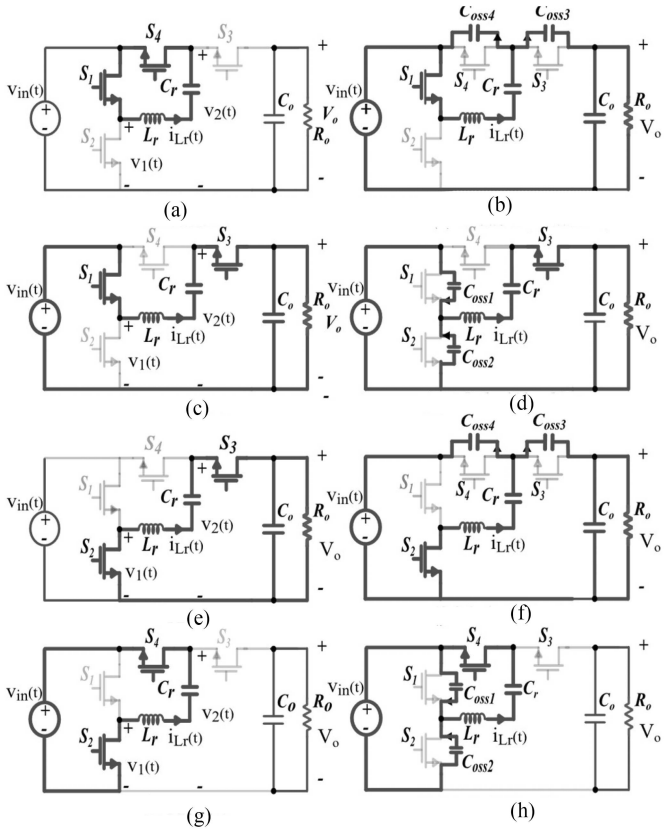


Fig. 5. Modes of operation for a DMRSCR module (i.e., a dc/dc RSCC). (a) Mode 1. (b) Mode 2 (deadtime). (c) Mode 3. (d) Mode 4 (deadtime). (e) Mode 5. (f) Mode 6 (deadtime). (g) Mode 7. (h) Mode 8 (deadtime).

Therefore, the DMRSCR operates properly when ϕ, duty ratio, and f_{sw} are varying based on the input voltage variations.

Additionally, there is an *LC* resonant tank containing a resonant inductor (L_r) primarily employed to mitigate current spikes in the switches and a resonant capacitor (C_r) which is the capacitor for the switched capacitor converter. The adjustment of this *LC* resonant tank is pivotal in achieving soft switching within the converter. Specifying a proper value for L_r is essential as it aids in achieving soft switching by discharging the output capacitor (C_{oss}) of the switches during deadtime modes. This RSCC operates as a step-up converter.

This converter contains four switches, and they can operate in two main modes when there is no phase shift and $d_1 = d_2$ and the switching frequency is close to the resonance frequency (f_r) [25], [37]. Additionally, they can operate in four main modes when the phase shift is introduced, and duty cycle ratios d_1 and d_2 are variable or constant. This study underscores the indispensability of phase shift for input current feedback control due to attaining PFC in DMRSCR. Moreover, the resonant inductor current must be linear during the main modes. Therefore, the *LC* resonance period between the resonant inductor and capacitor should be much larger than each main switching mode to ensure that the resonant inductor current is linear. Therefore, the switching frequency is deliberately set far from the resonance frequency. The operational modes of the dc/dc RSCC are elucidated in Fig. 5. These modes depend on considerations

TABLE I
SEQUENCE OF SWITCHES IN MAIN AND DEADTIME MODES

	S_1	S_2	S_3	S_4	C_{oss1}	C_{oss2}	C_{oss3}	C_{oss4}
Mode1 (main)	1	0	0	1	0	0	0	0
Mode 2	1	0	0	0	0	0	1	1
Mode 3 (main)	1	0	1	0	0	0	0	0
Mode 4	0	0	1	0	1	1	0	0
Mode 5 (main)	0	1	1	0	0	0	0	0
Mode 6	0	1	0	0	0	0	1	1
Mode 7 (main)	0	1	0	1	0	0	0	0
Mode 8	0	0	0	1	1	1	0	0

TABLE II
PARAMETRIC SIMPLIFIED VOLTAGE SOURCES VALUES

	Time duration	$v_1(t)$	$v_2(t)$	$v_2(t) - v_1(t)$
Mode 1	ϕT_{sw}	$v_{in}(t)$	$v_{in}(t)$	0
Mode 3	$(d_1 - \phi)T_{sw}$	$v_{in}(t)$	V_o	$V_o - v_{in}(t)$
Mode 5	$(d_2 + \phi - d_1)T_{sw}$	0	V_o	V_o
Mode 7	$(d_2' - \phi)T_{sw}$	0	$v_{in}(t)$	$v_{in}(t)$

such as deadtime and C_{oss}. This converter exhibits a total of eight distinct modes of operation. As can be seen, the RSCC operation contains four main modes (modes 1, 3, 5, and 7) and four deadtime modes (modes 2, 4, 6, and 8). The sequence of modes and corresponding switches is delineated in Table I. During the main modes, two switches are involved, whereas in the deadtime modes, a single switch with a couple of C_{OSS} capacitors conduct.

C. Modeling of a DMRSCR Module (dc/dc RSCC)

The negligible deadtimes between complementary gate pulses, especially when compared to the main modes' durations, permit their omission from consideration. By disregarding these deadtimes, the operational focus is streamlined to four main modes, which are modes 1, 3, 5, and 7, as shown in Fig. 5. Considering these four main modes, the converter must operate as a step-up converter in a positive phase shift. Simplification of the converter can be realized by representing it as two voltage sources. $v_1(t)$, $v_2(t)$, and one *LC* tank. The value of these voltages in each main mode in Fig. 5(a), (c), (e), and (g) are as Table II. In this table, T_{sw} is the switching period.

The voltage sources $v_1(t)$ and $v_2(t)$ encompass ac and dc components. The simplified waveforms illustrating the four main modes in the dc/dc RSCC are depicted in Fig. 6. the shape of the $i_{Lr}(t)$ undergoes variations contingent upon the relationships among the input voltage, output voltage, and resonant capacitor voltage ($v_{Cr}(t)$). Notably, the slope of $i_{Lr}(t)$ in each mode is influenced by the specific values of these three voltages. The waveforms for $i_{Lr}(t)$ and $i_o(t)$ in Fig. 6 exemplify one of the potential conditions among $v_{\text{in}}(t)$, V_o and $v_{Cr}(t)$ as a representative waveform.

In this article, the value of the C_r is assigned a large enough value, resulting in a minimal resonant capacitor voltage ripple (ΔV_{Cr}) compared to V_{Cr} within one switching cycle ($\Delta V_{Cr} \ll V_{Cr}$).

By distracting the dc value and using the gyrator theory [38], Fig. 7 shows the ac equivalent circuit of main modes in the Fig. 5.

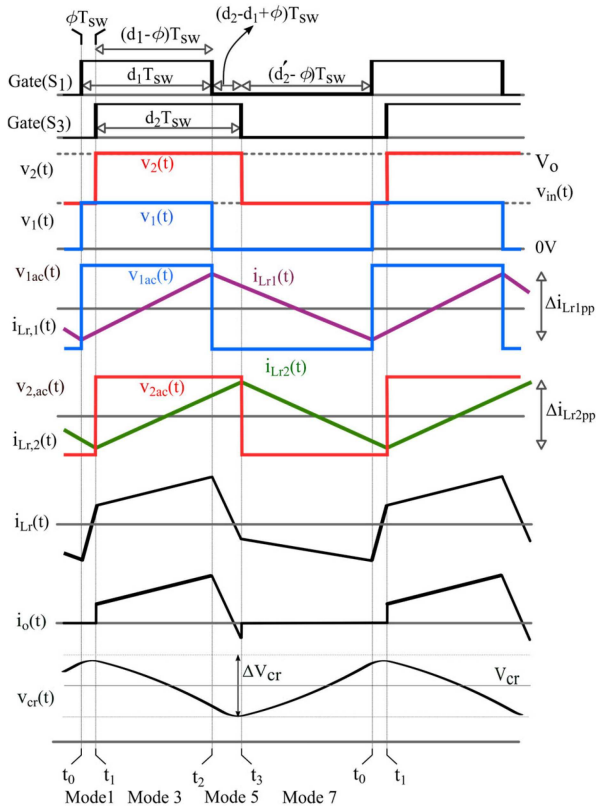


Fig. 6. Waveforms of the simplified DC/DC RSCC.

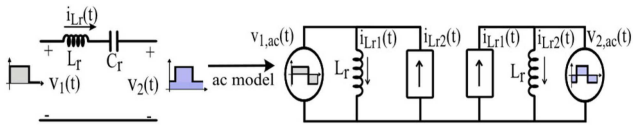


Fig. 7. AC equivalent simplified circuit of the DC/DC RSCC.

The average value of $\langle v_2(t) - v_1(t)\rangle_{T_{sw}}$ in each switching cycle denotes the average resonant capacitor voltage (V_{cr}) and each of $\langle v_2(t)\rangle_{T_{sw}}$ and $\langle v_1(t)\rangle_{T_{sw}}$ can be expressed as (1)–(3)

$$\langle v_2(t) - v_1(t)\rangle_{T_{sw}} = V_{cr} = d_2 V_o + v_{in}(t)(1 - d_2 - d_1) \tag{1}$$

$$\langle v_1(t)\rangle_{T_{sw}} = d_1 v_{in}(t) \tag{2}$$

$$\langle v_2(t)\rangle_{T_{sw}} = d_2 V_o + v_{in}(t) d_2' \tag{3}$$

$$d_2' = 1 - d_2. \tag{4}$$

The ac components for $v_1(t)$ and $v_2(t)$ are determined by subtracting their average values. Using (2), (3), and Table II, these values are expressed in Table III.

In the above equations, the expression for d_1' is as (5) and $t_4 = t_0 + T_{sw}$

$$d_1' = 1 - d_1. \tag{5}$$

TABLE III
AC COMPONENTS OF THE SIMPLIFIED VOLTAGE SOURCES

	$v_{1ac}(t)$	$v_{2ac}(t)$
$t_0 < t < t_1$	$d_1' v_{in}(t)$	$-d_2(V_o - v_{in}(t))$
$t_1 < t < t_2$	$d_1' v_{in}(t)$	$d_2'(V_o - v_{in}(t))$
$t_2 < t < t_3$	$-d_1 v_{in}(t)$	$d_2'(V_o - v_{in}(t))$
$t_3 < t < t_0$	$-d_1 v_{in}(t)$	$-d_2(V_o - v_{in}(t))$

Based on Fig. 7 and the values in Table III, the peak-to-peak value of each inductor will be as (6) and (7)

$$\Delta i_{Lr1_{pp}} = \frac{d_1' d_1 v_{in}(t) T_{sw}}{L_r} \tag{6}$$

$$\Delta i_{Lr2_{pp}} = \frac{d_2' d_2 (V_o - v_{in}(t)) T_{sw}}{L_r}. \tag{7}$$

As depicted in Fig. 6, the output current flows when the switch S_3 is conducting, characterizing modes 2 and 3 as the output current. The average value of the output current for each dc/dc RSCC module at one switching period T_{sw} is expressed as follows:

$$i_o(t) = -\frac{v_{in}(t)\left(\phi^2 + d_1 d_2'(d_1 - 2\phi - d_2)\right)}{2 f_{sw} L_r}. \tag{8}$$

III. AC/DC MODULATION OF DMRSCR

A. ZVS Constraints for a DMRSCR Module

Considering a constant value for the C_{oss} in this article, the initial values of the $i_{Lr}(t)$ in each main mode should surpass the needed amount of current for discharging and charging the C_{oss} capacitors in each complementary switch.

As evident in Fig. 4, achieving ZVS for S_1 requires the resonant inductor current to be negative and for S_2, it should be positive. Also, the current should be positive for S_3 and negative for S_4. Accordingly, the ZVS conditions based on the waveforms in Figs. 6 and 4 can be expressed as follows:

$$\begin{cases} i_{Lr}(t_0) < -\dfrac{2C_{oss} v_{in}(t)}{t_{db}}, \ [\text{ZVS for } S_1] \\ i_{Lr}(t_1) > \dfrac{2C_{oss}(V_o - v_{in}(t))}{t_{db}}, \ [\text{ZVS for } S_3] \\ i_{Lr}(t_2) > \dfrac{2C_{oss} v_{in}(t)}{t_{db}}, \ [\text{ZVS for } S_2] \\ i_{Lr}(t_3) < -\dfrac{2C_{oss}(V_o - v_{in}(t))}{t_{db}}, \ [\text{ZVS for } S_4]. \end{cases} \tag{9}$$

In accordance with Fig. 7, the value of the $i_{Lr}(t)$ is the difference between two separated primary and secondary inductor currents, and it would be as follows:

$$i_{Lr}(t) = i_{Lr1}(t) - i_{L2}(t). \tag{10}$$

In reference to Fig. 7 and waveforms $i_{Lr1}(t), i_{Lr2}(t)$ in Fig. 6, the slope of each inductor, which is the voltage across each inductor in each mode, could be found from Table III for each current. Furthermore, using values in Table III, (6), (7) and (10),

the initial values in each main mode for $i_{Lr}(t)$ are as (11)–(14) which are dependent on the three control parameters of phase shift, duty cycles, and the switching frequency. Precise determination of these initial conditions is crucial for the proper operation of the converter

$$i_{Lr}\ (t_0) = \left(d_2\left(1-m\left(t\right)\right)\left(2\phi - d_2^{'}\right) - d_1 d_1^{'}\right)\ \frac{v_{\text{in}}\left(t\right)T_{\text{sw}}}{2L_r} \tag{11}$$

$$i_{Lr}\ (t_1) = \left(d_1^{'}\left(2\phi - d_1\right) + d_2 d_2^{'}\left(m\left(t\right)-1\right)\right)\ \frac{v_{\text{in}}\left(t\right)T_{\text{sw}}}{2L_r} \tag{12}$$

$$i_{Lr}\ (t_2) = \left(\begin{array}{c}\left(m\left(t\right)-1\right)d_2^{'}\left(d_2+2\phi-2d_1\right)\\ +d_1 d_1^{'}\end{array}\right)\ \frac{v_{\text{in}}\left(t\right)T_{\text{sw}}}{2L_r} \tag{13}$$

$$i_{Lr}\ (t_3) = -\left(\begin{array}{c}d_2 d_2^{'}\left(m\left(t\right)-1\right) - d_1 d_1^{'}\\ +2d_1\left(\phi - d_1 + d_2\right)\end{array}\right)\ \frac{v_{\text{in}}\left(t\right)T_{\text{sw}}}{2L_r} \tag{14}$$

where $m(t)$ is the voltage gain, and it is defined as follows:

$$m\left(t\right) = V_o\ /v_{\text{in}}\left(t\right). \tag{15}$$

With the initial conditions specified in (9) and initial values in (11)–(14), the ZVS conditions could be achieved based on the input voltage variations. By substituting (11)–(14) in (9) inequalities and solve those inequalities for d_1 and d_2, eight constraints arise for each d_1 and d_2. These constraints have some overlaps, and they can condensed into two common constraints for d_1 as expressed in (16), and two common constraints defined in (17) for d_2. These constraints ensure that the ZVS conditions remain unaffected by the switching frequency, disregarding the influence of the C_{oss} capacitor

$$\begin{cases} i)\ d_1 < \frac{1}{2} - \left(m\left(t\right)-1\right)d_2^{'} + \sqrt{\begin{array}{l}\frac{1}{4}\left(1-2\left(m\left(t\right)-1\right)d_2^{'}\right)^2\\ +\left(m\left(t\right)-1\right)d_2^{'}\left(d_2+2\phi\right)\\ -\frac{4L_rC_{oss}}{T_{\text{sw}}t_{db}}\end{array}} \\ ii)\ d_1 < -\frac{1}{2} + \phi + d_2 + \sqrt{\begin{array}{l}\frac{1}{4}\left(2\phi-1+2d_2\right)^2\\ +d_2\left(m\left(t\right)-1\right)d_2^{'}\\ -\frac{4L_rC_{oss}\left(m\left(t\right)-1\right)}{T_{\text{sw}}t_{db}}\end{array}} \end{cases} \tag{16}$$

$$\begin{cases} i)\ d_2 > \frac{1}{2} - \phi + d_1 - \sqrt{\begin{array}{l}\frac{1}{4}\left(2\phi-2d_1-1\right)^2 + 2\left(\phi-d_1\right)\\ +\frac{d_1 d_1^{'}}{m\left(t\right)-1} - \frac{4L_rC_{oss}}{T_{\text{sw}}t_{db}\left(m\left(t\right)-1\right)}\end{array}} \\ ii)\ d_2 < \frac{1}{2} - \dfrac{d_1 - \sqrt{\begin{array}{l}\frac{1}{4}\left(m\left(t\right)-1\right)^2 + 2\phi d_1\left(m\left(t\right)-1\right)\\ +\left(2-m\left(t\right)\right)d_1^2 - \frac{4L_rC_{oss}\left(m\left(t\right)-1\right)}{T_{\text{sw}}t_{db}}\end{array}}}{m\left(t\right)-1}. \end{cases} \tag{17}$$

TABLE IV
DMRSCR PARAMETERS VALUES

Parameter	Value
V_{in}(rms)	120 – 300 V_{rms}
f_{in}	60 Hz
V_o	450 V
Output power (P_o)	1.1 kW
$L_{r1} = L_{r2}$	30 μH
$C_{r1} = C_{r2}$	9.6 μF
C_{out}	1 mF
f_r	9.68 kHz
Duty ratio (d_1)	0.4-0.45
Duty ratio (d_2)	0.4 – 0.75
Phase shift ratio (ϕ)	0 – 0.2
Deadband (t_{db})	100 ns

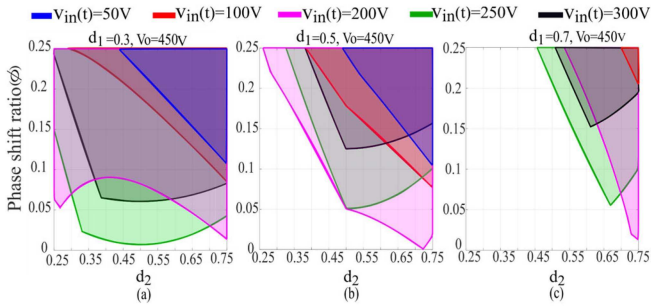


Fig. 8. ZVS region by in different values of the input voltage. Phase shift versus d_2 in three values of d_1. (a) $d_1 = 0.3$. (b) $d_1 = 0.5$. (c) $d_1 = 0.7$.

B. ZVS Region Analysis

In Table IV, the designed parameters for the converter in a 1.1 kW prototype with 450 V_{dc} the output voltage is outlined. With these parameters, the ZVS region can be specified. In this part, the ZVS region is defined when the root mean square (RMS) of the input voltage is $V_{\text{in}} = 230\ V_{\text{rms}}$ as an example. The region can be similarly determined for other input voltage levels.

As depicted in Table IV, the input voltage exhibits variations ranging from zero to a peak value of 325 V for $V_{\text{in}} = 230\ V_{\text{rms}}$. Consequently, the phase shift, duty cycle, and switching frequency need to change or be precisely determined to have PFC, ZVS, VR, and Δi_{Lr} adjustment, respectively. Utilizing the information provided in Table IV, (9), (16), and (17) the ZVS region under different input voltage values is depicted in Fig. 8. In this figure, the ZVS region is limited by four lines obtained using (11)–(14). The common area from those lines represents the ZVS region.

As evident in Fig. 8, the ZVS region changes with variations in the input voltage, and the ZVS region becomes broader when $d_1 < 0.5$, indicating that operating with $d_1 < 0.5$ is more favorable in this converter. Fig. 8 also highlights that the most extensive ZVS region occurs when the input voltage is approximately half the output voltage. In some areas around zero crossing and the peak value of the input voltage, the ZVS region is narrower. Consequently, achieving ZVS in DMRSCR becomes more straightforward when the input voltage is close to half of the output voltage, with a wide range of duty cycles and phase shift. Achieving ZVS is sensitive when the input

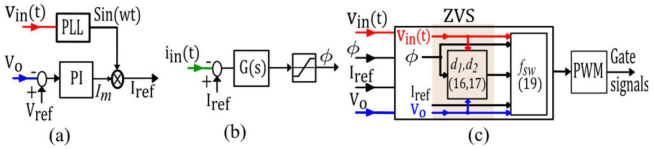


Fig. 9. Overall control diagram with (a) VR, (b) PFC, and (c) ZVS constraints and f_{sw} calculations in detail.

voltage is around ZC or the peak value of the input voltage. Therefore, careful consideration of ZVS in these areas is crucial. In DMRSCR, the power transfer around the ZC is minimal, and the losses around this area can be negligible. However, the maximum transferring power occurs when the input voltage is close to the peak value, emphasizing the importance of ensuring ZVS in these areas. Therefore, to achieve ZVS in different values of the input voltage, d_1 and d_2 must adapt to variations in the input voltage. The PFC is achieved based on the phase shift variations. Thus, after specifying the phase shift, the duty cycles will subsequently adjust based on ZVS conditions related to the input voltage and the constraints in (16) and (17). Fig. 9(c) shows the duty cycle calculation in the control diagram.

C. Voltage Regulation

The power transferred to the output is determined by multiplying the output voltage by the output current. Equation (8) provides the expression for the output current. In the ideal case of the DMRSCR, the input power is equal to the output power asfollows:

$$V_m I_m \sin^2(\omega t) = V_o\, i_o(t) \tag{18}$$

where V_m and I_m are the peak values of the input voltage and the input current, respectively. Thus, the switching frequency can be derived from (8) and (18) as shown in the following:

$$f_{\text{sw}} = \frac{1}{T_{\text{sw}}} = -\frac{V_m R_o}{4 V_o L_r \sin(\omega t)}\left[\phi^2 + d_1 d_2^{'}(d_1 - 2\phi - d_2)\right] \tag{19}$$

where R_o is the load resistance. As evident, the switching frequency becomes a function of the input voltage and is subject to change in response to variations in the input voltage.

Due to the linear operation in the converter and the $i_{L_r}(t)$ waveform in Fig. 6, the maximum value of the resonant inductor current represents one of the initial values and the initial values in (11)–(14) change based on the input voltage variations. Therefore, the maximum value of $i_{L_r}(t)$ also varies. When the input voltage approaches the ZC, the voltage gain increases, and the initial conditions in (11)–(14) can be summarized as (20)–(23) in DMRSCR

$$i_{L_r}(t_0)\;|_{v_{\text{in}}(t)\to 0} = -d_2 V_o (2\phi + d_2 - 1)\left(\frac{1}{2L_r f_{\text{sw}}}\right) \tag{20}$$

$$i_{L_r}(t_1)\;|_{v_{\text{in}}(t)\to 0} = -d_2 V_o (d_2 - 1)\left(\frac{1}{2L_r f_{\text{sw}}}\right) \tag{21}$$

$$i_{L_r}(t_2)\;|_{v_{\text{in}}(t)\to 0} = -V_o (d_2 - 1)\left(\frac{2\phi + d_2 - 2d_1}{2L_r f_{\text{sw}}}\right) \tag{22}$$

$$i_{L_r}(t_3)\;|_{v_{\text{in}}(t)\to 0} = d_2 V_o (d_2 - 1)\left(\frac{1}{2L_r f_{\text{sw}}}\right). \tag{23}$$

The initial resonant inductor currents near ZC from (20)–(23) are predominantly influenced by the switching frequency, phase shift, and duty cycles. Given the minimal power transfer near ZC, it is necessary to maintain a small resonant inductor current ripple to minimize conduction losses. Therefore, increasing the switching frequency around the ZC reduces the resonant inductor ripple in that area.

The output voltage can be found from (19) and it will be as (24). As can be seen, the output voltage is a function of the switching frequency and the load. Therefore, the switching frequency needs to vary to regulate the output voltage. Consequently, the switching frequency variation has two benefits of VR and adjustment of the Δi_{Lr} particularly around ZC

$$V_o = -\frac{V_m R_o}{4 f_{\text{sw}} L_r \sin(\omega t)}\left[\phi^2 + d_1 d_2^{'}(d_1 - 2\phi - d_2)\right]. \tag{24}$$

Fig. 9(a) illustrates the VR control diagram. In this figure, the output voltage is compared with the reference voltage, and the created error is compensated by a proportional-integral (PI) block. Multiplying the PI output by the phase-locked loop generates the reference current (I_{ref}) and this current is utilized to calculate the f_{sw} and the current control loop in the PFC part.

D. PFC Control Method

The DMRSCR operates as a rectifier, functioning with an ac input voltage that necessitates the implementation of PFC. The control diagram for the PFC is structured as a closed-loop system, where feedback from the input current is utilized to regulate the PF. The control diagram for the PFC is a simple diagram illustrated in Fig. 9(b).

In Fig. 9, after defining I_{ref} from the VR section in Fig. 9(a), it is compared with the actual input current as the PFC section in Fig. 9(b). The resulting error is then compensated in a PI compensator, $G(s)$. Subsequently, the desired phase shift is established. Duty cycles ratios (d_1, d_2) and the switching frequency (f_{sw}) are defined based on (16), (17), and (19) as depicted in Fig. 9(c).

Once the closed-loop controller determines the phase shift, the values of the duty cycle ratios (d_1, d_2) and the switching frequency can be calculated, and the pulsewidth modulation (PWM) signal is generated accordingly depending on the input voltage value in the positive or negative half cycle. In DMRSCR, the phase shift is constrained to a range of $0 < \phi < 0.2$. In the subsequent section, the maximum value of d_2 is determined to be 0.75. It is crucial to maintain the maximum value of the phase shift below 0.25 to ensure the correct switching sequence as per Table I and avoiding any unwanted mode. Also, higher phase shift values can lead to increased conduction losses due to circulating current. Because in higher phase shift operation, the converter will remain longer in mode 1 as shown in Fig. 5(a) and this mode makes more circulating current.

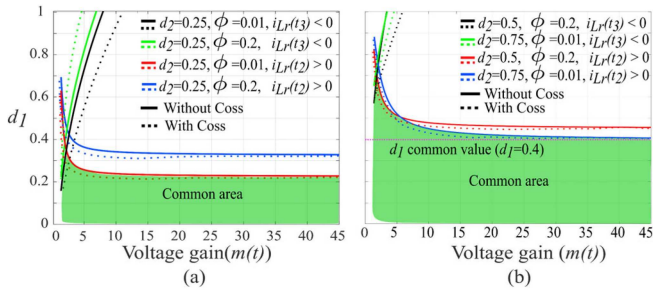


Fig. 10. Common area for specifying d_1 for ZVS area. (a) $0.25 < d_2 < 0.75$. (b) $0.5 < d_2 < 0.75$.

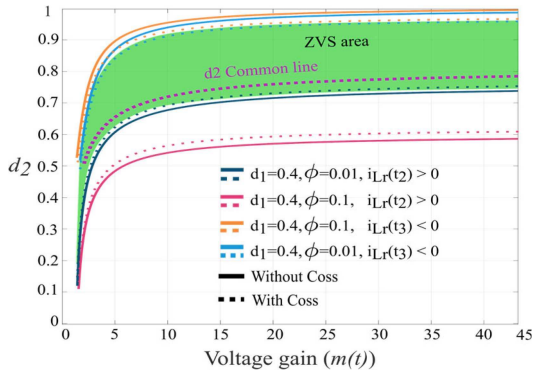


Fig. 11. Common area for d_2 based on the critical value of $d_1 = 0.4$.

IV. Hardware Design of DMRSCR

A. Resonant Inductor and Capacitor Design

The minimum resonant inductor current for charging and discharging the C_{oss} capacitors is given by the following:

$$i_{\text{minZVS}} = 2C_{oss}V_{DS}/t_{db}. \tag{25}$$

In (25), V_{DS} is the drain-to-source voltage of the switch, which is turning OFF and t_{db} is the dead band, which should be sufficiently long to discharge C_{oss}.

By assuming a 1 kW output power and $V_{\text{in}} = 230\ V_{\text{rms}}$ as a sample design, the minimum switching frequency is considered 70 kHz for transferring the instantaneous peak power of 2 kW and therefore, using (19), the resonant inductor value is calculated as $L_r = 30\ \mu$H.

The resonant capacitor's value should be sufficiently large to ensure that the f_r is far from the minimum switching frequency ($f_{\text{sw\_min}}$) allowing the converter to operate in a linear mode. Because of that, the value of the resonant capacitor is considered as $C_r = 9.6\ \mu$F. Therefore, the value of f_r is as follows:

$$f_r = \frac{1}{2\pi\sqrt{L_rC_r}} = 9.68\ \text{kHz}. \tag{26}$$

As indicated in (26), the f_r is far from the minimum switching frequency ($f_{\text{sw\_min}} \gg f_r$) even for other lower values of the $f_{\text{sw\_min}}$.

B. Duty-Cycle Constraints

As evident from (16), d_1 is a function of d_2, $m(t)$ and ϕ. By considering the extreme values for d_2 and ϕ, the constraints for d_1 can be determined. These constraints for d_1 are depicted in Fig. 10. In this figure, there are two types of lines. The dotted lines are the effect of C_{oss} capacitor and the full lines are without the impact of the C_{oss} capacitor in (16). The effect of the C_{oss} capacitor in d_1 variation is insignificant, and the dotted lines follow the full lines in Fig. 10. Therefore, the influence of the switching frequency on d_1 variation is negligible.

As depicted in Fig. 10, when considering extreme constraints for ϕ and d_2 between $0.25 < d_2 < 0.75$, the common area for d_1 is less than 0.24 in Fig. 10(a) which is not desirable due to increased current stress on switches. In Fig. 10(b), depicting the common area for d_1 when $0.5 < d_2 < 0.75$, the common area for d_1 is less than 0.5. Hence, selecting a fixed value within this common area is more appropriate for d_1. Considering the impact of C_{oss} on the ZVS operating region and the stress on switches for small values of d_1, the value of d_1 is chosen as $d_1 = 0.4$.

From (17), the constraints for d_2 can be derived, considering $d_1 = 0.4$. The suitable operating region for d_2 to achieve ZVS is depicted as Fig. 11. This figure illustrates that the value of d_2 needs to change to ensure ZVS across different input voltage values. Opting for a single fixed value for d_2 cannot ensure ZVS across all areas. In this figure, the dotted line, referred to as the "common line," has been designated for d_2 to change based on the input voltage. It is positioned near the lower limit of the ZVS area, considering the higher stress on the switches near the upper limit. Moreover, accounting for the effect of C_{oss}, the common line should be higher than the lower limit in the equations. Notably, the proper value for d_2 is $d_2 \geq 0.5$. In this figure, the ZVS area is concentrated when the phase shift is minimal. Thus, by assuming zero phase shift and considering $d_1 = 0.4$ the simplified equation derived from (17) is expressed as follows:

$$d_2 = \frac{3}{4} - \frac{0.45}{2m\,(t) - 1}. \tag{27}$$

Therefore, in this article, the value of d_1 can be fixed, and the value of d_2 changes based on the input voltage variations. These constraints are specified when $V_{\text{in}} = 230\ V_{\text{rms}}$. The constraints for the other input voltage values may change.

The same approach for d_1, there are two types of lines in Fig. 11 for the variations of d_2. The dotted lines are by considering the effect of the C_{oss} capacitor in (17) and the full lines are without considering the effect of the C_{oss} capacitor. As seen in this figure, the dotted lines are close to the full lines and follow the same route as the full lines. Therefore, the influence of the C_{oss} capacitor on d_2 variation is not significant, and the effect of the switching frequency on d_2 is negligible as well.

C. Switching Frequency

The situations around the ZC are important to determine the maximum switching frequency and Δi_{Lr} is the critical parameter in that area. Therefore, the maximum switching frequency can be specified by considering a limitation for the resonant inductor current around the ZC. Reducing the load alters the

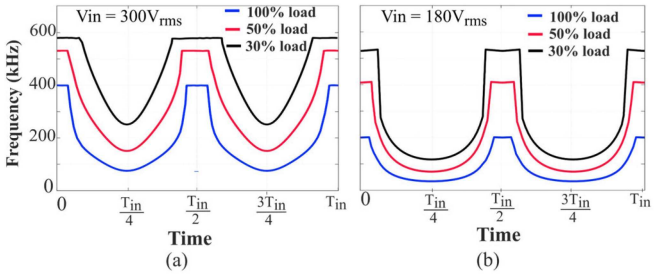


Fig. 12. Switching frequency variations based on the passing time in 100%, 50%, and 30% of the load in (a) $V_{\text{in}} = 300\ \text{V}_{\text{rms}}$ and (b) $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$.

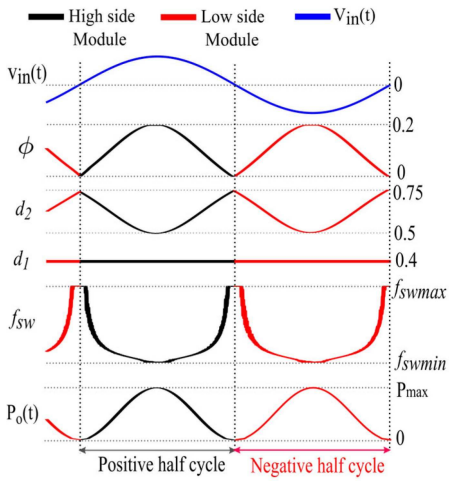


Fig. 13. Phase shift (ϕ), duty cycle ratios (d_1, d_2), switching frequency (f_{sw}) variations based on the input voltage changes.

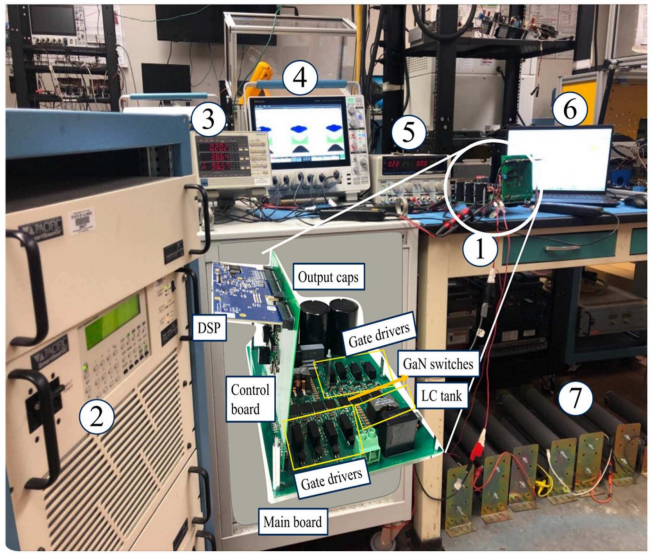
switching frequency range due to the dependency of switching frequency on load. Therefore, using (19) and Table IV, the switching frequency curves in different loads and two sample input voltages are depicted in Fig. 12 when $V_{\text{in}} = 300\ \text{V}_{\text{rms}}$ in Fig. 12(a) and $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$ in Fig. 12(b). In this figure, T_{in} is the input voltage period. As seen in this figure, the switching frequency is limited around the ZC because it goes to infinity based on (19) and it is not desired in the hardware design.

With the designed values for the phase shift, duty cycles, and switching frequency, the variations of these three parameters based on the input voltage changes are illustrated in Fig. 13. In this figure, the black traces depict the high-side module operation when the input voltage is in positive half cycle. The traces in red represent the low-side module operation when the input voltage is in its negative half cycle. The phase shift ratio is aligned with the input voltage and power transfer, and it needs to be maximum in the peak of the input voltage to transfer the maximum power to the output.

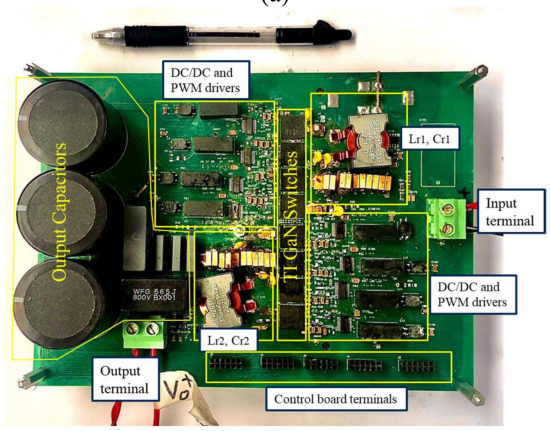
V. Hardware Results

A. Hardware Setup and the Waveforms

A 1.1 kW hardware prototype has been developed based on the specifications provided in Table IV with a hardware setup



(a)



(b)

Fig. 14. Hardware setup of the prototype. (a) 1: DMRSCR prototype with main, control, and DSP boards. 2: AC power supply. 3: power analyzer. 4: Oscilloscope. 5: Auxiliary dc power supply. 6: PC programming. 7: Resistive load. (b) Power board view.

TABLE V
TI Switch Main Specifications

TI Switch part number	LMG3422R050RQZT
$R_{DS}(on)$	50 mΩ
I_{DS_rms}	32 A
V_{DS}	600 V
C_{oss} (Average)	145 pF

shown in Fig. 14. Fig. 14(a) shows the overall view of the hardware setup with measurement devices, the power supplies, and the load. Fig. 14(b) shows a view of the power board. The switches utilized in this prototype are from Texas Instrument (TI) and are identified by the part number LMG3422R050RQZT. Critical specifications for this switch can be found in Table V. With its integrated gate driver, this switch is accompanied by additional components on the board, serving purposes such as digital isolation, switch power supply, PWM signal adjustment and slew rate control. The switches also incorporate protection

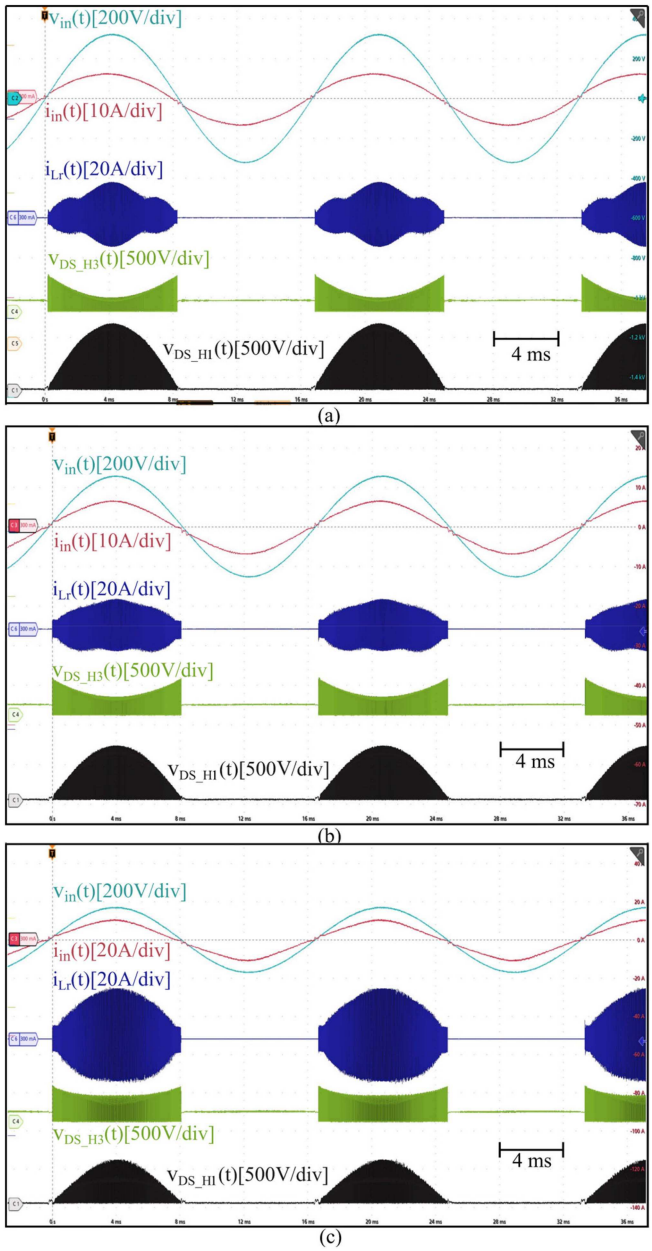


Fig. 15. Experimental results for the DMRSCR. (a) $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$. (b) $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$. (c) $V_{\text{in}} = 120\ \text{V}_{\text{rms}}$. Blue: input voltage. Red: Input current. Navy blue: High-side resonant inductor current $i_{Lr1}(t)$. Black: Drain–source voltage S_{H1} ($V_{DS_{H1}}$). Blue: Drain–source voltage S_{H3} ($V_{DS_{H3}}$).

features, including overcurrent and overtemperature safeguards and a fault signal for enhanced switch operation monitoring. The PWM signals are generated using the TMS320F28379D microcontroller from TI.

Fig. 15 shows the hardware results related to the prototype in 1 kW output power in three input voltages $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$ and $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$ and 800 W in $V_{\text{in}} = 120\ \text{V}_{\text{rms}}$. In this figure, the results for the resonant inductor current and switch waveforms are for the RSCC_{H} components. The RSCC_{L} operates the same as well. The high-side resonant inductor conducts only in the positive half cycle. Because of that, $i_{\text{Lr1}}(\text{t})$ has value only in the positive half cycle of the input voltage. The magnitude of

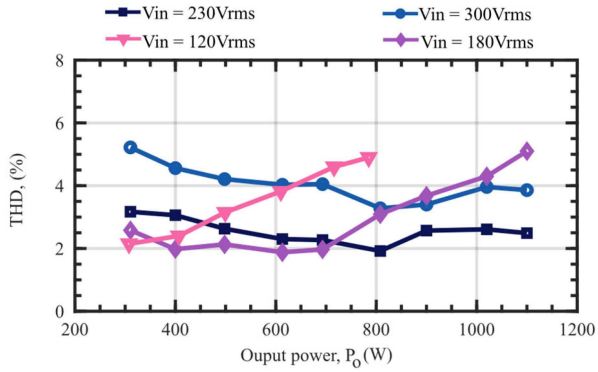


Fig. 16. Measured THD curves at different power levels for the DMRSCR. Green: $V_{\text{in}} = 300\ \text{V}_{\text{rms}}$. Black: $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$. Purple: $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$. Pink: $V_{\text{in}} = 120\ \text{V}_{\text{rms}}$.

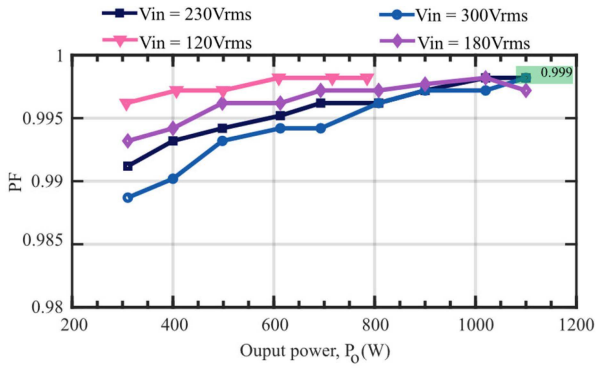


Fig. 17. Measured power factor curves in different powers and input voltage. Navy blue: $V_{\text{in}} = 300\ \text{V}_{\text{rms}}$. Black: $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$. Purple: $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$. Pink: $V_{\text{in}} = 120\ \text{V}_{\text{rms}}$.

the drain to source voltage for the input switches (IS), which are S_{H1}, S_{H2}, S_{L1}, S_{L2} equals the input voltage based on Fig. 1 and therefore, varying the input voltage causes changes in $V_{\text{DS}_{\text{H1}}}$. The difference between the input and the output voltages is on the output switches (OS), which are S_{H3}, S_{H4}, S_{L3}, S_{L4}, and the maximum $V_{\text{DS}_{H3}}$ occurs around the ZC. Total harmonic distortion (THD) in different power levels is depicted in Fig. 16. In this figure, the THD is mostly lower than 5% in different input voltages. The power factor curve in various power levels is depicted in Fig. 17.

In Fig. 15(a), there is a minimal distortion around ZC in the input current waveform. The reason for this distortion is the limitation of switching frequency. As can be seen in (19), theoretically, the switching frequency tends to reach infinitive around ZC, which is not desired and must be limited in that area. Because of that limitation, minimal distortion happens.

Fig. 17 shows the measured PF curve in different powers and rms values of the input voltages. This figure shows that the DMRSCR has a high PF in various powers and input voltages.

B. Dynamic Response

Figs. 18 and 19 show the DMRSCR dynamic response to the load and input voltage changes. Fig. 18(a) shows the dynamic

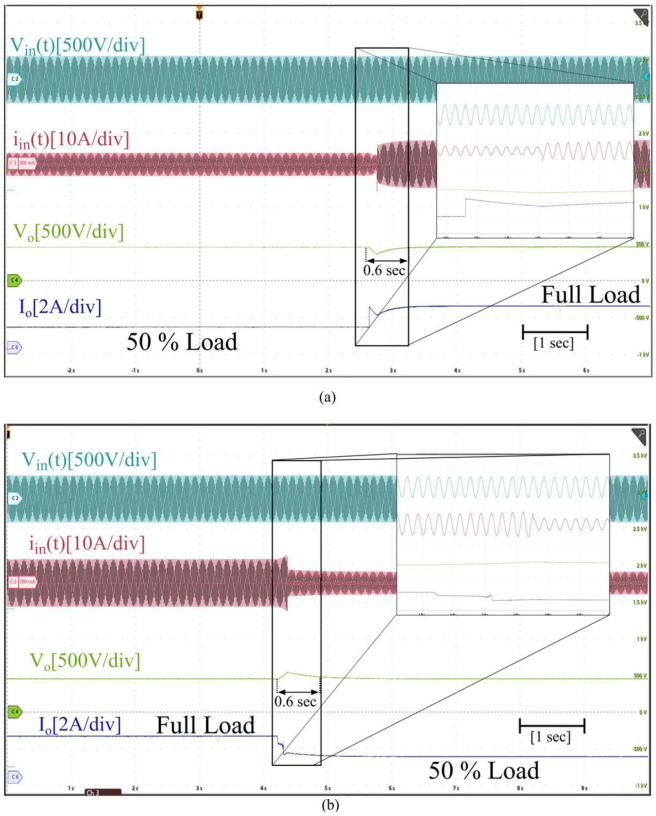


Fig. 18. DMRSCR dynamic response in changing the load with a constant input current magnitude. Blue: input voltage. Red: input current. Green: output voltage. Navy blue: output current. $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$, $\text{V}_{\text{o}} = 450$ V. (a) Changing the load from 500 W to 1 kW. (b) Changing the load from 1 kW to 500 W.

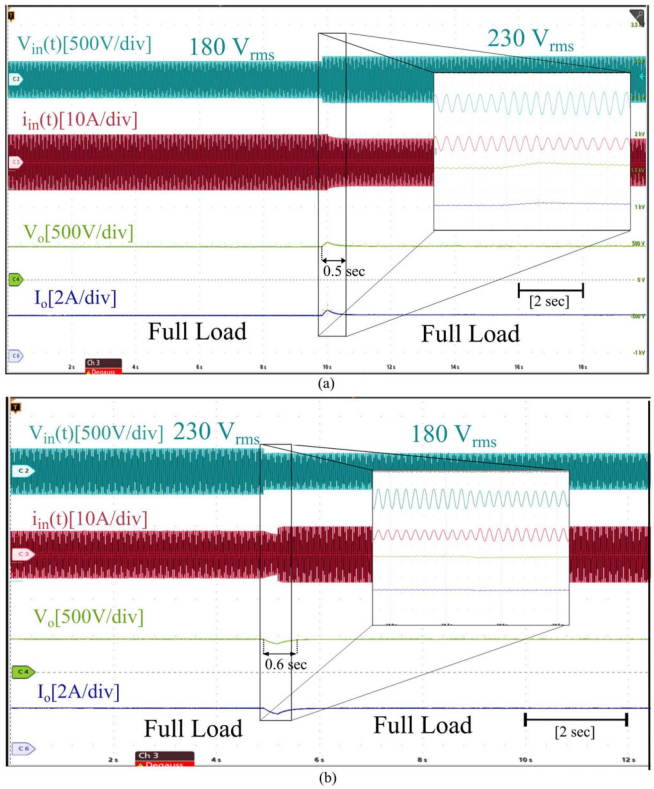


Fig. 19. DMRSCR dynamic response in changing the input voltage magnitude in a constant load. Load: 1 kW, $V_{\text{o}} = 450$ V. (a) Changing the input voltage from $V_{\text{in}} = 180\ V_{\text{rms}}$ to $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$. (b) Changing the input voltage from $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$ to $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$.

response in a sudden change in the load from 50% to the full load in a constant input voltage magnitude. This figure shows that the output voltage is regulated after 0.6 s. The opposite operation is happening in Fig. 18(b). In this figure, the load has changed from the full load to 50% load. Because of the reduction in load, there is an overshoot on the output voltage, and after 0.6 s, the output voltage returns to the original value. This overshoot is about 20% of the output voltage, which increases the output voltage to 540 V, and this value is lower than the switches voltage stress mentioned in Table V. Also, the PFC has happened, and the input current keeps sinusoidal before and after the change in both cases at Fig. 18. In Fig. 19(a) the load is constant at 1 kW, and there is a sudden change in the input voltage from $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$ to $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$. This figure shows an overshoot in the output voltage; after 0.5 s, the output voltage is regulated. This overshoot is about 15% and increases the output voltage to 518 V, which is lower than the switches voltage stress mentioned in Table V. The opposite operation has happened in Fig. 19(b) and the input voltage changes suddenly from $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$ to $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$. The output voltage has an undershoot at that time and is regulated after 0.6 s. The input current is sinusoidal, and the PFC is maintained before and after the change in both cases at Fig. 19.

TABLE VI
VOLTAGE STRESS ON SWITCHES IN DMRSCR

	IS $(S_{H1}, S_{H2}, S_{L1}, S_{L2})$	OS $(S_{H3}, S_{H4}, S_{L3}, S_{L4})$
Voltage stress (V)	V_m	$V_o - V_{in}(t)$ (V_o close to ZC)

C. Voltage and Current Stress on Switches

Based on the operating modes in Figs. 2 and 5, the voltage stress on the switches is of two different types. For the IS, only the maximum value of the input voltage is on the switches. For the OS, the difference between the input and the out voltages is on the switches. Therefore, the maximum voltage stress on the OS will be around the ZC, where the input voltage is zero, and only the output voltage is on the OS terminals. The voltage stress on switches is as Table VI.

The current stress on the switches is equal to the peak resonant inductor current. As can be seen from the modes of operation in Fig. 5, the $i_{Lr}(t)$ passes through two switches in each main mode. Therefore, the peak value of the $i_{Lr}(t)$ is the current stress for the switches. As mentioned in Section II-B, the $i_{Lr}(t)$ is linear. Therefore, the maximum value of $i_{Lr}(t)$ can be specified based on the initial values of $i_{Lr}(t)$ in each mode. The initial

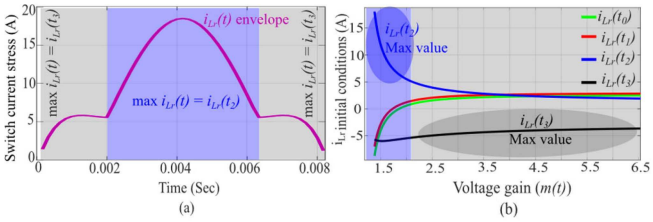


Fig. 20. Current stress on switches based on the resonant inductor current envelope in DMRSCR in full load power at 230 V_{rms} of the input voltage. (a) Maximum $i_{Lr}(t)$ envelope with the specified maximum initial conditions. (b) $i_{Lr}(t)$ initial values variations based on the voltage gain varying.

TABLE VII
CURRENT STRESS ON SWITCHES IN DIFFERENT INPUT VOLTAGES AT FULL LOAD

Switches current stress on full load				
$V_{in}(V_{rms})$	120	180	230	300
Current stress on switches	$i_{Lr}(t_3)$	$i_{Lr}(t_2)$	$i_{Lr}(t_2)$	$i_{Lr}(t_0)$

values in each mode are as (11)–(14). These initial values vary based on the input voltage and other control parameters. Thus, one of the initial values is maximum in each switching period, depending on the input voltage value. Thus, the maximum value of the resonant inductor current in each switching cycle can be obtained from (11) to (14), and it is as Fig. 20 in full load power at 230 V_{rms} of the input voltage.

In Fig. 20(a) the $i_{Lr}(t)$ envelope equals the switches' current stress in half the input voltage period. This envelope can be detected from the resonant inductor current waveform in Fig. 15(a). As depicted in Fig. 20(a), the $i_{Lr}(t)$ has two regions, considering the symmetricity of the inductor current. These regions are created based on the initial values of the $i_{Lr}(t)$, which vary based on the input voltage variations, and it shows in Fig. 20(b). In this figure, $i_{Lr}(t_2)$ is the maximum value compared to the other initial values in low values of the voltage gain (in the maximum values of the input voltage gain) and $i_{Lr}(t_3)$ has the maximum value in high values of the voltage gain (the input voltage goes to zero). Therefore, the current stress on switches is the maximum value of the resonant inductor current envelope, and it is equal to the value of $i_{Lr}(t_2)$ when $V_{in} = 230\ V_{rms}$.

Table VII shows the switches' current stress on the other RMS values of the input voltages. In this table, the current stress on the switches in DMRSCR is related to the maximum initial values of the resonant inductor current when the DMRSCR transfers the maximum power in the peak of the input voltage. It is different in each RMS input voltage.

D. ZVS Realization and the Efficiency Plots

As mentioned, the ZVS region varies with changes in the input voltage. Because of that, the ZVS operation needs to be shown in different values of the input voltage. Since the switches are equipped with integrated gate drivers, precise access to gate-to-source voltage is unavailable. Consequently, ZVS operation is illustrated based on the drain-to-source voltage and the resonant inductor current. The ZVS situations for each switch have been outlined in (9), and the status of the drain to source voltages and the resonant inductor current is illustrated in Fig. 6. Using (25) and the values from Tables IV and V, the minimum value of the $i_{Lr}(t)$ to achieve ZVS can be determined. Depending on the input voltage variations, $i_{Lr}(t)$ is 1.3 A for the OS near ZC, and it is lower at peak input voltage. The current is 0.9 A for the IS around the peak value of the input voltage, and it is lower around the ZC for the IS.

The ZVS waveforms are illustrated in Fig. 21 for a 1 kW test at $V_{in} = 230\ V_{rms}$. These results are in different values of the input voltage for the $RSCC_H$. The results mirror those of the $RSCC_L$. Notably, to achieve ZVS in the switches, the resonant inductor current must surpass the minimum values. As the input voltage increases, the required current for IS rises and decreases for the OS. In Fig. 21(a)–(d) in which the results are around the ZC to half of the output voltage, the magnitude of $i_{Lr}(t)$ is maximum for the OS, which is necessary to attain ZVS. It is lower for the IS desired to achieve ZVS for the IS. The situations are inverse for the input and OS when the input voltage is around its peak value, as shown in Fig. 21(e)–(g). Therefore, the ZVS happens for all the switches from Fig. 21(a) to (g) in a wide range of the input voltage.

Fig. 22 illustrates efficiency curves across various power levels for four RMS input voltage values, all with an output voltage of 450 V_{dc}. Lower input voltages correspond to decreased efficiency due to increased resonant inductor current magnitudes, leading to heightened conduction losses. Notably, at $V_{in} = 120\ V_{rms}$, the resonant inductor current magnitude exceeds the switches' maximum current capability, limiting the efficiency curve to below 800 W. Notably, lower efficiency is observed at lower power levels due to the converter operating at higher switching frequencies, resulting in increased turn-OFF losses. Additionally, losses become more significant compared to the transferred power at lower power levels. The maximum efficiency achieved in 1.1 kW was 98.27%. By increasing the power level, the conduction losses increase and affect efficiency.

E. Losses Analysis, Thermal Results and Comparison

Fig. 23 shows the thermal image views from the converter operation in three different situations in a 1.1 kW load when the converter operates at an input voltage of 230 V_{rms} [see Fig. 23(a)] and 180 V_{rms} [see Fig. 23(b)]. Also, another thermal image in 800 W when the converter operates in 120 V_{rms} as the input voltage [see Fig. 23(c)]. The board temperature rises when the RMS input voltage is lower at the same power level due to an increase in input current and switch current. This leads to higher conduction losses on switches, resulting in increased temperature on the board. Additionally, the red color in the images is mainly around the switches, demonstrating the impact of the switches' conduction losses on the overall losses in the converter.

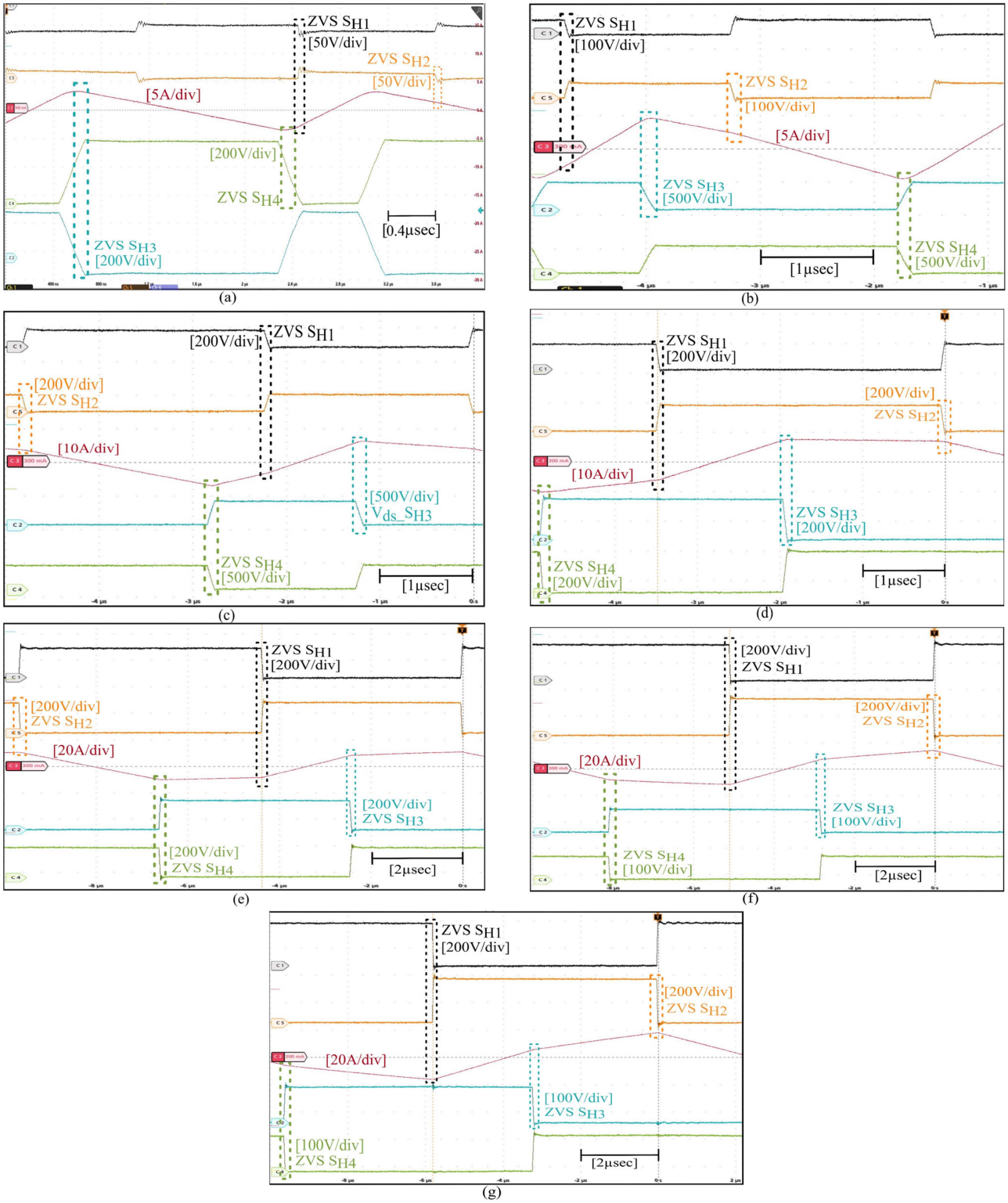


Fig. 21. Drain-to-source voltage V_{ds} in high-side module switch waveforms with high-side resonant inductor current $i_{Lr1}(t)$ in $V_{\text{in}} = 230$ V_{rms}, P_o =1 kW, and $V_o = 450$ V. In all pictures, black: $V_{ds_{SH1}}$, orange: $V_{ds_{SH2}}$, red: $i_{Lr1}(t)$, green: $V_{ds_{SH4}}$, blue: $V_{ds_{SH3}}$. (a) $V_{\text{in}}(t) = 10\ V$, $f_{\text{sw}} = 400$ kHz (b) $V_{\text{in}}(t) = 42\ V$, $f_{\text{sw}} = 370$ kHz, (c) $V_{\text{in}}(t) = 100\ V$, $f_{\text{sw}} = 178$ kHz, (d) $V_{\text{in}}(t) = 160\ V$, $f_{\text{sw}} = 125$ kHz, (e) $V_{in}(t) = 220\ V$, $f_{\text{sw}} = 100$ kHz, (f) $V_{\text{in}}(t) = 280\ V$, $f_{\text{sw}} = 83.6$ kHz , and (g) $V_{\text{in}}(t) = 320\ V$, f_{sw}=74.2 kHz.

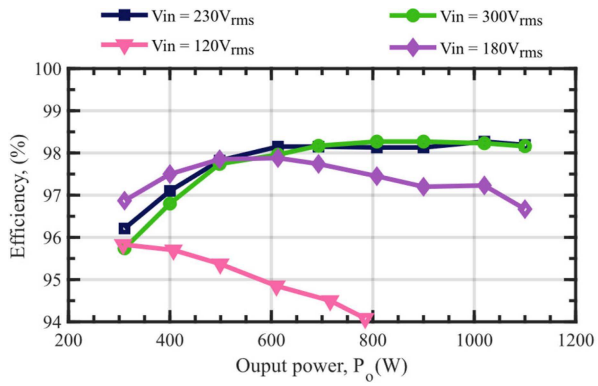


Fig. 22. Efficiency vs power for the DMRSCR experimental results in four different input voltages. Red: $V_{\text{in}} = 300\ \text{V}_{\text{rms}}$, Black: $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$, Orange: $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$, Green: $V_{\text{in}} = 120\ \text{V}_{\text{rms}}$. With $V_{\text{o}} = 450\ \text{V}_{\text{dc}}$.

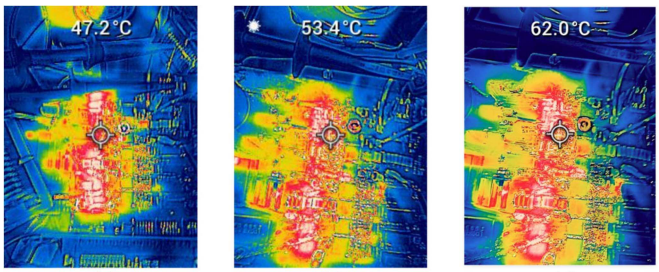


Fig. 23. Thermal image from the hardware operation in different situations. (a) $V_{\text{in}} = 230\ \text{V}_{\text{rms}}$, $P_o = 1.1$ kW. (b) $V_{\text{in}} = 180\ \text{V}_{\text{rms}}$, $P_o = 1.1$ kW. (c) $V_{\text{in}} = 120\ \text{V}_{\text{rms}}$, $P_{\text{o}} = 800$ W.

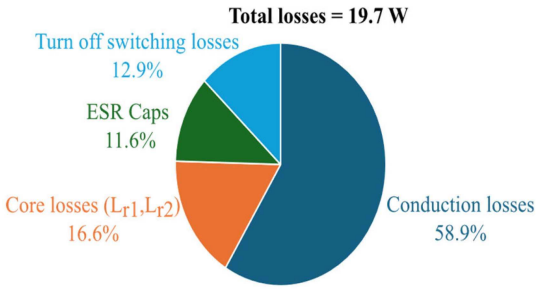


Fig. 24. Loss distribution estimation and thermal image for 1 kw operation.

An estimated loss distribution for a 1 kW power level in the converter is illustrated in Fig. 24. Conduction losses dominate the overall losses, attributed to turn-ON switch resistance ($R_{DS_{\text{on}}}$) and the winding losses for the resonant inductors. Turn-OFF switching losses are the other part of the losses. This study has primarily focused on turn-on losses, making the switching losses in this figure reflective of turn-OFF losses.

Table VIII shows the details of the loss distribution shown in Fig. 24. The conduction losses are mostly related to the switches' conduction losses in each input voltage period. The core losses are related to both resonant inductors. The equivalent series capacitor (ESR) losses contain two types of losses. One type is related to the output filter capacitor. The output electrolytic

TABLE VIII
DETAILED NUMERICAL LOSS DISTRIBUTION IN 1 KW LOAD

Losses	Value	
Conduction losses	Switches conduction losses:	10.613 W
	L_{r1} and L_{r2} winding losses:	0.967 W
Core losses	L_{r1} and L_{r2} core losses:	3.28 W
ESR capacitors losses	Output Capacitors ESR losses:	2 W
	C_{r1} and C_{r2} ESR losses:	0.3 W
Switches turn-OFF losses	Average turn-off losses:	2.54 W

capacitors need to take the second harmonic pulsating power to the output; the other type is resonant inductor capacitors. Those capacitors are ceramic, and they need low ESR to have lower losses during the operation. The turn-OFF switching losses are different at each switching period because of the variable switching frequency in the converter's operation. Because of that, the average switching losses are provided in the table.

Table IX compares the DMRSCR with the other PFC works. This table shows that the DMRSCR can achieve high efficiency compared to the other states of the arts at a high switching frequency range, showing the effect of proper design and achieving ZVS in a wide input voltage range. The DMRSCR has lower voltage stress on the IS compared to the other works. It means that half of the switches can be chosen by lower rated voltage when the converter is needed to operate at higher step-up applications. This table shows that the switching frequency is narrow compared with paper [9] in both full and light load conditions in DMRSCR; it gives the converter a simple digital control design. The DMRSCR results are in a wide range of the input voltage from 120 to 300 V_{rms}. Additionally, the control complexity in the DMRSCR is lower than paper [9] because the proposed model for the DMRSCR is predictive and it does not need any additional control circuit to achieve ZVS.

The topology in [7] is similar to the topology in [9]. The switching frequency is constant in this topology, and the soft switching range is narrow compared with the DMRSCR, and because of that, the efficiency is lower than DMRSCR. Also, the THD and PF ranges are wide from light to full load. The topology used high-value magnetics with an auxiliary inductor. The control complexity is medium because it uses an additional phase-shifting control. In other works in [5] and [6], the full load efficiency in these works is lower than DMRSCR. PF and THD ranges are wide compared to the DMRSCR. Conventional DB boost PFC is shown in [3]. As seen in Table IX, this topology has the same number of switches as the DMRSCR, and it can achieve about 1% lower efficiency because of a lack of control over DB and soft switching. Also, the control complexity system is medium because of an additional current-sharing circuit.

VI. CONCLUSION

This article has introduced a modulation strategy for a DMRSCR to achieve an extensive ZVS for a wide input voltage range besides regulating the output voltage and achieving PFC. The modulation strategy involves adjusting the phase shift ratio, duty cycle ratios, and switching frequency based on the variable input voltage. The phase shift ratio is determined through

TABLE IX
COMPARISON BETWEEN DMRSCR WITH THE OTHER TOPOLOGIES

Reference	Proposed	[6]	[5]	[7]	[9]	[3]
Topology	DMRSCR (Step-up)	Resonant BL PFC (Step-up)	BL boost PFC (Step-up)	BL Totem-Pole (Step-up)	ZVS Totem-pole (Step-up)	Conventional DB Boost PFC (Step up)
Output power	1.1 kW	400 W	850 W	1.6 kW	600 W	1.3 kW
f_{sw} (kHz)	70 – 350 (Full load) 243 – 555 (Light load)	320	65	200	200 – 2400 (Full load) 200 – 4200 (Light load)	100
# switches	8	6	6	6	6	8
Full load Efficiency	98.27 %	95.6 %	96 %	98.05 %	98.7 %	97.4 %
THD range	Narrow (2 - 3.1%)	Wide (15 – 30 %)	Wide (5 – 30%)	Wide (6.83 – 20 %)	Narrow (0.2 – 4 %)	5.8 % (In full load)
PFC range	Narrow (0.992 – 0.999)	Wide (0.94 – 0.98)	Wide (0.88 – 0.99)	Wide (0.955 –0.996)	0.998 (In full load)	0.986 (In full load)
Input voltage range (V_{rms})	120 - 300	220	110	230	230	90 - 264
Output Voltage (V_{dc})	450	400	400	400	400	400
Magnetics cores	2 × 30 μH	2 × 70 μH	1 × 254 μH	2×122 µH + 50 µH	2 (Not reported)	2 (Not reported)
Soft switching range	Wide	Wide	Narrow	Medium	Wide	Not reported
Control Complexity	Low	Low	Low	Medium	High	Medium
Switches voltage stress	$V_{in,max}$ (IS) V_o (OS)	V_o	V_o	V_o	V_o	V_o

closed-loop control, guiding the adjustment of duty cycles to achieve ZVS. Subsequently, the switching frequency is calculated to regulate the output voltage and adjust the magnitude of the resonant inductor current. The article models the dc/dc RSCC first and then extends it to the DMRSCR because the operation of the DMRSCR is such as a dc/dc RSCC with a variable input voltage in each input voltage half cycle. The 1.1 kW experimental prototype is utilized to design constraints, specifying limitations for control parameters to achieve ZVS within a wide input voltage range. The switching frequency is adjusted based on the load (300 W to 1.1 kW), and its variation is about 5x in full loads. The maximum achieved efficiency is 98.27% for the DMRSCR.

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