Challenges in Zero-Voltage-Switched-on Multi-MHz Multi-kW SiC Full-Bridge Inverter and Oriented Design for High-Power Capacitive Power Transfer System

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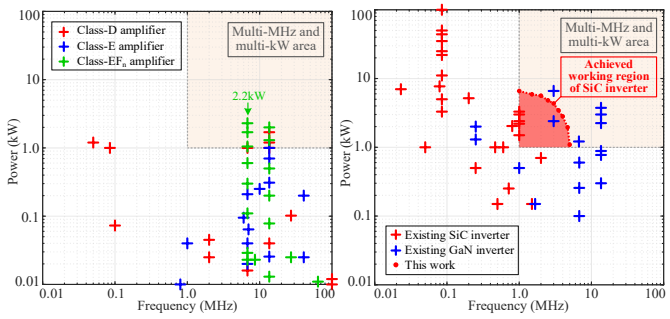
***Abstract*- This paper investigates the challenges in designing and implementing silicon carbide (SiC) full-bridge inverters that operate at multi-MHz multi-kW, aiming at exciting high-power capacitive power transfer (CPT) systems. There are three contributions. First, this paper firstly reveals the drain-source current and voltage oscillations of a zero-voltage-switched-on (ZVS) full-bridge inverter caused by the large hard switching-off current of MOSFET when working at multi-MHz and multi-kW, which emerges as the main challenge that limits the further increase of the switching frequency. Second, a methodology to enhance the high-frequency switching of a full-bridge inverter is explicated in terms of switching device selection, gate-driving circuit design, ZVS realization, and inverter layout optimization. Three inverter examples are respectively implemented based on three commercial gate driver chips, UCC5390, IXRFD631, and UCC27531D with SiC MOSFET C3M0060065K. The implemented inverters can work from 1 MHz at 6.59 kW to 5 MHz at 1.09 kW, which creates new power and frequency records of a SiC full-bridge inverter and points out the ZVS switching limit of 3.5MHz. Third, an impressive 3 MHz 4.34 kW capacitive power transfer (CPT) system is constructed based on the implemented inverters, which achieves a dc-dc efficiency of 94.14% at a distance of 120 mm, validating the proposed multi-MHz and multi-kW SiC full-bridge inverter design and boosting the development of CPT technology.**

***Index Terms*— Silicon carbide (SiC) MOSFET, full-bridge inverter, capacitive power transfer, multi-kW and multi-MHz**

I. Introduction

Recently, capacitive power transfer (CPT) technology has shown good potential in applications of medical equipment, underwater scenarios, and even railway applications [1]-[4].

In a CPT system, the inverter works as the AC power source exciting the alternating electric fields for wireless power transfer (WPT). Considering the proportional relationship between the power transfer capability of a CPT system and the operating frequency and the coupling capacitance, a multi-megahertz (multi-MHz) operating frequency is generally necessary to achieve multi-kW power transfer due to the weak coupling capacitance (picofarad level) of the capacitive coupler in air [5]. Namely, a multi-MHz multi-kW inverter is needed in high-power CPT systems. Recently, benefiting from wide band-gap (WBG) semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN) switching devices, MHz high-power AC power sources have become accessible [6]-[7].



(a) resonant power amplifiers (b) full-bridge/multiphase inverters

Fig.1. Summary of state-of-the-art designs. (a) Power *vs.* frequency of existing power amplifier designs, referring to [8]-[21], [22]-[33], [34]-[51]; (b) Comparison of power *vs.* frequency for SiC- and GaN-based full-bridge/multiphase inverter in a WPT system, referring to [52]-[82], [83]-[100].

An AC source can be realized by two approaches: 1) resonant power amplifiers, such as class-D [8]-[21], class-E [22]-[33], and class-EF$_n$ amplifiers [33]-[51]; 2) full-bridge/multiphase inverter [52]-[82], [83]-[100]. In comparison, a resonant power amplifier usually needs fewer switches with a simpler topology, smaller parasitic parameters, and less complex gate driver circuits. Fig. 1(a) summarizes the performance of existing power amplifiers.

Class-D amplifiers generally use two power switches [8]-[21]. For example, the voltage-mode class-D (VMCD) amplifier is constructed in a half-bridge structure [8]-[16], which has fewer parasitic elements in its power loop than a full-bridge inverter. However, the output AC voltage is decreased by half with the same input DC voltage. Meantime, the high-side switch of a VMCD amplifier still needs an isolated gate driver. The current-mode class-D (CMCD) amplifier consists of two low-side switches with two high-side inductors [17]-[21] which does not require isolated gate drivers. However, the voltage stress of switches is 3.14 times the input DC voltage [17], which is adverse for high-power applications. Ref. [16] has shown a 1.7 kW VMCD amplifier at 13.56 MHz, while Ref. [21] demonstrates a 100 MHz CMCD amplifier with a low power of 12 W.

Class-E amplifiers present good simplicity in both circuit topology and gate driver design by using only one switch at the low side [22]-[33], beneficial to muti-MHz switching. It also has the advantages of zero-voltage switching (ZVS) and accessible zero-voltage derivative switching (ZVDS) for min-

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imal switching loss. The drawback is that the peak voltage on the switch can achieve up to 3.6 times the input DC voltage [37], and the optimal ZVS operation depends on its load condition. The single-switch structure also limits its power level. Refs. [32] and [33] demonstrated state-of-the-art 1 kW and 200 W class-E amplifiers working at 13.56 MHz and 40.68 MHz, respectively.

Class F amplifiers add resonant *LC* tanks to the load network [34] to control the harmonics of the drain-source voltage and current of the switch. Applying this method to a class-E amplifier, a hybrid class-EF_n amplifier is derived [35]-[37], consisting of a class-E topology and an additional *LC* network paralleled to the switch. The subscript *n* refers to the harmonics to which the *LC* resonant network is tuned. The class-EF_2 amplifier, also named Class-Φ_2 amplifier [38]-[51], whose power switch burdens a peak voltage of 2.2 times the input DC voltage [40], has become more attractive than class-E topologies in high-power applications. Ref. [43] presents a 2kW single-end class-EF_2/Φ_2 amplifier working at 13.56MHz. Besides, the push-pull class-EF_2/Φ_2 amplifier is further proposed with a high power capability, and the output power reaches 2.2 kW at 6.78 MHz [44], [45].

Based on Fig. 1(a), power amplifiers with a reduced number of switches facilitate high-frequency operation at multi-MHz. However, it is challenging to further increase its power level because an amplifier usually only contains one or two switches [15], and the voltage stress on the switch may be much higher than the input DC voltage. Furthermore, the output voltage may not be load-independent, e.g., Class-E/EF_n, which is unfriendly for users. Therefore, it is necessary to investigate other alternatives with more switches to enhance the power capability [99], and the full-bridge/multiphase inverter is a candidate as summarized in Fig. 1(b).

Fig. 1(b) shows SiC- and GaN-based full-bridge/multiphase inverters in WPT systems [52]-[82], [83]-[100]. In comparison, a GaN device can switch at high frequency due to its smaller parasitic elements and lower driving voltage range. In the multi-kW and multi-MHz area, GaN-based inverters have been adopted [87]-[88], [98]-[99]. However, gallium nitride material has poorer thermal conductivity than silicon carbide material and the small package size of GaN switches is also adverse for heat dissipation. It means that the SiC devices have better thermal management capability. Due to the small package, GaN-based inverters require an elaborately designed cooling system [88], [99] that increases complexity in a practical implementation. Meanwhile, SiC devices demonstrate higher breakdown voltage than GaN devices due to the larger dielectric constant of materials. For example, the voltage rating of a commercial SiC device can reach 1200V or 1700V, but a GaN device usually operates below 650V. The higher voltage rating facilitates higher power conversion capacity [55]. According to Fig. 1(b), the existing SiC-based inverters mainly work at around 1 MHz or lower frequency, and current applications lack attempts at higher frequencies. Investigation on the limitations of a high-frequency high-power full-bridge inverter is insufficient, meantime, the switching limit of a SiC full-bridge inverter and the boundary between SiC and GaN inverters in multi-MHz multi-kW area is still unclear.

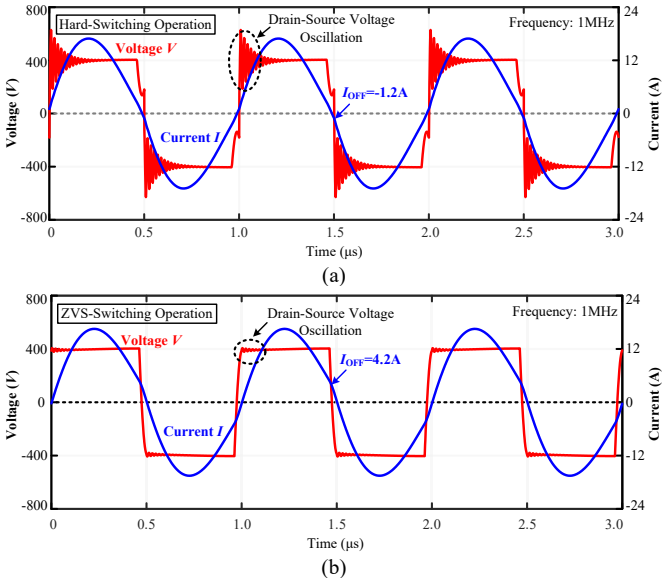

Fig.2. working waveforms of a (a) hard-switched-on inverter; (b) zero-voltage-switched-on inverter.

This paper aims to explore the upper limit of the switching frequency of a SiC full-bridge inverter when working a multi-kW applications and reveal the dominant factors that limit the further increase of the switching frequency. The main contributions are explicated below.

First, compared to the existing work generally focusing on the oscillations caused by hard-switching, this paper firstly reveals the oscillations in a ZVS-operated full-bridge inverter caused by large turn-off current I_{OFF} when working at multi-kW multi-MHz scenarios. The interference of inverter oscillation on the gate driving signals limits the achievement of the higher switching frequency of a ZVS-operated inverter.

Second, this paper is the first to comprehensively analyze, design, and implement SiC H-bridge inverters aiming at multi-kW multi-MHz. The work explicates the methodology to enhance high-speed switching of a full-bridge inverter by device selection, driving circuit design, ZVS realization, and parasitic inductance minimization via PCB layout design, which significantly extends the achievable power and frequency records of SiC inverter with 6.59 kW at 1MHz and 1.09 kW at 5MHz, as shown in Fig. 1 (b). A ZVS switching limit of 3.5MHz of the SiC full-bridge inverter is pointed out.

Third, the implemented inverter is adopted to energize a capacitive power transfer (CPT) prototype, which achieves a record-breaking 4.34 kW power transfer capability at 3MHz with 94.14% DC-DC efficiency.

II. Oscillation Analysis of ZVS-Operated Full-Bridge Inverter

A high-frequency high-power full-bridge inverter is generally required to work with zero-voltage switching-on (ZVS) operation. Apart from reducing switching-on loss, compared to hard switching-on, ZVS operation can eliminate the rush charging and discharging currents of the C_{oss} at turn-on transients (mitigate di/dt and dv/dt), suppressing drain-source current and voltage oscillations of MOSFETs, as shown in Fig.2,

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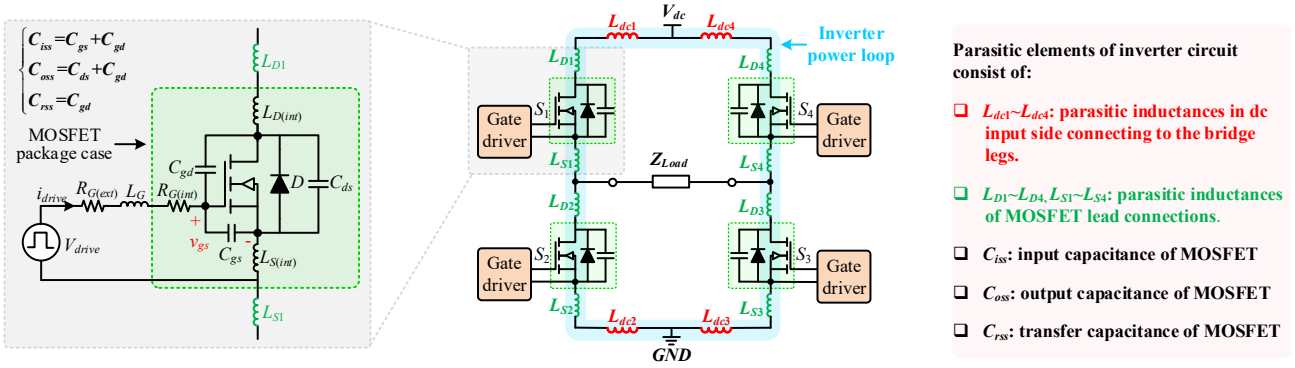

Fig.3. Equivalent circuit model of a full-bridge inverter at high frequency, considering parasitic parameters of circuit components and PCB layout. The dc side inductances L_{dc1} and L_{dc2}, bridge-leg inductances L_{b1} and L_{b2}, and lead inductances L_{D1}~L_{D4}, L_{S1}~L_{S4} should be paid attention to for high-frequency operation.

consequently contributing to clean gate-driving signals and safe operation of the inverter.

However, it is also noted that in a full-bridge inverter, the ZVS turn-on is always accompanied by a hard switching-off in which a positive turn-off current I_{OFF} of MOSFET exists, as shown in Fig.2 (b). When working at a low frequency, e.g. 100kHz, a long dead time T_{dead} can be utilized and a small turn-off current I_{OFF} works well for achieving ZVS, which does not bring about big issues. However, as the switching frequency increases to multi-MHz, the dead time T_{dead} has to reduce accordingly. In this case, a large turn-off current I_{OFF} is inevitable in a ZVS-operated inverter. The increased I_{OFF} means high di/dt in the parasitic inductance during the turn-off transient, meantime, a large I_{OFF} will charge and discharge C_{oss} faster, causing high dv/dt. The large di/dt and dv/dt caused by I_{OFF} jointly aggravate the inverter oscillations despite the ZVS operation, which will significantly endanger the reliability of gate driving signals, emerging as the critical limitation of multi-MHz and multi-kW inverter.

A. High-Frequency Modeling of Full-Bridge Inverter

Fig. 3 shows the high-frequency circuit model of a full-bridge inverter, including four switches S_1~S_4. L_{dc1}~L_{dc4} are parasitic inductances at the DC side, and L_{D1}~L_{D4} and L_{S1}~L_{S4} are parasitic inductances attributed to device leads and circuit traces. C_{gd}, C_{gs}, and C_{ds} are junction capacitances, and $L_{D(\text{int})}$, $L_{S(\text{int})}$, and $R_{G(\text{int})}$ are respectively the internal parasitic inductance and resistance. V_{drive} is the voltage supply for the driver circuit, and L_G is the total parasitic inductance in the driving loop. $R_{G(\text{ext})}$ is an externally added driving resistance.

In Fig.3, when a switching device works at multi-MHz, parasitic parameters are not negligible. $R_{G(\text{int})}$ and C_{gs} slow down the tun-on/off speed and also induce driving power loss. C_{ds} causes difficulty in achieving ZVS in high-frequency operation, resulting in a larger turn-off current. C_{gd} and $L_{S(\text{int})}$ can cause coupling between the control and power sides, inducing interference to gate drivers when high dv/dt and di/dt occur.

B. ZVS Turn-on and Hard-Switching-off Analysis

(1) Switching Transient Analysis

To achieve ZVS, an inductive load is a prerequisite and the inverter MOSFETs will turn off at a positive drain-source current I_{OFF} (namely, hard switching-off), which can fully discharge the output capacitance C_{oss} of the other MOSFET of the same bridge leg that needs to be turned on [4].

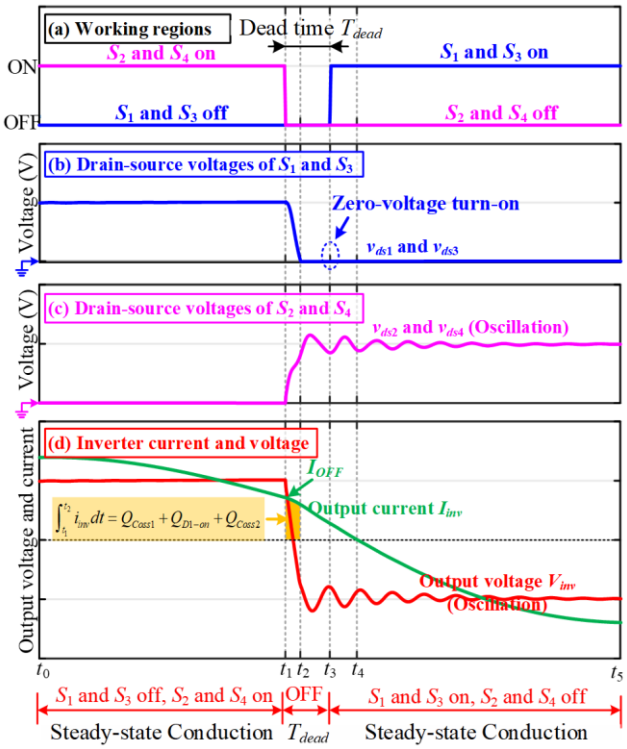

Fig.4. Transient waveforms of ZVS turn-on for S_1 and S_3 and hard switching off for S_2 and S_4.

Fig.4 shows the conceptual transient waveforms of zero-voltage-switched-on S_1 and S_3 accompanied by hard-switched-off S_2 and S_4 as an example. Fig.5 shows the working condition of the inverter at each switching transient while Fig.6 and Fig.7 respectively demonstrate the states of zero-voltage-switched-on S_1 and hard-switched-off S_2.

1) t_0-t_1: At the initial steady-state condition, S_2 and S_4 are conducting while S_1 and S_3 are off-state, shown in Fig.5(a), Fig.6 (a) and Fig.7(a).

2) t_1-t_2: At t_1, S_2 and S_4 start to turn off with a positive current I_{OFF} due to an inductive load, namely hard switching-off. S_1 and S_3 are still off-state, and the inverter enters dead-time duration. Then, I_{OFF} starts to discharge C_{oss1} and C_{oss3} and charge C_{oss2} and C_{oss4}, as shown in Figs.5 (b), 6 (b) and 7(b). At t_1, i_{Coss1}=i_{Coss3}=0 and i_{Coss2}=i_{Coss4}=I_{OFF} are achieved.

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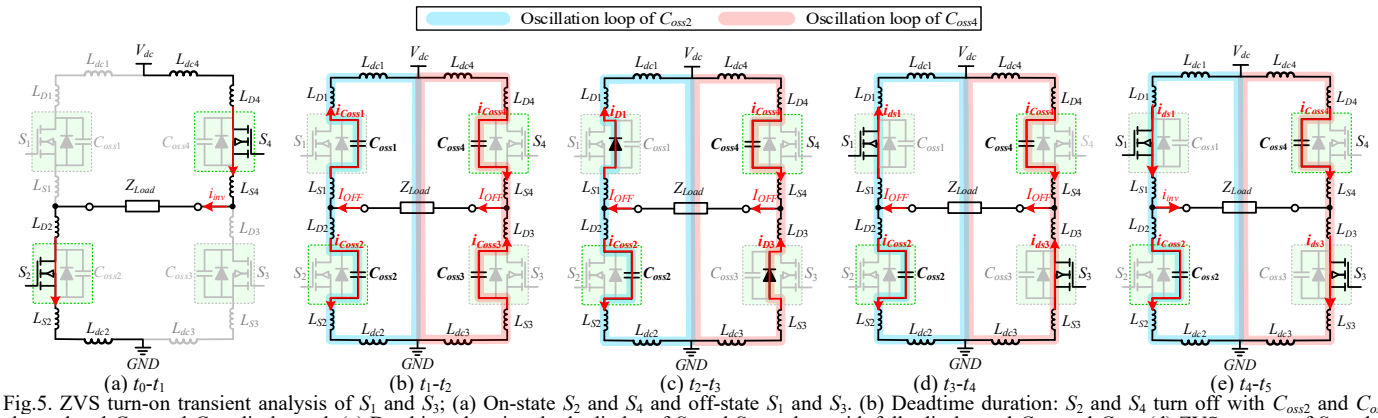


Fig.5. ZVS turn-on transient analysis of S_1 and S_3; (a) On-state S_2 and S_4 and off-state S_1 and S_3. (b) Deadtime duration: S_2 and S_4 turn off with C_{oss2} and C_{oss4} charged and C_{oss1} and C_{oss3} discharged; (c) Deadtime duration: body diodes of S_1 and S_3 conduct with fully discharged C_{oss1} and C_{oss3}; (d) ZVS turn-on of S_1 and S_3 and current commutes from body diode to drain-source channel; (e) Forward conducting S_1 and S_3, and off-state S_2 and S_4.

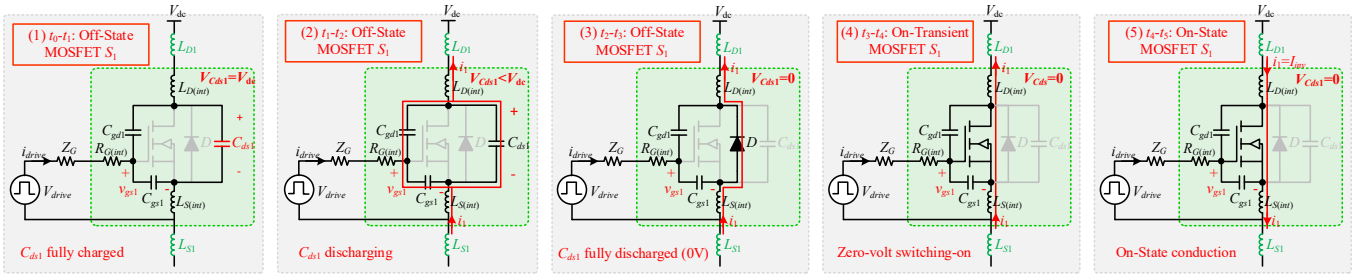


Fig.6 State of MOSFET S_1 during zero-voltage-switching-on transients

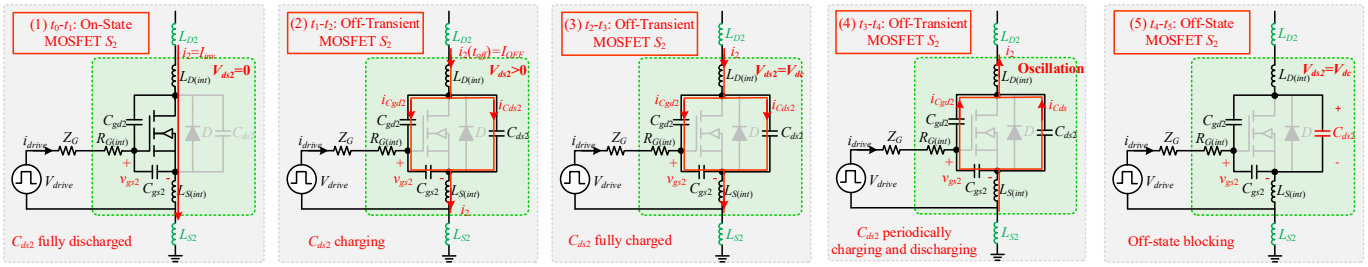


Fig.7 State of MOSFET S_2 during hard-switching-off transients

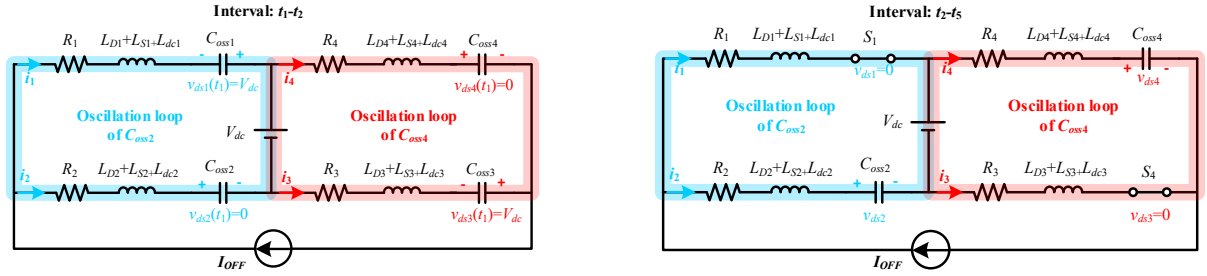


Fig.8. Equivalent charging/discharging circuit of output capacitance during ZVS turn on of S_1, (a) interval t_1-t_2; (b) t_2-t_5, considering parasitic parameters.

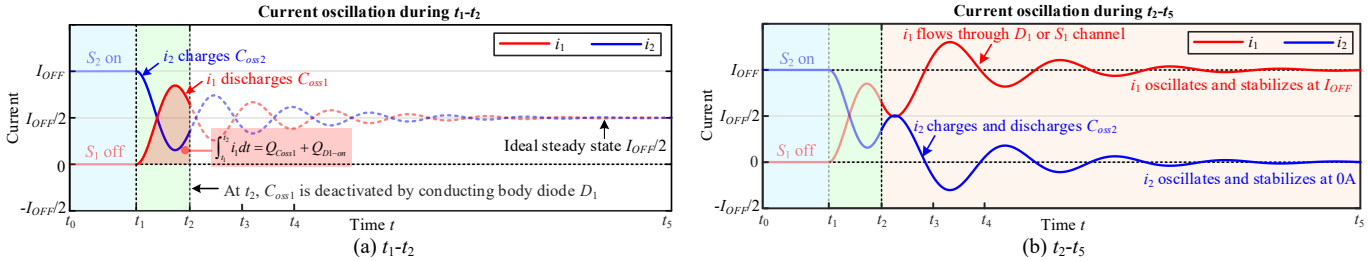


Fig.9. Conceptual waveforms of oscillations in currents i_1 and i_2 during ZVS turn-on transient of S_1, (a) interval t_1-t_2; (b) t_2-t_5, considering parasitic parameters.

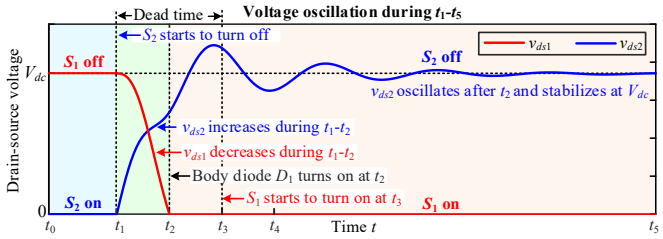


Fig.10. Conceptual waveforms of drain-source voltage of S_1 and S_2 during ZVS turn-on transient of S_1, showing oscillation in S_2 voltage due to parasitic parameters.

Fig.8 (a) shows the equivalent circuit of C_{oss1}~C_{oss4} during t_1-t_2. R_1~R_4 represents the parasitic resistances. The inductive load is considered a current source I_{OFF}. At t_1, i_1=i_3=0 and i_2=i_4=I_{OFF} are initiated. Assuming that the inverter has identical parasitic parameters for each device, it is straightforward to derive the steady state of the circuit in Fig.8 (a):

$$i_1 = i_2 = i_3 = i_4 = I_{OFF}/2 \tag{1}$$

Fig.9 (a) shows the conceptual curves of i_1 and i_2 during t_1-t_2. R_1~R_4 are very small, therefore, the currents will experience attenuated oscillations before stabilizing at I_{OFF}/2.

3) t_2-t_3: As shown in Fig.5, at moment of t_2, C_{oss1} and C_{oss3} fully discharge. Afterward, body diodes of S_1 and S_3 are forced on, and the charging current of C_{oss1} and C_{oss3} commutes to body diodes, as shown in Figs.5(c), 6(c) and 7(c). During t_2-t_3, S_1 and S_3 voltages are clamped by the forward voltage of body diodes, creating a ZVS turn-on condition for S_1 and S_3.

Fig.8 (b) shows the equivalent circuit of C_{oss2} and C_{oss4} during t_2-t_5. The conducting body diodes of S_1 and S_3 deactivate C_{oss1} and C_{oss3}. The steady state of Fig.8 (b) satisfies (2). Similarly, due to small parasitic resistances, i_1~i_4 will oscillate to the steady state, as shown in the conceptual curves in Fig.9 (b).

$$i_1 = i_3 = I_{OFF},\ i_2 = i_4 = 0 \tag{2}$$

4) t_3-t_4: According to Fig.4, at the moment of t_3, S_1 and S_3 start to turn on. During the turn-on transient, the drain-source voltage is clamped to 0V by their body diodes, achieving ZVS turn-on. Then, the current commutes to the drain-source channel from body diodes, as shown in Figs.5 (d) and 6 (d). Figs.8 (b) and 9 (b) show the equivalent circuit and current oscillations during t_3-t_4.

5) t_4-t_5: At t_4, i_2 reduces to 0 and starts to increase in the reverse direction. S_1 and S_3 are on, while S_2 and S_4 are off. In this interval, i_2 and i_4 gradually attenuate to zero after multiple oscillations, and v_{ds2} and v_{ds4} reach the steady value of V_{dc}.

Fig.10 shows the drain-source voltages of S_1 and S_2. During t_1-t_2, v_{ds1} and v_{ds2} monotonously decrease and increase, respectively. After t_2, v_{ds1} is kept at 0V, while v_{ds2} has oscillations. S_3 and S_4 experience the same condition as S_1 and S_2.

(2) Zero-Voltage Switching-on Realization

To achieve ZVS of S_1 and S_3, S_2 and S_4 have to work with hard switching-off, and the I_{OFF} should fully discharge C_{oss1} and C_{oss3}, and charge C_{oss2} and C_{oss4} during dead time T_{dead}, then, turn on body diodes of S_1 and S_3, as shown in Fig.4, which can be described in (3).

$$\int_0^{T_{dead}} i_{OFF}\,dt \geq Q_{Coss1} + Q_{D1-on} + Q_{Coss2} = Q_{rr1} + Q_{Coss2} \tag{3}$$

Q_{Coss1} and Q_{Coss2} are the charge stored in C_{oss1} and C_{oss2}, respectively, given below:

$$Q_{Coss1} = V_{dc} \times C_{oss1},\ \ Q_{Coss2} = V_{dc} \times C_{oss2} \tag{4}$$

$Q_{D1\text{-on}}$ is the required charge to achieve the forward voltage of body diode of S_1. Q_{rr1} represents the reverse recovery charge of the body diode of S_1, which is the sum of $Q_{D1\text{-on}}$ and Q_{Coss1} and can be obtained from the device datasheet.

The average current during dead time is defined as $I_{OFF,\,avg}$. If four devices have identical Q_{rr} and Q_{Coss}, $I_{OFF,avg}$ should satisfy (5) to achieve ZVS operation.

$$I_{OFF,avg} \geq (Q_{rr} + Q_{Coss})/T_{dead} \tag{5}$$

It shows that when working at a low frequency, a large dead time enables a small turn-off current I_{OFF} for ZVS while the dead time reduces as the switching frequency increases, in which the turn-off current I_{OFF} will multiply. For example, for C3M0060065K at 400V, according to [101], Q_{rr} and Q_{Coss} are 151nC and 32nC, respectively. If the frequency is set to 300kHz with a dead time of 200ns, and 3MHz with a dead time of 20ns, $I_{OFF,avg}$ respectively need to achieve 0.915A and 9.15A. The large turn-off current I_{OFF} at high-frequency switching is the main challenge of a ZVS-operated inverter.

Table I. Properties of a 2nd-order dynamic system to model oscillations.

Property	Description	
2nd-order system	$\frac{d^2 f(x)}{d^2 x} + A\frac{df(x)}{dx} + Bf(x) = C$	
Undamped oscillation frequency	$\omega_n = \sqrt{B}$	
Damping coefficient	$\zeta = \frac{A}{2\omega_n}$	
Characteristic roots	$r_1, r_2 = \frac{-A \pm \sqrt{A^2 - 4B}}{2}$	
Solution	1. Overdamped $f(x) = \frac{C}{B} + K_1 e^{r_1 x} + K_2 e^{r_2 x}\ (\zeta > 1)$	No oscillation
	2. Critically damped $f(x) = \frac{C}{B} + (K_1 + K_2 x) e^{r_1 x}\ (\zeta = 1)$	No oscillation
	3. Underdamped $\begin{cases} f(x) = \frac{C}{B} + e^{-\alpha x}(K_1 \cos\omega_d x + K_2 \sin\omega_d x) \\ \alpha = \frac{A}{2}, \omega_d = \frac{\sqrt{4B - A^2}}{2} (0 < \zeta < 1) \end{cases}$	Oscillation

C. Analysis of the Oscillations Caused by Large I_{OFF}

In a ZVS-operated inverter, the MOSFET switches on at a drain-source voltage of zero and switches off at a non-zero drain-source current I_{OFF}. The hard switching-off current I_{OFF} is the root cause of inverter oscillations under ZVS operation. Fig.8 shows the oscillation loops of a full-bridge inverter during t_1-t_2 and t_2-t_5. The oscillation loop for C_{oss1} (C_{oss2}) is analyzed as an example. To simplify the circuit analysis, (6) is introduced.

$$\begin{cases} L_{D1} + L_{S1} + L_{dc1} = L_1, L_{D2} + L_{S2} + L_{dc2} = L_2 \\ L_{D3} + L_{S3} + L_{dc3} = L_3, L_{D4} + L_{S4} + L_{dc4} = L_4 \\ C_{oss1} = C_{oss2} = C_{oss3} = C_{oss4} = C_{oss} \end{cases} \tag{6}$$

(1) Current Oscillation During Interval t_1-t_2

During t_1-t_2, the C_{oss2} oscillation loop is described below.

$$L_1\frac{di_1}{dt}+\frac{1}{C_{oss}}\int_{t_1}^{t} i_1dt+i_1R_1=L_2\frac{di_2}{dt}+\frac{1}{C_{oss}}\int_{t_1}^{t} i_2dt+i_2R_2 \quad (7)$$

At t_1, currents i_1 and i_2 satisfy:

$$i_1+i_2=I_{OFF} \quad (8)$$

During t_1-t_2, i_2 satisfies a 2nd-order dynamic system.

$$\frac{d^2i_2}{d^2t}+\frac{R_1+R_2}{L_1+L_2}\frac{di_2}{dt}+\frac{2}{(L_1+L_2)C_{oss}}i_2=\frac{I_{OFF}}{(L_1+L_2)C_{oss}} \quad (9)$$

The properties of a typical 2nd-order system are summarized in Table I. The undamped oscillation frequency ω_1 and damping coefficient ζ_1 are defined in (10).

$$\omega_1=\frac{1}{\sqrt{(L_1+L_2)C_{oss}/2}},\ \zeta_1=\frac{(R_1+R_2)}{2}\sqrt{\frac{C_{oss}}{2(L_1+L_2)}} \quad (10)$$

Parasitic resistances R_1~R_4 are small, capacitance C_{oss} is about 100pF (95pF for C3M0065065K), and parasitic inductance is in tens of nanohenry (nH), resulting in a damping coefficient ζ_1 below 1.0 as an underdamped system.

According to Table I, in an underdamped condition during t_1-t_2, the current i_2 is expressed below.

$$i_2(t)=\frac{I_{OFF}}{2}+e^{-\alpha_1\cdot(t-t_1)}\cdot[K_1\cos\omega_{d1}(t-t_1)+K_2\sin\omega_{d1}(t-t_1)] \quad (11)$$

The attenuation coefficient α_1 and oscillating frequency ω_{d1} are given as follows.

$$\alpha_1=\frac{R_1+R_2}{2(L_1+L_2)},\ \omega_{d1}=\omega_1\sqrt{1-\xi_1^2} \quad (12)$$

Coefficient K_1 and K_2 are determined by the initial condition of i_2=I_{OFF} and di_2/dt=0 at t_1, given below:

$$K_1=\frac{I_{OFF}}{2},\ K_2=\frac{\alpha_1}{\omega_{d1}}\cdot\frac{I_{OFF}}{2} \quad (13)$$

According to (8), during t_1-t_2, i_1 is expressed as:

$$i_1(t)=\frac{I_{OFF}}{2}-e^{-\alpha_1\cdot(t-t_1)}\cdot[K_1\cos\omega_{d1}(t-t_1)+K_2\sin\omega_{d1}(t-t_1)] \quad (14)$$

During t_1-t_2, i_1 and i_2 respectively oscillate with an initial value of 0A and I_{OFF} at t_1, and both aim to stabilize at I_{OFF}/2. i_3 and i_4 experience the same situation with i_1 and i_2.

Considering (5), (13), and (14), there is a conflict: (5) shows that a large I_{OFF} helps to achieve ZVS, however, (13) and (14) show that I_{OFF} also contributes to current oscillation. Meantime, (12) indicates that the reduction of L_1 and L_2 helps the attenuation coefficient α_1, resulting in a fast attenuation speed.

In addition, Fig. 9 shows that, during t_1-t_2, i_1 and i_2 are always positive. Therefore, there is no drain-source voltage oscillation across C_{oss1} and C_{oss2} during t_1-t_2.

(2) Current Oscillation During Interval t_2-t_5

During t_2-t_5, C_{oss1} is deactivated. The oscillation of C_{oss2} is described below.

$$L_1\frac{di_1}{dt}+i_1R_1+V_{dc}=L_2\frac{di_2}{dt}+\frac{1}{C_{oss}}\int_{t_1}^{t} i_2dt+i_2R_2 \quad (15)$$

According to (8) and (15), the 2nd-order equation of i_2 is:

$$\frac{d^2i_2}{d^2t}+\frac{R_1+R_2}{L_1+L_2}\cdot\frac{di_2}{dt}+\frac{1}{(L_1+L_2)C_{oss}}i_2=0 \quad (16)$$

The undamped oscillating frequency ω_2 and damping coefficient ζ_2 during t_2-t_5 are defined below.

$$\omega_2=\frac{1}{\sqrt{(L_1+L_2)C_{oss}}},\ \zeta_2=\frac{(R_1+R_2)}{2}\sqrt{\frac{C_{oss}}{L_1+L_2}} \quad (17)$$

From Table I, when ζ_2 is below 1.0, i_2 is expressed in (18), showing attenuated oscillation around a steady value of 0A.

$$i_2(t)=e^{-\alpha_2\cdot(t-t_2)}\cdot[K_3\cos\omega_{d2}(t-t_2)+K_4\sin\omega_{d2}(t-t_2)] \quad (18)$$

The attenuation coefficient α_2 and oscillating frequency ω_{d2} during t_2-t_5 are given as follows.

$$\alpha_2=\frac{R_1+R_2}{2(L_1+L_2)},\omega_{d2}=\omega_2\sqrt{1-\xi_2^2} \quad (19)$$

Coefficient K_3 and K_4 are determined by the initial condition of current i_2 at t_2, given below.

$$K_3=i_2(t_2),K_4=[(\frac{di_2}{dt}\Big|_{t=t_2}+\alpha_2\cdot i_2(t_2)]\Big/\omega_{d2} \quad (20)$$

From (8) and (18), during t_2-t_5, current i_1 is expressed as:

$$i_1(t)=I_{OFF}-e^{-\alpha_2\cdot(t-t_2)}\cdot[K_3\cos\omega_{d2}(t-t_2)+K_4\sin\omega_{d2}(t-t_2)] \quad (21)$$

Compared to (10), during t_2-t_5, i_1 and i_2 have a larger damping coefficient ζ_2 and a lower oscillating frequency ω_{d2}.

In (18) and (21), K_3 and K_4 are determined by the initial condition current i_2 at t_2, which have high uncertainty and vary with load. However, the maximum achievable K_3 and K_4 are positively related to the turn-off current I_{OFF}. Namely, a small I_{OFF} helps to suppress current oscillation. Meantime, the reduction of parasitic inductances L_1 and L_2 contribute to a large attenuation coefficient α_2, achieving a fast attenuation speed.

During t_2-t_5, i_2 oscillates around its steady-state value of 0A. It periodically changes its direction, meaning C_{oss2} is frequently charged and discharged, causing the drain-source voltage oscillation on S_2. A similar condition also applies to S_4.

(3) Drain-Source Voltage Oscillation During Interval t_2-t_5

During t_2-t_5, the drain-source voltage v_{ds2} is expressed in (22). According to (22), the voltage oscillation is positively related to parasitic inductance and coefficients K_3 and K_4 (namely, turn-off current I_{OFF}). Increasing C_{oss} can reduce the oscillation amplitude of v_{ds2}. However, a large C_{oss} is adverse for ZVS operation and requires a high I_{OFF}, which increases coefficients K_3 and K_4, deteriorating the oscillation.

From another perspective, at the switching-off moment of S_2, the energy E stored in the parasitic inductances is given by (23). Energy E oscillates between the parasitic inductance and the C_{oss2} of off-state S_2 during dead time with a very low damping coefficient (small resistance), causing drain-source current and voltage oscillations (di/dt and dv/dt). The oscillations because significant at multi-MHz due to a large I_{OFF} for

$$\begin{aligned}v_{ds2}(t)&=V_{ds2}(t_2)+\frac{1}{C_{oss}}\cdot\int_{t_2}^{t} i_2(t)dt=V_{dc}-(L_1+L_2)\cdot e^{-\alpha_2\cdot(t-t_2)}[(K_3\alpha_2+K_4\omega_{d2})\cos\omega_{d2}(t-t_2)+(K_4\alpha_2-K_3\omega_{d2})\sin\omega_{d2}(t-t_2)]\\&=V_{dc}-\sqrt{K_3^2+K_4^2}\cdot\sqrt{\frac{L_1+L_2}{C_{oss}}}\cdot e^{-\alpha_2(t-t_2)}\cdot\cos[\omega_{d2}(t-t_2)-\theta],\quad(\theta=\arccos\frac{K_3\alpha_2+K_4\omega_{d2}}{\sqrt{(K_3^2+K_4^2)(\alpha_2^2+\omega_{d2}^2)}})\end{aligned} \quad (22)$$

ZVS operation.

$$E = \frac{1}{2} L_2 I_{OFF}^2 (L_2 = L_{D2} + L_{S2} + L_{dc2}) \quad (23)$$

The large parasitic inductance L_2, increased turn-off current I_{OFF} for high-frequency zero-voltage switching-on, and the very small damping of the oscillation circuit jointly aggravate the oscillation of a multi-kW and multi-MHz inverter. Therefore, the most effective method to suppress drain-source voltage oscillation is to minimize parasitic inductances of the inverter loop and select the switching device with as small a C_{oss} as possible for reducing I_{OFF} during ZVS.

D. Simulation of Inverter Oscillation

To demonstrate the impact of parasitic inductance of the inverter loop and the turn-off current I_{OFF} on inverter oscillation, LTspice simulation is conducted for a full-bridge inverter with a series RLC resonant network working at 3MHz. Simulation parameters are provided in Table II.

Fig.11 (a) shows simulated voltage and current waveforms at different parasitic inductances and a fixed turn-off current of I_{OFF}=12A. In an ideal condition of zero parasitic inductance in case I, the inverter voltage has no oscillation. In cases II-IV, as the inductance increases, the drain-source voltage oscillations show reduced oscillation frequency, prolonged attenuation process, and aggravated oscillation amplitude.

Table II. LTspice simulation of an C3M0060065K-based full-bridge inverter

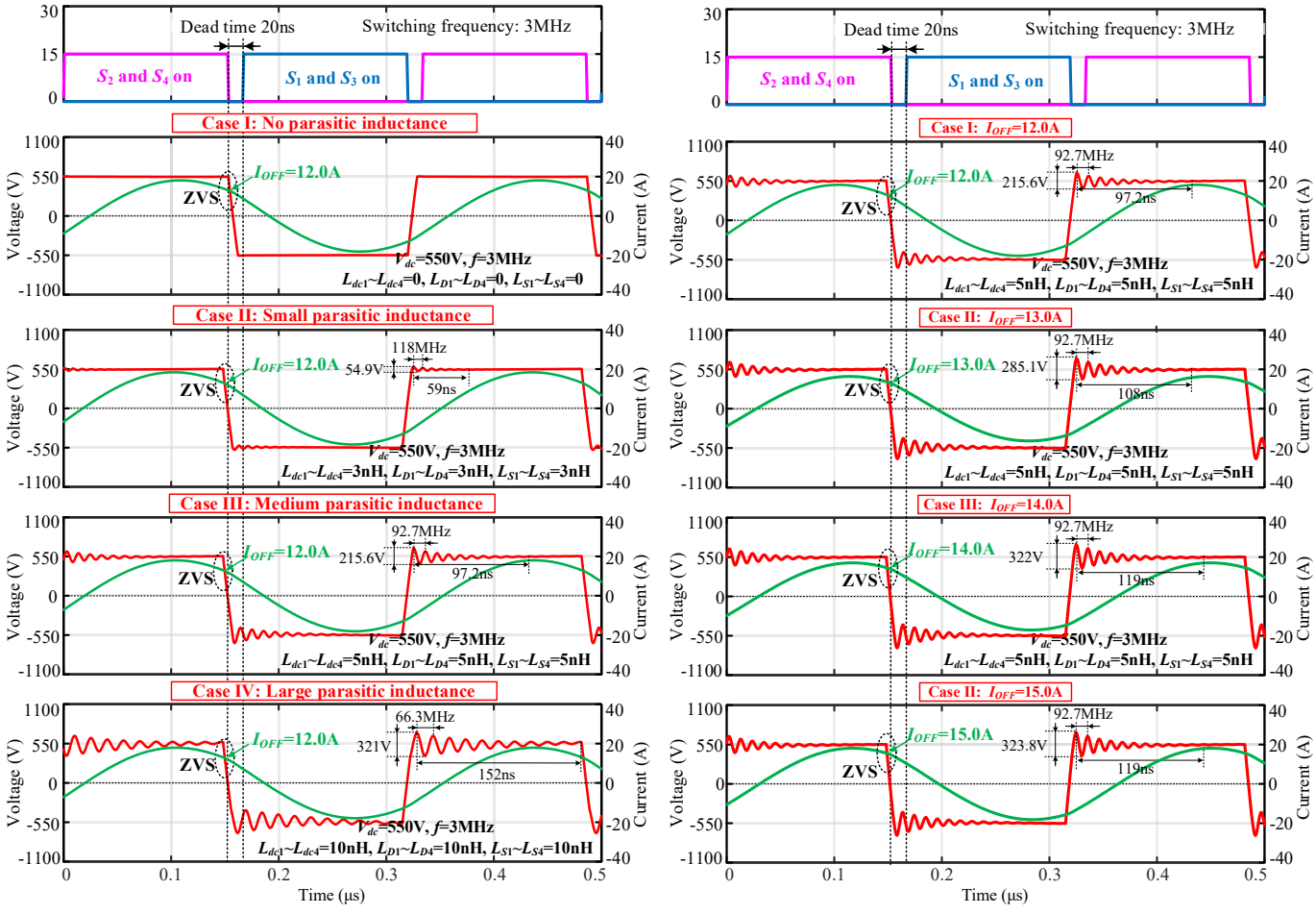
Parameter	Value	Parameter	Value
V_{dc}	550V	f	3MHz
Dead time	20ns	C_{oss} (C3M0060065K)	95pF
I_{OFF}	12.0A~15.0A	L	10μH
R	25Ω~30Ω	C	0.28nF~0.33nF

Fig.11 (b) shows the simulated inverter voltage and current at different turn-off current I_{OFF} with parasitic inductances of L_{dc1}~L_{dc4}=5nH, L_{D1}~L_{D4}=5nH, and L_{S1}~L_{S4}=5nH. It shows that increasing I_{OFF} can deteriorate the oscillation by aggravating amplitude and prolonging attenuation duration.

E. Impact of Inverter Oscillations on Driving Signals

The inverter current and voltage oscillations, namely high di/dt, and dv/dt will also induce oscillation in the gate driving signal via parasitic capacitance C_{gd}, $L_{S(\text{int})}$ which may mistakenly trigger the MOSFETs of the same bridge legs during the dead time and leads to short-circuit failure. Both the inverter oscillations and its interference on the gate driving signal will deteriorate as the frequency increases, which limits the achievement of a higher operating frequency of the inverter.

Fig.12 (a) shows the impact of current oscillation (di/dt) on the gate signal during the turn-off transient of S_2. $Z_G(\omega_d)$ represents the driving loop impedance. The current oscillation



(a) parasitic inductance impact (b) turn-off current I_{OFF} impact

Fig 11. LTspice-simulated inverter oscillation at (a) different parasitic inductances; (b) different turn-off current I_{OFF}, even when ZVS condition is satisfied.

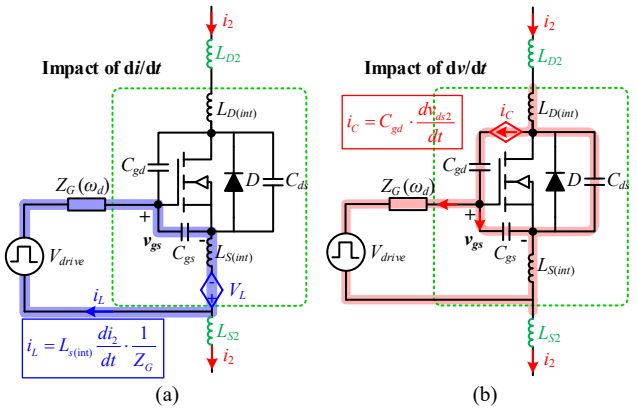


Fig.12. Impact of (a) current oscillation (di/dt); (b) voltage oscillation (dv/dt) on driving signals during the turn-off transient of S_2.

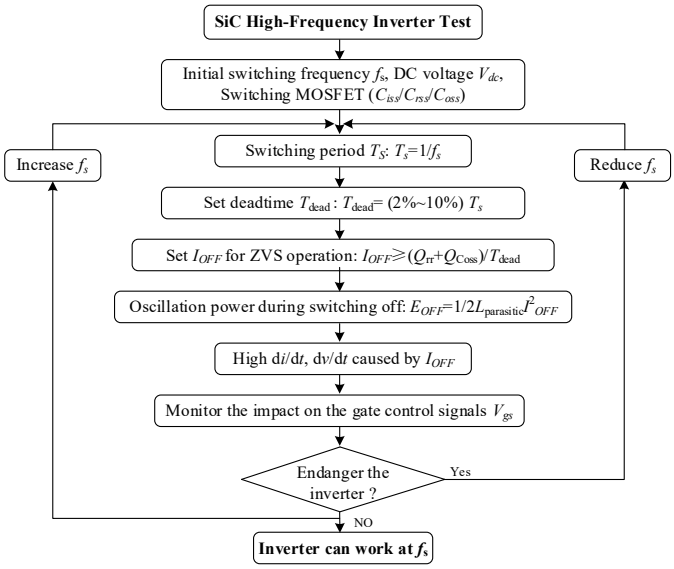


Fig.13 Flowchart of investigating the upper limit of the switching frequency of a ZVS-operated full-bridge inverter.

induces a voltage V_L on the internal parasitic $L_{S(\text{int})}$. V_L can excite a current i_L to charge and discharge the gate capacitance C_{gs}. The gate voltage fluctuation caused by $L_{S(\text{int})}$ is given by (24), which is linearly related to i_2. It also shows that a small $L_{S(\text{int})}$ and a large $Z_G(\omega_d)$ help to suppress $\Delta v_{gs,Ls(int)}$.

$$\Delta v_{gs,L_{S(\text{int})}} = \frac{1}{C_{gs}}\int_{t_1}^{t} i_L dt = \frac{L_{s(\text{int})}}{C_{gs}\cdot Z_G(\omega_d)}[i_2(t) - I_{OFF}] \quad (24)$$

Fig.12 (b) shows the impact of voltage oscillation (dv/dt) on the gate signal. The drain-source voltage oscillation during turn-off can induce an oscillating current i_C via C_{gd}. The gate voltage fluctuation caused by C_{gd} is given by (25), which is linearly related to v_{ds2}. It indicates that a small C_{gd} and a small $Z_G(\omega_d)$ help suppress $\Delta v_{gs,Cgd}$.

$$\Delta v_{gs,C_{gd}} = \frac{1}{C_{gs}}\int_{t_1}^{t} \frac{Z_G(\omega_d)\cdot i_C}{\left|Z_G(\omega_d)+1/j\omega_d C_{gs}\right|}dt = \frac{C_{gd}}{C_{gs}}\frac{Z_G(\omega_d)}{\left|Z_G(\omega_d)+1/j\omega_d C_{gs}\right|}v_{ds2}(t) \quad (25)$$

Based on the theoretical analysis above, to achieve a high-frequency full-bridge inverter and reduce the impact of inverter oscillations on gate signals, four design guidances should be followed.

1. Select the switching device with as small parasitic elements as possible, such as small $R_{G(\text{int})}$ and C_{iss} for fast switching on and off, small $L_{S(\text{int})}$ and C_{gd}, to reduce the coupling between the gate and drain-source side, and small C_{oss} and low reverse recovery charge Q_{rr} to allow a low I_{OFF} for ZVS.

2. Select the specialized high-speed SiC gate driver with high current driving capability and low propagation delays, which is important for multi-MHz switching.

3. Minimize the parasitic inductance of the inverter loop to suppress the current and voltage oscillation of the inverter.

4. Achieve a high $Z_G(\omega_d)$ in the charging path of C_{gs} and a low $Z_G(\omega_d)$ in the discharging path. The failure of a full-bridge inverter is usually caused by the false trigger of turn-on during dead-time duration. A high $Z_G(\omega_d)$ in the charging path of C_{gs} can attenuate the charging current while a low $Z_G(\omega_d)$ in the discharging path allows a high discharging current, which can respectively suppress the impact of di/dt, and dv/dt.

F. Switching Limit of ZVS-Operated Full-Bridge Inverter

According to the abovementioned theoretical analysis, the steps of investigating the upper limit of the switching frequency of a ZVS-operated full-bridge inverter as well as the factors that limit the further increase of the switching frequency are summarized in Fig.13 and elaborated below.

In a full-bridge inverter with a specified switching frequency f_s, DC input voltage V_{dc}, and SiC switching MOSFET (C_{iss}/C_{rss}/C_{oss}), the dead time T_{dead} is generally 2%~10% of the switching period T_s. The turn-off current I_{OFF} is determined by the requirement for zero-voltage switching-on realization specified in (5). When the inverter aims to work at a higher frequency, which means a shorter switching period T_s. Then, the dead time T_{dead} needs to be reduced accordingly, which will cause the increase of turn-off current I_{OFF} to satisfy the ZVS operation. The increased turn-off current I_{OFF} means high di/dt in the parasitic inductance during the turn-off transient, meantime, a large I_{OFF} will charge and discharge C_{oss} faster, causing high dv/dt. The large di/dt and dv/dt caused by I_{OFF} jointly aggravate the inverter oscillations despite the ZVS operation, which may endanger the control signals of gate drivers, limiting the further increase of the switching frequency of the ZVS-operated inverter.

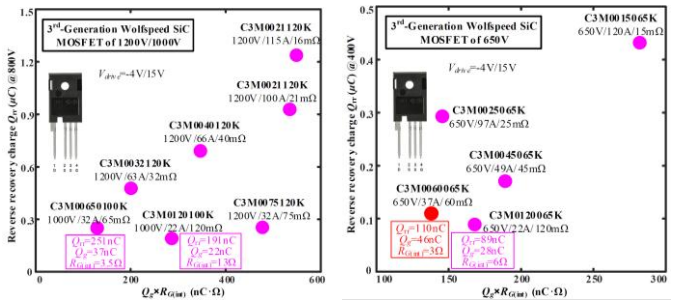
III. Multi-MHz Multi-kW Oriented SiC Full-Bridge Inverter Design and Implementation

To achieve reliable operation of a full-bridge inverter at multi-MHz and multi-kW, it is important to minimize the inverter oscillation to guarantee clean and reliable gate driving signals. The inverter implementation should focus on high-speed switching device selection, high-current driving circuit design, and inverter printed circuit board (PCB) design to minimize parasitic inductance.

A. Switching Device Selection

When selecting the optimal switching devices, two factors are mainly considered: 1) high-speed switching capability; 2) ZVS achievability.

High-speed switching capability aims at short rising/falling time of driving signals. In Fig.3, V_{drive} charges and discharges the gate capacitance C_{iss}, and the driving circuit parameters (L_G, $R_{G(\text{ext})}$, $R_{G(\text{int})}$, and C_{iss}) affect switching speed. With min-



(a) 1200V/1000V series (b) 650V series

Fig.14. Comparison of state-of-art SiC MOSFETs of Wolfspeed, demonstrating $Q_g \times R_{g(\text{int})}$ and Q_{rr} (small value is preferred) for switching device selection.

imized external parameters L_G and $R_{G(\text{ext})}$ by the PCB layout, the switching speed is mainly determined by $R_{G(\text{int})}$ and C_{iss}.

The charging process of C_{iss} during turn-on transient is described by (26). v_{gs} is the transient gate-source voltage and t_r is the rising time during the turn-on transient. It shows that $R_{G(\text{int})}$ and total gate charge Q_g dominate the turn-on/off speed.

$$\int_0^{t_r} \frac{V_{drive} - v_{gs}}{R_{G(\text{int})}} dt = Q_g \Rightarrow \int_0^{t_r} (V_{drive} - v_{gs}) dt = Q_g R_{G(\text{int})} \quad (26)$$

At ZVS operation, C_{oss} needs to be fully discharged, and the body diode is forced on, clamping the drain-source voltage at 0V. Hence, a small C_{oss} and a fast recovery body diode are preferred. Q_{rr} represented the reverse recovery charge of the body diode and the charge stored in C_{oss}. A low Q_{rr} contributes to high ZVS achievability.

Based on the discussion above, two figure-of-merits (FOMs) are derived to select the SiC switch devices for high-frequency switching operation, provided in (27), which respectively represents the switching speed and the ZVS achievability.

$$FOM1 = R_{G(\text{int})} \times Q_g, \quad FOM2 = Q_{rr} \quad (27)$$

Aimed at multi-MHz and multi-kW scenarios, SiC MOSFETs with TO-247-4 packages and Kelvin source terminal are the main candidates due to the excellent heat dissipation capability as well as the minimized common-source parasitic inductance $L_{S(\text{int})}$. Fig. 14 shows a detailed study of 3rd-generation Wolfspeed SiC MOSFETs. A switching device with small $Q_g \times R_{g(\text{int})}$ and Q_{rr} is preferred. 1200V/1000V devices tend to have larger Q_{rr}, Q_g, and $R_{G(\text{int})}$ than 650V devices. Among 650V devices, C3M0060065K and C3M0120065K show better high-speed capability than others. C3M0060065K is selected as an example for multi-MHz and multi-kW inverter demonstration.

B. Multi-MHz Gate Driver Selection

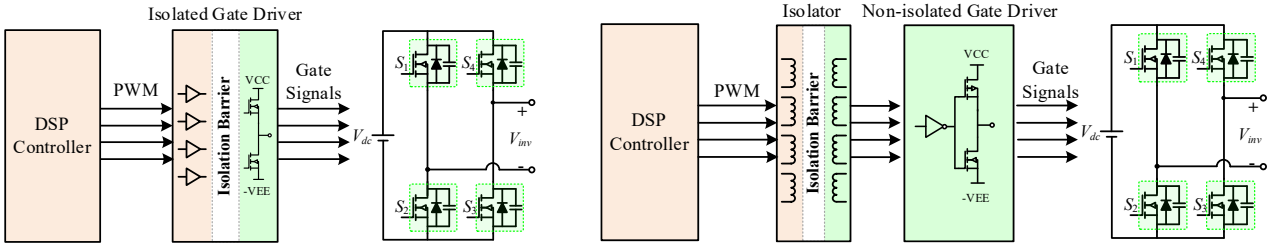
Aimed at muti-MHz switching, high-speed SiC gate drivers with high current driving capability and low propagation delays are preferred. In a full-bridge inverter, high-side switches need to be isolatedly driven. Fig. 15 shows two structures to achieve isolated gate driving for a full-bridge inverter based on isolated and non-isolated gate drivers, respectively. Particularly, the second approach is supported by additional digital isolators at the controller side. Non-isolated gate drivers can achieve a higher driving current, meaning a fast rising and falling transient. Examples of state-of-the-art commercially available gate drivers are compared in Tables III and IV.

When selecting a gate driver, the peak current capability is important. The isolated gate driver UCC5390 and non-isolated gate driver IXRFD 631 can respectively achieve a peak current of 10A and 30A. Meanwhile, the non-isolated gate driver UCC27531 is selected as a comparison. The digital isolator ADuM210N is used together with IXRFD 631 and UCC27531 to achieve signal isolation.

C. Parasitic Inductance Reduction of Inverter Layout

When designing the printed circuit board (PCB) of a multi-MHz multi-kW inverter, parasitic inductance minimization has the highest priority to mitigate the inverter oscillations. Other considerations include isolation and installation of heatsinks.

Fig.16 demonstrates a four-layer PCB layout of the implemented UCC5390-based inverter, which is the optimal inverter PCB design after multiple iterations. Key points for the PCB layout are summarized below.



(a) isolated gate driver (b) digital isolator plus non-isolated gate driver

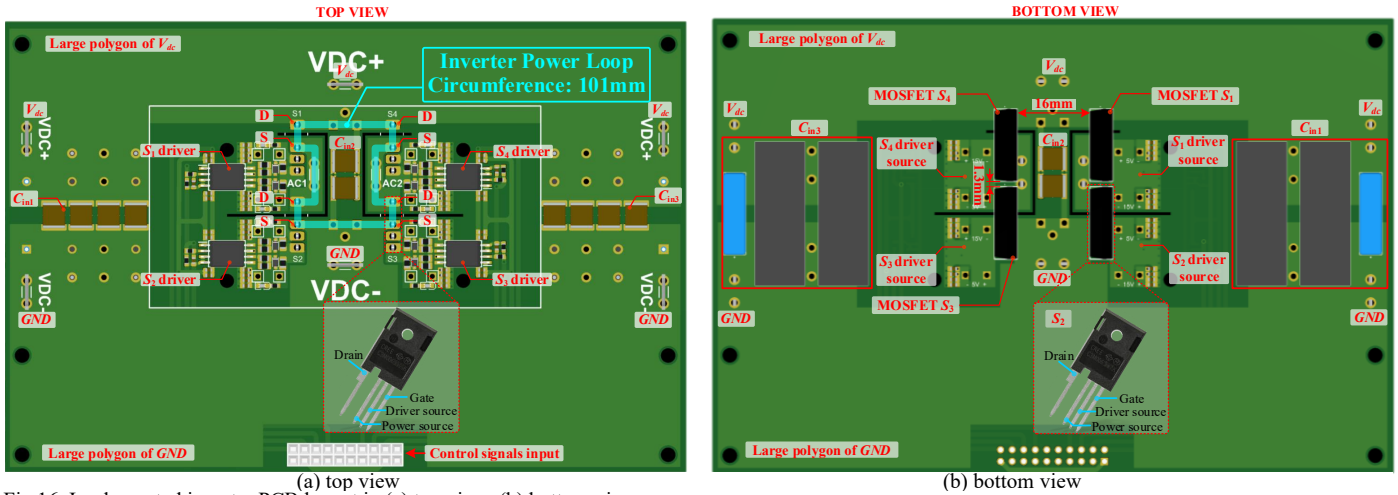
Fig. 15. Gate driving approaches for a full-bridge inverter, considering both isolated and non-isolated solutions.

Table III. State-of-art isolated gate drivers

Isolated driver	Brand	Supply	Isolation	Output type	Output current	Output Rise and Fall Time
ADum3223	Analog	4.5V~20V	Inductive	Dual	4.0A	12ns/12ns @VCC=12V, C_{Load}=2nF
ACPL-P346	Broadcom	10V~20V	Optical	Single	2.5A	8ns/8ns @VCC=10V, C_{Load}=1nF
Si823H9	Skyworks	5.5V~30V	Silicon	Single	4.0A	12ns/12ns @VCC=12V, C_{Load}=200pF
UCC5390	Texas Instrument	13.2V~33V	Capacitive	Single	10A	10ns/10ns @VCC=15V, C_{Load}=1nF

Table IV. State-of-art non-isolated gate drivers

Non-isolated driver	Brand	Supply	Output Type	Output current	Output Rise and Fall Time
UCC27531	Texas Instrument	10V~35V	Single	2.5A (source)/5.0A (sink)	15ns/7ns @VCC=18V, C_{Load}=1.8nF
IXRFD631	IXYS	8V~30V	Single	30A	5.5ns/5ns @VCC=15V, C_{Load}=2nF
IXDD414	IXYS	4.5V~35V	Single	14A	25ns/22ns @VCC=18V, C_{Load}=15nF



(a) top view (b) bottom view

Fig.16. Implemented inverter PCB layout in (a) top view; (b) bottom view.

1) H-Type Compact Configuration. When it comes to minimizing parasitic inductances, H-type configuration is straightforward, in which the V_{dc} and *GND* nets are respectively concentrated. Therefore, the dc-side parasitic inductance L_{dc}~L_{dc8} can be minimized by employing large polygon copper to V_{dc} and *GND* nets. All TO-247 SiC MOSFETs are tightly and vertically mounting of to the PCB board to minimize the lead inductance. Two switches in the same bridge leg are closely placed at a distance of 1.3mm, as shown in Fig.16 (b). The distance between different bridge legs is only 16mm, which is used for the heatsink installation. In Fig.16 (a), the circumference of the inverter power loop is 101mm, which is the minimum achievable length. Based on the finite element analysis (FEA), a low inductance of 35.59nH is achieved in the inverter loop.

2) Distributed DC-Side High-Frequency Filter Capacitors. Filter capacitors are useful to cancel parasitic inductances at dc side, which are placed as close to bridge legs as possible. They are distributed to the double sides and the middle part of inverter legs, shown as C_{in1}, C_{in2}, and C_{in3} in Fig.16. Then, the parasitic inductance distribution is provided in Fig.17. C_{in2} is close to inverter legs to enable a small L_{dc2}, L_{dc3}, L_{dc6} and L_{dc7} in Fig.17. The V_{dc} and *Ground* nets are respectively connected in large copper polygons. The filter capacitors have low equivalent series resistance (ESR) and equivalent series inductance (ESL), and their self-resonant frequency is far larger than the operating frequency.

3) Large Copper Polygon Pouring. Wide trace routing and large copper polygon pouring are helpful to reduce the inductance and resistance of the circuit loop, which also contribute to high current capacity. In the implemented PCB, a large copper polygon is used in V_{dc}, *Ground* (GND), AC output nets as well as the driver source of each switch, as shown in Fig.16.

D. Gate Driver Layout for Driving Capability Optimization

The gate driver circuit design is shown in Fig.18. The paths of source current I_{source} in the turn-on transient and sink current I_{sink} in the turn-off transient are separated by two diodes to regulate impedance. Meantime, ferrite beads (FB) are used, which aim to dampen high-frequency oscillations [102]. The PCB layout of the gate driver circuit is shown in Fig.19, and

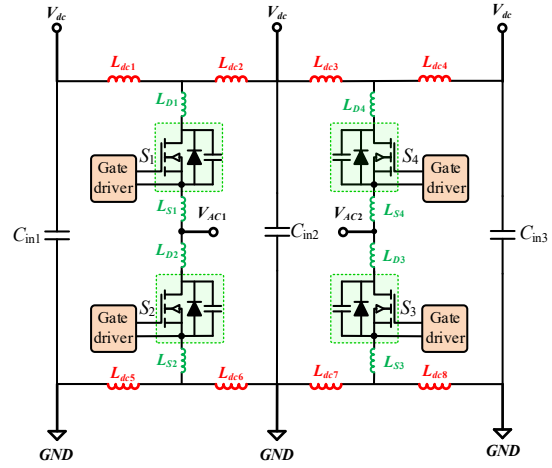


Fig.17. Parasitic inductance distribution of the implemented inverter PCB.

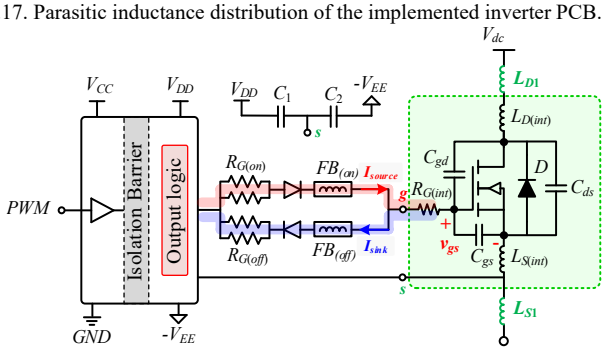


Fig.18. Gate driver circuit design in the implemented inverter.

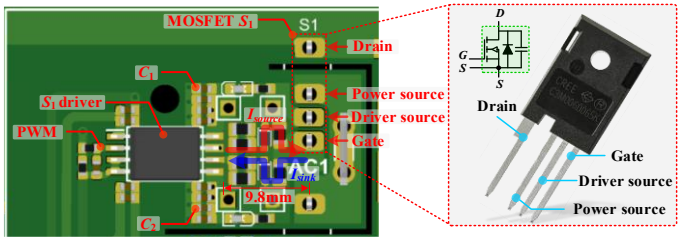


Fig.19. PCB layout of the gate driver circuit.

the key points are summarized below.

1) Short Driving Circuit Loop. To fully enable the peak current driving capability, the driving circuit loop is as short as

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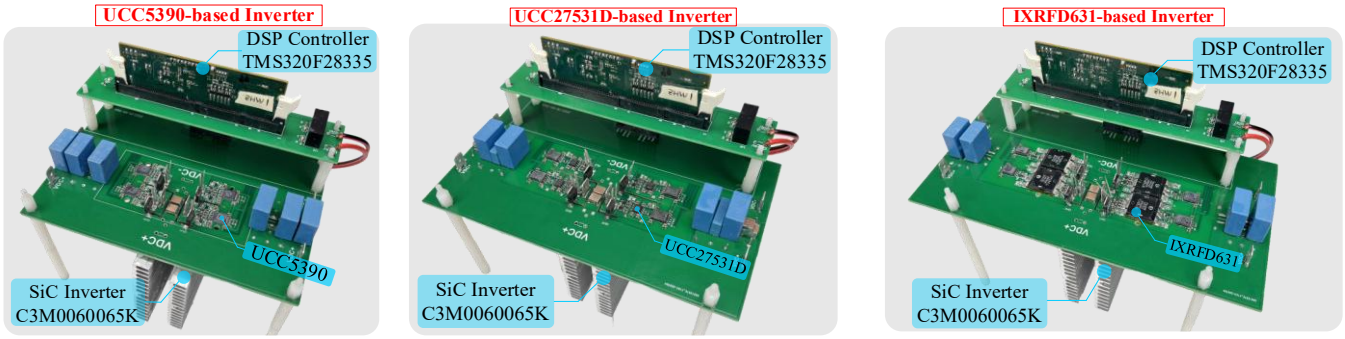
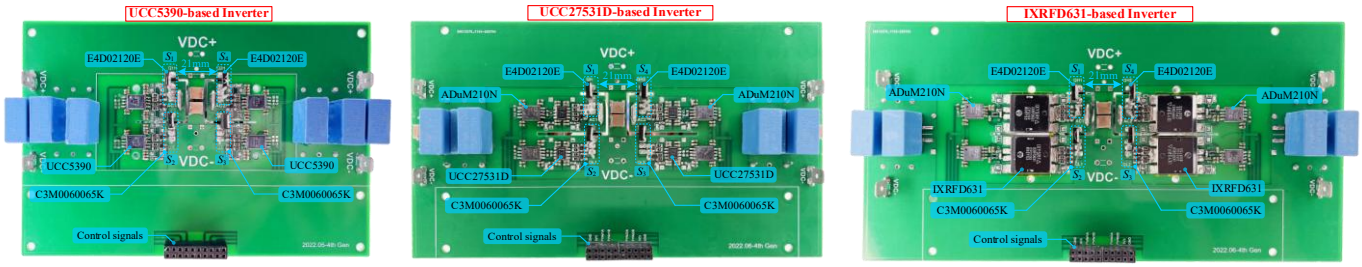


(a) UCC5390 (b) UCC27531 (c) IXRFD631

Fig.20. 3D view of the implemented inverters based on (a) UCC5390; (b) UCC27531; (c) IXRFD631.



(a) UCC5390 (b) UCC27531 (c) IXRFD631

Fig.21. Top view of the implemented inverters layout based on (a) UCC5390; (b) UCC27531; (c) IXRFD631.

possible with low resistance and inductance. The distance from the output lead of the driver to the gate terminal of the switch is minimized to 9.8mm. The returning path is built by large copper polygons in the second, third, and bottom layers to minimize impedance.

2) High-Frequency Capacitor as Gate Driver Power Supply. The gate driver needs to draw/sink up to tens of amperes of current from/in its power supply in several nanoseconds, which requires very low impedance between the driver and its power supply. To achieve this goal, capacitors with low ESR and ESL are used in parallel with the power supply, which are shown as C_1 and C_2 in Fig.18. They should be much larger than the parasitic input capacitance C_{iss}. In the implemented inverter, they are mounted in both the top and bottom layers of the PCB, including 8 paralleled high-frequency ceramic capacitors in a small footprint size of 0603 with 3 different values of 0.1μF, 0.22μF, and 0.47μF to achieve a small impedance, as shown in Figs. 16 and 19.

E. Anti-Parallel Zero-Recovery Diode for ZVS Achievability

The body diode plays an important role in ZVS operation. However, it has a large reverse recovery charge Q_{rr}, which is adverse for ZVS at multi-MHz. Then, zero-recovery SiC diodes can be externally anti-paralleled to deactivate the body diodes and improve the ZVS achievability.

When selecting the anti-parallel diode, low reverse recovery charge and small parasitic capacitance are preferred. With thorough comparison among the state-of-art 6th-and 4th-generation SiC Schottky diodes manufactured by Wolfspeed Inc., finally, E4D02120E [103], which has the minimal junction capacitance and reverse charge, is selected and compared with the body diode of C3M0060065K, as shown in Table V. E4D02120E is a majority carrier diode with a low forward voltage and zero reverse recovery charge. At a reverse voltage of 400V, its parasitic capacitance is only 17pF, and the total reverse charge is 10nC, which is much smaller than 151nC of the body diode. Meantime, the lower forward voltage of 1.4V contributes to deactivating the body diode of C3M0060065K.

Table V. Comparison of E4D02120E and body diode of C3M0060065K

Parameter	Body diode of C3M0060065K	SiC Schottky Diode E4D02120E
Forward voltage	5.1V @25℃	1.4V @25℃
Continuous forward current	23A @25℃	8A @ 25℃
Peak reverse voltage	650V	1200V
Parasitic capacitance	95pF @400V	17pF @400
Total reverse charge	151nC @400V	10nC @400V

F. Implemented Inverter Prototypes

Three inverters are implemented with C3M0060065K based on isolated gate driver UCC5390 and non-isolated gate drivers UCC27531 and IXRFD631, as shown in Figs.20 and 21.

The H-type inverter PCB layout is optimized to minimize the power loop length. Four C3M0060065K are vertically mounted at the PCB bottom side with minimum lead length. Gate drives are placed as close to the switch as possible. The external driving resistance $R_{G(ext)}$ is set at 0 Ω to maximize the driving current. High-impedance and low-impedance ferrite beads are respectively used in charging and discharging paths. E4D02120E is directly mounted to the drain and source terminals of the switch.

IV. Multi-MHz and Multi-kW Inverter Testing

A. Inverter Testing Platform

Fig. 22 shows an RLC series resonant platform to test the multi-MHz and multi-kW inverter. The load resistance R is made of multiple 140W/2Ω non-inductive resistors, and a total resistance is 30Ω. The inductor is fabricated by 6000-strand

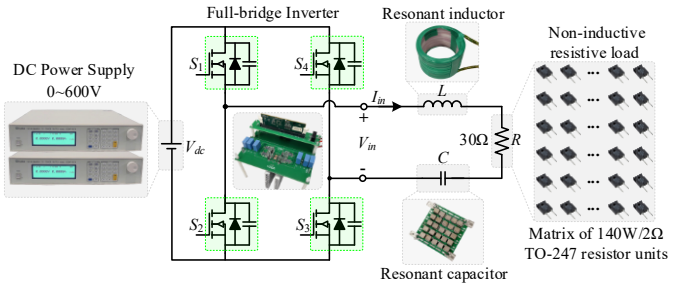


Fig.22. RLC resonant testing platform for multi-MHz and multi-kW inverter.

0.03mm Litz wire. The resonant capacitance is made up of multiple 2.5kV/270pF film capacitors. The inductance and capacitance are adjusted to maintain resonance at different frequencies [104]. Considering the MHz switching frequency, it is challenging to accurately measure the AC output power of the inverter. Therefore, this Section will mainly explore the power conversion capability, ZVS realization, and inverter oscillation of the SiC inverter at multi-MHz range.

B. Inverter Performance at Different Frequencies

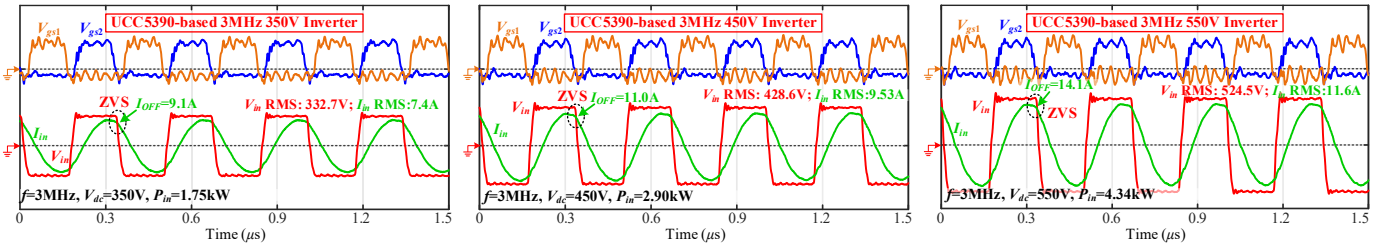
(1) 3MHz Experiments

With a switching frequency of 3MHz, the experimental waveforms of three inverters under different input dc voltages and power levels are provided in Figs.23, 24, and 25.

Fig.23 shows that the UCC5390-based inverter works well at 3MHz with achievable ZVS operation and acceptable gate signals. When the input dc voltage increases to 550V, the output power achieves 4.34kW with a turn-off current I_{OFF} of 14.1A, while the oscillation in the rising edge of V_{in} is still relatively small, which guarantees clean gate driving signals during dead time duration, creating safe working conditions for MOSFETs.

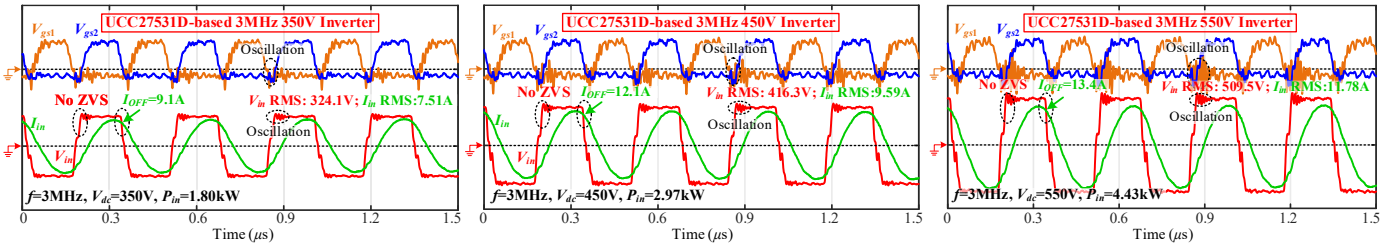
Fig.24 shows waveforms of a UCC27531D-based inverter. Compared to UCC5390, gate signals have much slower rising and falling edges due to the lower driving capability of 2.5A (source)/5A (sink). The lower driving capability also means large impedance $Z_G(\omega_d)$ in the driving loop, which brings about three negative impacts: 1) prolonged time of the operation of the switch in the saturation region, increasing loss; 2) shorter dead time than expected, adverse for ZVS operation. 3) poor suppression of the interference of inverter voltage oscillations (dv/dt) on gate driving signals according to (25). Therefore, due to the reduced dead time, it cannot achieve ZVS turn-on at 3MHz with the comparable turn-off current I_{OFF}. As shown in Fig.24, there are significant high-frequency oscillations (dv/dt) in the rising edge of V_{in} due to the unachieved ZVS turn-on, which induces significant oscillation in gate signals V_{gs1} and V_{gs2}, as shown in Fig.24 (b) and (c). These oscillations in the gate driving signals cause dangerous working conditions, which should be avoided.

Fig. 25 shows waveforms of an IXRFD631-based inverter. It has the highest driving current of 30A (source)/30A (sink), meaning the shortest rising and falling time, which is validated by the driving signals shown in Fig.25. Due to the strong driv-



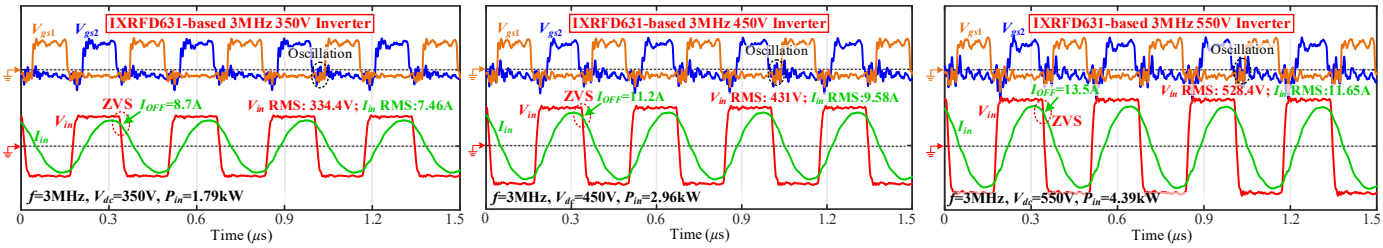
(a) V_{dc}=350V (b) V_{dc}=450V (c) V_{dc}=550V

Fig. 23. 3MHz experimental waveforms of UCC5390-based inverter at (a) V_{dc}=350V; (b) V_{dc}=450V; (c) V_{dc}=550V.



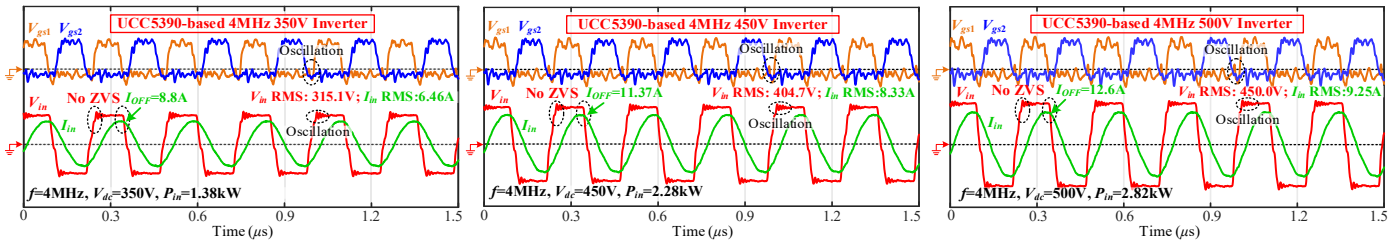
(a) V_{dc}=350V (b) V_{dc}=400V (c) V_{dc}=450V

Fig. 24. 3MHz experimental waveforms of UCC27531D-based inverter at (a) V_{dc}=350V; (b) V_{dc}=400V; (c) V_{dc}=450V.



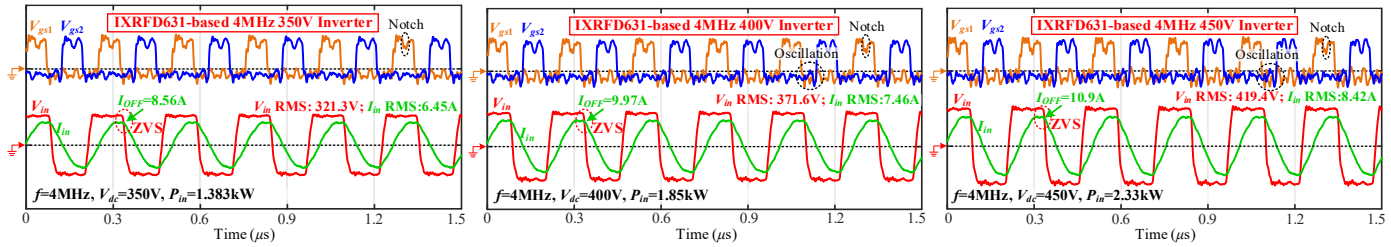
(a) V_{dc}=350V (b) V_{dc}=450V (c) V_{dc}=550V

Fig. 25. 3MHz experimental waveforms of IXRFD631-based inverter at (a) V_{dc}=350V; (b) V_{dc}=450V; (c) V_{dc}=550V.



(a) V_{dc}=350V (b) V_{dc}=450V (c) V_{dc}=550V

Fig. 26. 4MHz experimental waveforms of UCC5390-based inverter at (a) V_{dc}=350V; (b) V_{dc}=450V; (c) V_{dc}=550V.



(a) V_{dc}=350V (b) V_{dc}=400V (c) V_{dc}=450V

Fig. 27. 4MHz experimental waveforms of IXRFD631-based inverter at (a) V_{dc}=350V; (b) V_{dc}=400V; (c) V_{dc}=450V.

ing capability, the effective dead time is enhanced. Working at 3MHz, it can also achieve ZVS turn-on with an input dc voltage of up to 550V, a power level of 4.39kW and a lower turn-off current. However, the high driving capability also means the smaller impedance $Z_G(\omega_d)$ in the driving loop of IXRFD631, which is adverse for resisting the impact of inverter current oscillation (di/dt) according to (24). Therefore, in the IXRFD631-based inverter, the oscillations of the gate-driving signals are mainly caused by current oscillation (di/dt) and deteriorate with an increasing dc voltage and power level, which affects the safe operation.

(2) 4MHz Experiments

To further investigate the performance of the implemented UCC5390 and IXRFD631-based inverters, a 4MHz experiment test is conducted, and the experimental waveforms are shown in Figs. 26 and 27.

As shown in Fig. 26, when the implemented UCC5390-based inverter works at 4MHz, the rising/falling slope of its driving signals becomes more significant, causing a shorter dead time than expected and ZVS operation is no longer achievable. The output voltage is close to a trapezoidal wave, and there are spikes at the rising edge of V_{in}, which induces oscillations in gate signals, which limits the further increment of the power and frequency. With f=4MHz, the implemented UCC5390-based inverter can work with a maximum dc voltage of 500V with a power level of 2.82kW.

Fig. 27 shows the waveforms of the IXRFD631-based inverter at 4MHz. Due to the fast rising and falling slope of gate signals, ZVS operation is still maintained, and the voltage V_{in} is in a nice square shape. As a non-isolated gate driver, the input PWM control signal (0~3.3V) of IXRFD631 shared a common-source ground with its output driving signals, therefore, the interference of the inverter oscillation on gate driving will also be coupled to the input PWM signal via the common source ground. It may mistakenly trigger the input logic threshold of IXRFD631, which accounts for the notch in the driving signals, demonstrated in Fig.27, showing the vulnerability of the non-isolated gate driver when implemented at the high side of the inverter. When the IXRFD631-based inverter works at 4 MHz, it can safely work with an input dc voltage of up to 450V with acceptable notches at gate driving signals. When a dc voltage of 500V was attempted, the gate signals crashed, and two switches in the same bridge leg exploded due to a short-circuit failure.

(3) Comprehensive Comparison of Gate Drivers

Table VI compares three drivers UCC5390, UCC27531D, and IXRFD631. The non-isolated IXRFD631 can achieve the fastest driving speed due to its 30A source/sink capability, which is good for ZVS but shows drawbacks in resisting the inverter current oscillation (di/dt). The non-isolated UCC27531D has a low peak driving current of 2.5A (source)/5A (sink), causing a slow driving speed and difficulty in working at 3MHz or higher switching frequency with ZVS operation. Meantime, the low driving capability of UCC27531D is cause poor immunity to the inverter voltage oscillation (dv/dt). Furthermore, because of the non-isolated features, the input-side PWM signal of UCC27531D and IXRFD631 can be impacted by high dv/dt and di/dt of MOSFET during the switching transient via the common-source ground with its output driving signal. In comparison, UCC5390 has a peak driving current of 10A to support 3MHz ZVS operation, which achieves a good balance between the driving speed and immunity to dv/dt and di/dt. At 4MHz, despite the unavailable ZVS turn-on, the UCC5390-based inverter can still achieve 2.82kW at 500V, showing good reliability, which is considered the optimal one.

It noted that during the high-speed switching operation, the gate input capacitance C_{iss} is periodically charged and discharged, in which the resistance of the driving loop causes significant power loss. The power consumed by driving resistance to turn on and off the device can be estimated as:

Table VI Comparison between UCC5390 and IXRFD631

Gate Driver	UCC5390	UCC27531D	IXRFD631
Type	isolated	non-isolated	non-isolated
Peak current	10A/10A	2.5A/5A	30A/30A
Driving speed	fair	low	fast
Immunity to di/dt	medium	high	low
Immunity to dv/dt	medium	low	high
Reliability	high	fair	fair
Evaluation	★★★	★	★★

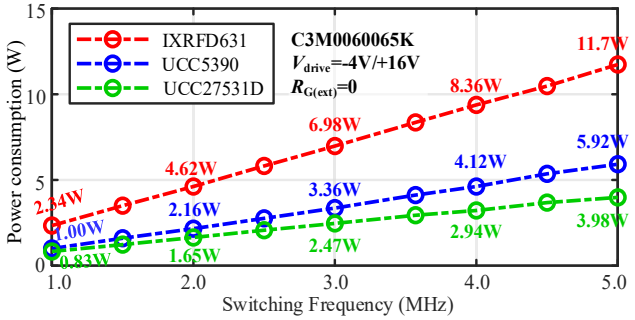


Fig.28. Power consumption of driving circuits versus frequency.

$$P_{drive} = f_s \times \int_0^T v_{drive} i_{drive} dt = \left(V_{drive(\max)} - V_{drive(\min)}\right) \cdot Q_g \cdot f_s \quad (28)$$

f_s is the switching frequency, T is the switching period, Q_g is the total gate charge while $V_{drive(\max)}$ and $V_{drive(\min)}$ respectively represent the steady-state turn-on and -off voltage. The driving power P_{drive} linearly increases with frequency. For example, for the MOSFET C3M0060065K with a driving signal of -4V/15V, according to its datasheet, Q_g is 46nC and the required driving power is calculated as 2.62W at 3MHz and 3.5W at 4MHz, respectively. P_{drive} is only the power consumed by driving resistance. The total power consumption of the driving circuit should be higher due to the additional loss of internal components and circuits of gate driver chips.

To satisfy the power demand of the driving circuits working at multi-MHz, in the presented inverter design, the positive gate driver supply is constructed by an externally connected 4-series-3-parallel Li-ion battery with a nominal voltage of 14.8 V (maximum 16.8V), and the negative gate driver supply is constructed by a 1-series-4-parallel Li-ion battery with a nominal voltage of 3.7V (maximum 4.2V). Then, the +14.8V/-3.7V gate driver supply is achieved, which can satisfy the power requirement as well as achieve high-side isolation.

Fig. 28 provides the power consumption of the three kinds of driving circuits working for a single MOSFET C3M0060065K. The power is mainly distributed on the gate driver chip, externally connected driving resistance, and the internal gate resistance of MOSFET. It indicates that the power consumption of the driving circuit almost linearly increases with frequency. At the same switching frequency, the driving circuit with higher driving capability tends to consume more power. The increased driving power at multi-MHz frequency will cause a significant temperature rise of gate driver chips, which may affect the functionality of the gate driver and therefore requires a proper cooling system.

In the presented inverter design, To mitigate the thermal issues of gate drivers, two methods are adopted: 1) aluminum heatsinks are attached to the surface of the gate driver chip; 2) forced air cooling is achieved by a 12V/2.5A fan. With an implemented cooling system, the implemented inverter can work reliably under 3MHz.

C. *Achievable Power Conversion Capability*

The UCC5390-based inverter tends to have optimal overall performance, considering speed, reliability, and power consumption. Then, the switching limit and power capability are explored from 1MHz to 5MHz, as shown in Fig.29.

The UCC5390-based inverter can still realize ZVS up to 3.5MHz. With an input dc voltage of 550V, it can achieve 6.59kW at 1MHz and 3.45kW at 3.5MHz. To maintain safety, the voltage reduces to 500V at 4MHz and 450V at 5MHz, and the power reaches 2.82kW and 1.09kW, respectively. Overall, the inverter power reduces with increasing frequency.

To achieve ZVS turn-on, an inductive load is needed, in which the inductive reactive power Q from the load is utilized to cancel the capacitive reactive power of the parasitic drain-source capacitances of the switch. As the frequency increases,

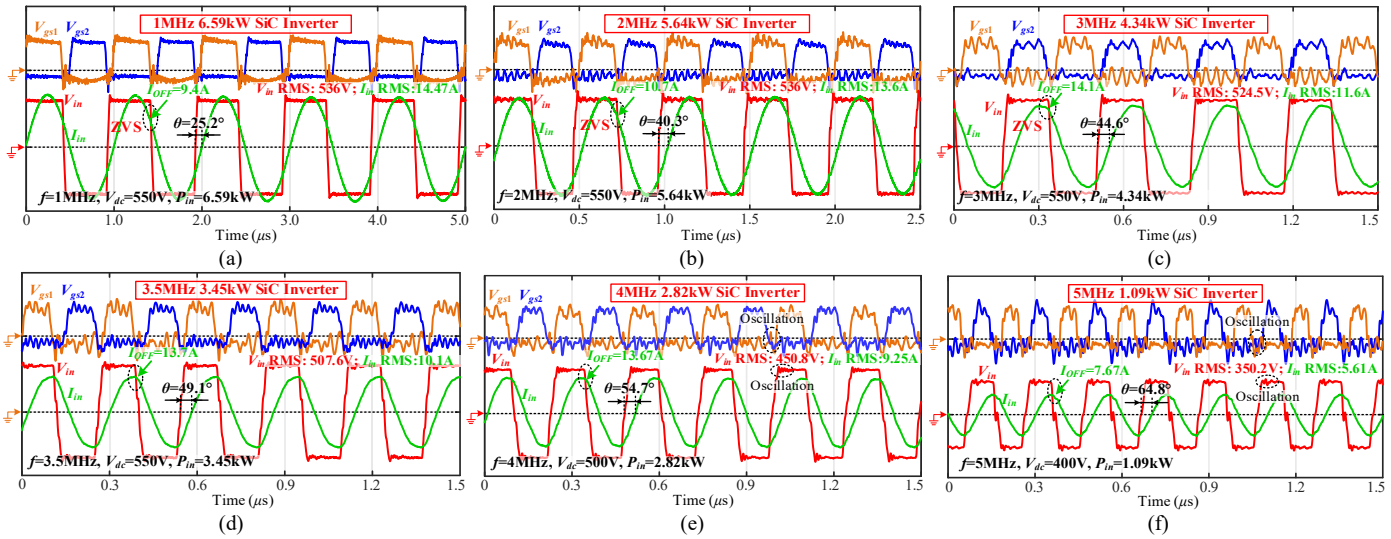


Fig. 29. Experimental waveforms of the implemented multi-kW multi-MHz inverter at (a) 1MHz and 6.59kW; (b) 2MHz and 5.64kW; (c) 3MHz and 4.34kW; (d) 3.5MHz and 3.45kW; (e) 4MHz and 2.82kW; (f) 5MHz and 1.09kW. (At 5MHz, UCC5390 has overheating issue and IXRFD631-based inverter is used.)

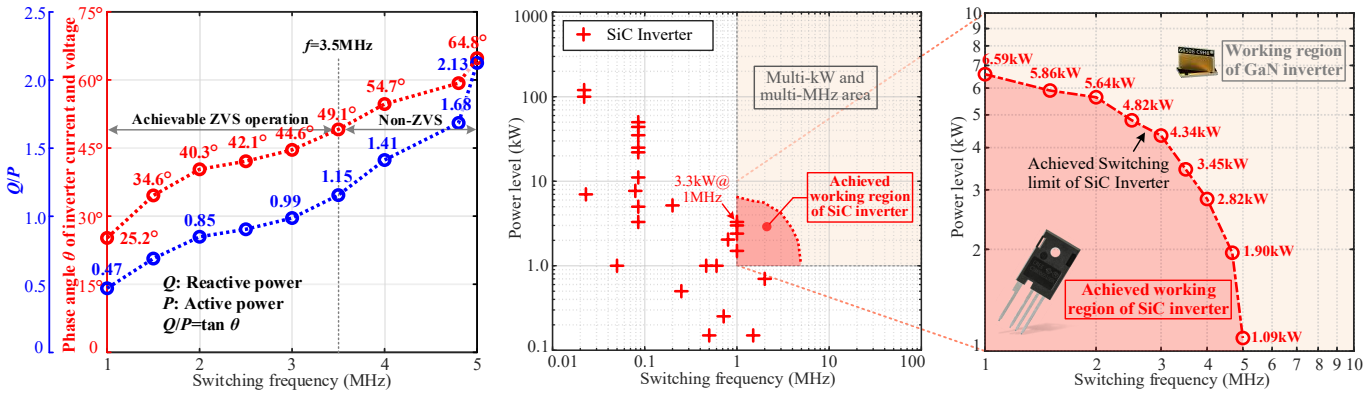


Fig.30. (a) Phase angle between inverter voltage and current; (b) Performance of existing SiC inverter; (c) Achieved working region of implemented SiC inverter

Table VII. Design challenges of a multi-kW multi-MHz full-bridge inverter (Example quantification based on experimental results in Fig. 29)

Challenges	Description	Quantification based on Fig.29	Impacts
1. High dv/dt and di/dt	$dv/dt = V_{dc}/t_{off}$ $di/dt = I_{OFF}/t_{off}$	dv/dt=550V/10ns=55V/ns di/dt=14.1A/10ns=1.41A/ns	Induce rush current injected into C_{gs} via C_{gd} and rush voltage on the gate driving loop via $L_{S(int)}$
2. Difficulty in ZVS realization	$I_{OFF,avg} \geq (Q_{rr}+Q_{Coss})/T_{dead}$	$I_{OFF,avg} \geq 10A @ T_{dead} = 10ns$	Require a large I_{OFF} due to short dead time T_{dead}, aggravating di/dt and inverter oscillation
3. Oscillation under ZVS operation	$(\Delta i, \Delta v) \propto (I_{OFF}, L_{Loop})$	$\Delta v_{peak\text{-}peak}$=107V @101MHz	Deteriorate gate driving signals by inducing oscillations
4. High power demand of driving circuit	$P_{drive} = \Delta V_{driver} \cdot Q_g \cdot f_s$	3.36W @UCC5390 6.98W @IXRFD631	Cause difficulty to isolated gate driver supplies design and gate driver cooling may be required.

the required Q from the load also rises, inducing an increasing phase angle θ between inverter current and voltage, as shown in Fig.30 (a). The ratio between inductive reactive power Q and the real power P in the load network is also provided.

The comparison between the achieved working region and the existing SiC inverters is shown in Figs.30 (b) and (c). The previous work focuses on 1MHz or lower frequencies, which leaves a large technical gap in the multi-kW and multi-MHz areas. Investigation on the limitations of a high-frequency high-power full-bridge inverter is insufficient, meantime, the switching limit as well as the safe working region of a SiC full-bridge inverter in the mult-MHz multi-kW area are unclear. This work explored the frequency limit of the SiC inverter up to 5MHz. It creates new power and frequency records for the SiC full-bridge inverter and further extends its safe working region.

D. *Summary and Quantification of Challenge In Multi-MHz Multi-kW Inverter*

Based on the presented analysis and experimental work, the design challenges in a multi-MHz and multi-kW SiC inverter are summarized in Table VII and explained below:

1) Due to the minimized parasitic input capacitance C_{iss} of switching devices and the high-speed gate driver, the turn-on and turn-off transients of the MOSFETs in a multi-MHz inverter are significantly shortened, which means a high dv/dt and di/dt, posing challenges to the isolated gate driver.

2) The reduced dead time in multi-MHz switching causes difficulty in achieving ZVS, and a large turn-off current I_{OFF} is required for ZVS operation.

3) The large I_{OFF} and uneliminated parasitic inductance L_{Loop} of the inverter loop can induce drain-source current and voltage oscillations despite achievable ZVS operation, which endangers the reliability of the gate driving signals and limits the achievement of the higher switching frequency.

4) The power consumption of gate driving circuits linearly increases with switching frequency, posing challenges to isolated gate driver supplies design, and incurring the thermal issue of gate drivers.

E. *Recommendations for Higher-Power and Higher-Frequency Inverter Design*

The paper reveals that the parasitic inductance of the inverter loop, parasitic C_{oss} of MOSFET, and the large turn-off current I_{OFF} under high-frequency ZVS operation are the root causes for inverter drain-source current and voltage oscillations, which emerge as the critical limitation in the multi-MHz and multi-kW switching operation via endangering the reliability of gate driving signals. Prior to this work, although it was known that the GaN-based inverter outperforms the SiC inverter in higher switching frequency, however, the switching limit of SiC inverters is unclear. Based on plenty of experimental tests, this work points out the ZVS switching limit of 3.5MHz of the SiC full-bridge inverter, and the implemented ZVS-operated SiC inverter can achieve 6.59kW at 1MHz and 4.3kW at 3MHz, which has further extended the working region of the SiC full-bridge inverter in the multi-MHz and multi-kW range. Therefore, when a high-frequency and high-power AC power source is needed and the required switching frequency is lower than 3.5MHz, the SiC full-bridge inverter is still a competitive solution. due to the better thermal performance and the lower requirement for the cooling system.

To further make a breakthrough, the future direction should focus on GaN switching device-based inverter design. GaN devices have smaller packages, smaller parasitic lead inductance, and junction capacitances than the SiC switching device, which contributes to improving the inverter oscillations and lowering I_{OFF} for ZVS operation. Meantime, the typical driv-

ing signal for GaN switching device is -3V/+6V, which is much lower than that of a SiC device of -5V/+15V, reducing the power requirement of the gate supply and mitigating the thermal issue of gate driving circuits. Meantime, it is noted that the small package of the GaN device brings about poor thermal dissipation performance. Therefore, a GaN-based inverter requires an elaborately designed cooling system for high-power applications, such as liquid cooling [99], which needs to be taken into consideration in practical implementation.

V. Implementation of 3MHz 4.3kW CPT Prototype

A. 3MHz High-Power CPT System Design

Based on the implemented inverter, a 3MHz CPT system is implemented, aiming at achieving record-breaking power and efficiency. The adopted CPT circuit is shown in Fig.31, which has been analyzed in [105]. It uses double-sided series-parallel (SP) IPT links to boost the plate voltage V_1 and V_2, enabling a high power transfer capability.

For the capacitive coupler, the mutual capacitance C_M and self-capacitances C_1 and C_2 satisfy:

$$\begin{cases} C_M = C_{M1} \cdot C_{M2} / (C_{M1} + C_{M2}) \\ C_1 = C_{12} + C_M, C_2 = C_{34} + C_M \end{cases} \tag{29}$$

The circuit resonance relationship satisfies:

$$\omega = \frac{1}{\sqrt{L_{f1} C_{f1} (1 - k_1^2)}} = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} = \frac{1}{\sqrt{L_{f2} C_{f2} (1 - k_2^2)}} \tag{30}$$

In the double IPT links, k_1 and k_2 are coupling coefficients and mutual inductance are defined as L_{M1} and L_{M2}, given as:

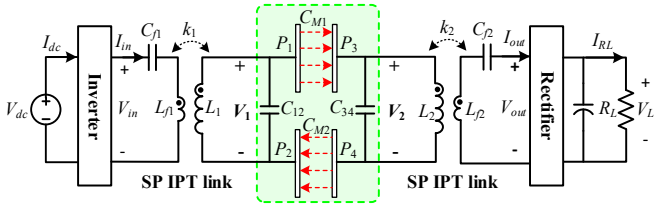


Fig.31. Circuit topology of the adopted capacitive power transfer system.

Table VIII. Parameters of the implemented 3MHz CPT prototype

Parameter	Value	Parameter	Value
V_{dc}	550 V	f	3 MHz
MOSFET	C3M060065K	Diode	C6D04065A
L_{f1}	3.34 μH	C_{f1}	2.48nF
L_{f2}	3.32 μH	C_{f2}	0.90nF
L_1	48.7 μH	L_2	48.3 μH
k_1, k_2	0.45	L_{M1}, L_{M2}	5.7 μH,
C_{M1}, C_{M2}	46.0pF	C_{12}, C_{34}	35.0pF
C_M	23.0 pF	C_1, C_2	58.0pF
Air gap	120 mm	k_C	0.40

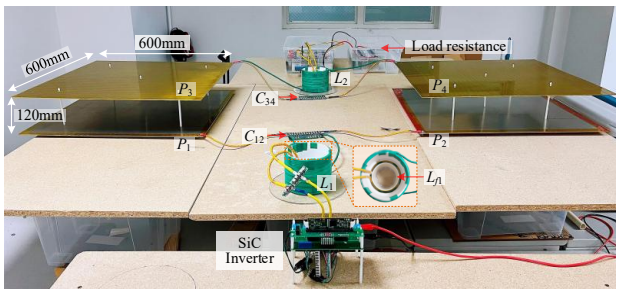


Fig.32. Implemented 3MHz CPT prototype with the proposed SiC inverter.

$$L_{M1} = k_1 \sqrt{L_1 \cdot L_{f1}}, \quad L_{M2} = k_2 \sqrt{L_2 \cdot L_{f2}} \tag{31}$$

According to [103], the output power P_{out} is given as:

$$P_{out} = V_{out} I_{out} = V_1 V_2 \omega C_M = V_{in} V_{out} \omega C_M \cdot \frac{L_1 L_2}{L_{M1} L_{M2}} \tag{32}$$

Table VIII provides the 3MHz CPT system parameters, and Fig. 32 shows the CPT prototype. The UCC5390-based inverter is used with SiC MOSFET C3M0060065K. The rectifier is implemented based SiC diode C4D04065A. All inductors are fabricated by 6000-strand 0.03mm Litz wire. For the double-sided SP IPT links, primary coils (L_{f1} and L_{f2}) are inside the secondary ones (L_1 and L_2), achieving a coupling coefficient of 0.45. RF ceramic capacitors of Vishay HIFREQ series are used to construct C_{f1}, C_{f2}, C_{12}, and C_{34}. The capacitive plate has a size of 600mm × 600mm. With a transfer distance of 120mm, C_M is 23pF, and a coupling coefficient of 0.4 is designed.

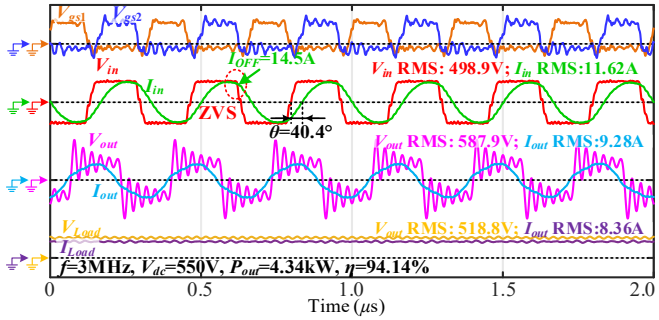


Fig.33. Experimental waveforms at 3MHz and 4.34kW power transfer.

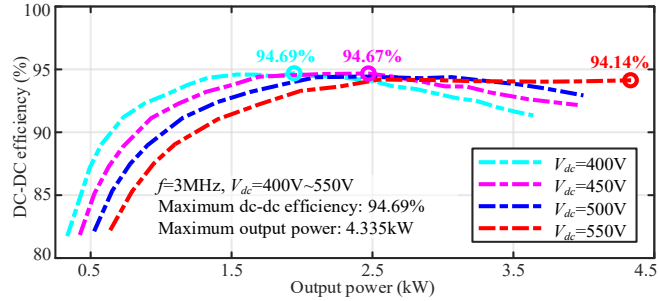


Fig.34. Measured dc-dc efficiency of the implemented CPT system.

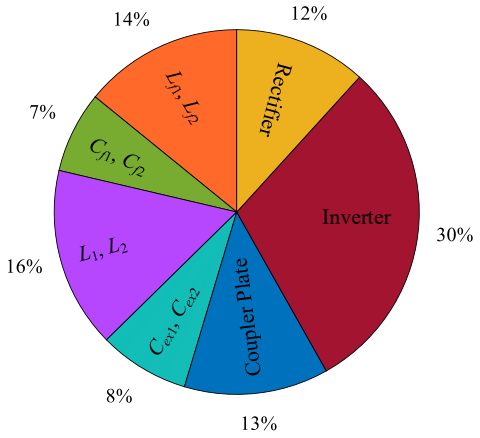


Fig.35 Power loss distribution in CPT components at 4.34kW.

B. 4.34kW Capacitive Power Transfer

Fig.33 shows the experimental waveforms at 3MHz and 4.34kW with a dc input voltage of 550V. The inverter current I_{in} lags V_{in} by 40.4° to achieve ZVS and the turn-off current I_{OFF} achieves 14.5A. The rectifier current I_{out} slightly leads V_{out}, which is attributed to the parasitic capacitance of rectifier diodes. The oscillation of the ac output voltage V_{out} is the measurement error caused by the parasitic inductance of the extension wire of the voltage probe.

Fig. 34 shows the dc-dc efficiency of the CPT system at different input dc voltages and load conditions, which considers the power loss in the inverter and rectifier. The dc-dc efficiency reaches 94.14% at the highest output power of 4.34kW, and the maximum efficiency achieves 94.69% when the DC voltage is 400V and the power is 1.94kW.

With f=3MHz, V_{dc}=550V, and P_{out}=4.34 kW, the power loss distribution among circuit components in the implemented CPT system is provided in Fig.35. Particularly, the inverter loss takes up 30% of the total power loss, around 81W, which is significantly higher than others. The loss on compensation inductors is slightly higher than that in compensation capacitors. The coupler plate dissipates 13% and the rectifier accounts for 12% of the power loss. In this case, the DC-AC efficiency of the implemented SiC inverter is estimated to be 98.2%.

C. Comparison with The State-of-Art CPT Works

A comparison with existing state-of-art CPT designs in terms of power, efficiency, operating frequency, and voltage stress, is provided in Table IX and Fig.36.

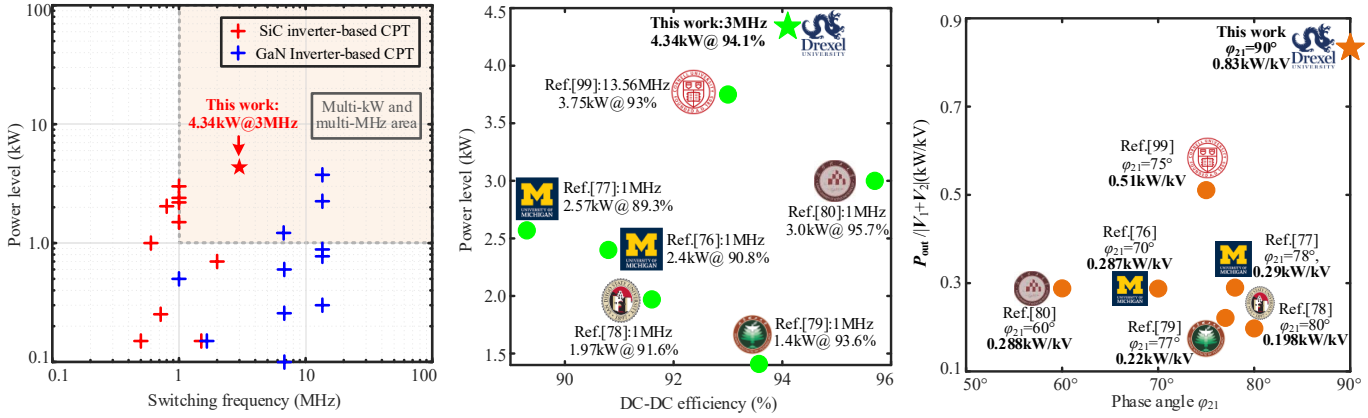
The CPT systems presented in [76]-[80], [99] are all developed from SS CPT compensations with double-sided high-order circuits. References [76]-[78] presented the early-stage high-power CPT design, which achieves a power level of below 3kW and an efficiency of around 90%. Based on these works, in 2019, Li et al. improved the LCLC-LCLC CPT system and achieved an efficiency of 93.57% at a transferred power of 1.41kW [79]. In recent years, high-power CPT systems over 3kW have been designed. Ref. [99] presents an excellent CPT system design with a power level of 3.75kW and an impressive high working frequency of 13.56MHz benefiting from a GaN-based full-bridge inverter. Unfortunately, it doesn't provide a solution for the rectification stage and the estimated dc-dc efficiency is only 93%. Meantime, the adopted SS CPT topology in [99] burdens the reactive power circulation between the primary and secondary sides [105]. Ref. [80] presented the highest capacitive power transfer efficiency of 95.7% on record. However, the bulky compensation inductors used in Ref [80] is almost six times the one used in the proposed design. Besides, the reactive power circulation exists, and the voltage stress V_{C1} is almost 1.5 times that of this work.

The implemented CPT system is developed from PP CPT compensations with double-sided SP IPT links, which achieves an impressive power transfer of 4.34kW, and the frequency of the implemented CPT system achieves the maximum record of 3MHz among all the SiC inverter-based CPT designs, as shown in Fig. 36 (a), validating the proposed multi-MHz and multi-kW inverter. Besides, this work reaches an excellent power and efficiency performance of 4.34kW and 94.1%, as shown in Fig.36 (b). Meantime, phase angle φ_{21} between port voltages V_1 and V_2 of the capacitive coupler achieves 90°, which maximizes the active power, achieves zero reactive power circulation, and minimizes the voltage stress. The proposed design achieves the highest power transfer capability of

Table IX. Comparison with state-of-art CPT designs.

Ref.	Year	Inverter	Topology	Input V_{dc}	P_{out}	η	f	C_M	k_C	φ_{21}*	V_1 and V_2
[76]	2015	SiC H-bridge	LCLC-LCLC	265V	2.4kW	90.8%	1MHz	18.35pF	0.155	70°	5.09kV, 5.09kV
[77]	2016	SiC H-bridge	CLLC-CLLC	400V	2.57kW	89.3%	1MHz	14pF	0.097	78°	5.31kV, 6.08kV
[78]	2017	SiC H-bridge	LCL-LCL	270V	1.97kW	91.6%	1MHz	9.91pF	0.081	80°	6.51kV, 6.51kV
[79]	2019	SiC H-bridge	LCLC-LCLC	250V	1.41kW	93.57%	1MHz	12.8pF	0.10	77°	3.99kV, 4.15kV
[99]	2020	GaN H-bridge	SS	430V	3.75kW	93%	13.56MHz	2.7pF	0.097	75°	5.9kV, 3.1kV
[80]	2021	SiC H-bridge	M_{SS}-SS-M_{SS}	500V	3.0kW	95.7%	1MHz	16.33pF	0.25	60°	6.01kV, 6.01kV
This work	2024	SiC H-bridge	M_{SP}-PP-M_{PS}	550V	4.34kW	94.1%	3MHz	23pF	0.40	**90°**	3.29kV, 4.05kV

φ_{21}: phase angle between port voltages V_1 and V_2 of capacitive coupler.



(a) power versus switching frequency (b) power and efficiency performance (c) power transfer capability per kV.

Fig. 36. Comparison with existing state-of-art CPT designs

0.83kW/kV among existing CPT systems, shown in Fig.36 (c).

VI. Conclusion

This paper investigated the challenges and explored the switching frequency limit of SiC full-bridge inverters, aiming at energizing multi-MHz and multi-kW CPT systems. Inverter drain-source current and voltage oscillations under zero-voltage switching-on are investigated, which are mainly attributed to the parasitic inductance of the inverter loop and the large turn-off current during ZVS operation. The inverter oscillation will induce oscillation in the gate driving signal via parasitic capacitance C_{gd}, $L_{S(\text{int})}$, which deteriorate as the frequency increases, endangering the reliability of gate driving signals and emerging as the limit on the achievement of a higher operating frequency. Mitigation methods are provided to guide the design of multi-MHz and multi-kW full-bridge inverters in terms of device selection, gate circuit design, ZVS turn-on realization, and PCB layout optimization.

Based on the presented design methodology, the implemented SiC full-bridge inverters achieve the highest power record of 6.59kW at 1MHz, and the highest switching frequency limit of 5MHz with 1.09kW when compared to existing SiC inverter designs, which further extends the working region of the SiC inverter and creates new power and frequency records. A ZVS switching limit of 3.5MHz of the SiC full-bridge inverter is pointed out. Based on the implemented SiC inverter, a 3MHz CPT prototype is energized, which achieves an impressive capacitive power transfer of 4.34kW with a dc-dc efficiency of 94.14%, validating the presented multi-MHz and multi-kW SiC inverter design. To achieve higher-power and higher-frequency power inversion, the future direction should focus on GaN switching device-based inverter with lower parasitic inductance, capacitance, and driving power, which contributes to improving the inverter oscillations and enables power conversion at higher frequency.

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