Real-time Demonstration of a Frequency-division Duplex 122Mbps Spread-Spectrum MIMO RFSoC Link

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***Abstract*—We design and implement a new multiple-input multiple-output (MIMO) frequency-division-duplex (FDD) spread-spectrum link and demonstrate real-time high-definition (HD) video streaming over a Radio Frequency System-on-a-Chip (RFSoC) software-radio testbed. To the best of our knowledge, this is the first-of-its-kind high-throughput low-latency full-duplex spread-spectrum link on RFSoC platforms which demonstrates an aggregated data throughput of 122 Mbps that supports real-time recording and playback of uncompressed full-HD video. The testbed comprises two Xilinx Zynq Ultrascale+ RFSoC ZCU111 evaluation kits with a custom-built application layer. A host-based graphical user interface (GUI) demonstrates live performance of the proposed 4x4 MIMO wireless link in terms of error vector magnitudepre-detection SINR and bit error rate (BER) and enables on-the-fly reconfiguration of link parameters such as spreading code sequence, transmit/receive antenna gains.**

I. Introduction

In recent years, the integration of general-purpose processors (GPPs) and field programmable gate arrays (FPGAs) within heterogeneous computing platforms (HCPs) has become prevalent. These platforms serve as the backend for software-defined radios (SDRs), facilitating the implementation of cognitive radio technologies. The combination of GPPs and FPGAs on a system-on-chip (SoC) offers an effective hardware-software (HW-SW) co-design solution, meeting the stringent power and timing constraints of advanced next-generation (NextG) wireless communication standards and protocols [1]. FPGAs contribute high computational throughput and deterministic latency, while GPPs adeptly handle sequential and dynamic processing [2]. The exploration of HW-SW co-design tradeoffs is discussed in [3], where 802.11a PHY-layer functionalities are executed in both the processing system (PS) and the programmable logic (PL) of a Zynq-based SoC. In the Openwifi project [4], a Xilinx Zynq SoC evaluation board (ZCU706) collaborates with the Analog Devices FMCOMMS2 radio board to implement a complete WiFi stack in Verilog. Simultaneously, a custom Linux kernel driver is developed for the PS to manage communications between the SoC and the radio board. The work presented in [5] focuses on implementation of the 5G NR PHY features on the FPGA of the USRP X300, utilizing National Instruments LabVIEW

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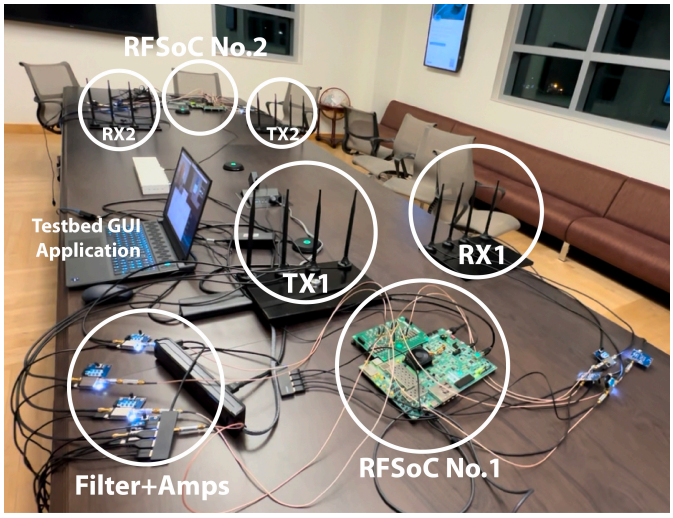

Fig. 1: Over-the-air (OTA) software-defined radio testbed to evaluate the 4x4 MIMO RFSoC FDD link.

to showcase a 4K live video streaming wireless link. In [6], a cognitive SDR with dynamic interference avoidance capability is demonstrated where the transceiver dynamically optimizes by joint space-time waveform shaping. Furthermore, multiple-input multiple-output (MIMO) communication architectures play a key role to unlocking new spectrum [7]. In addition to the vast benefits of MIMO technology including higher channel capacity and reliability, MIMO introduces degrees of freedom in both space and time domains.

Advancing progress on development of reconfigurable SDRs encounters two challenges. First, low-latency requirements of NextG communication standards and protocols could benefit from hardware-software co-design architectures that split signal processing workload between the processing system (PS) and programmable logic (PL) of an RFSoC platform. Second, the ever growing number of IoT devices competing for spectrum access could benefit from wireless system design that establish simultaneous transmit and receive communication links. However, the design of frequency division duplex (FDD) systems are not favorable in such a scenario because of two limitations. First, FDD requires distinct band utilization. Second, FDD systems require costly RF front-end hardware such as filters and amplifiers. However, an efficient solution

would be a combination of FDD and spectrally orthogonal waveforms which could be achieved through FDD spread-spectrum wireless systems.

In this demo (Fig. 1), we design and implement for the first time an autonomous high-throughput low-latency 4x4 MIMO RFSoC link which combines FDD and spectral orthogonality to demonstrate full-duplex communications. Using HW-SW co-design, signal processing functionalities are distributed between the PS and PL to achieve low-latency while a two-way uncompressed video recording and playback is demonstrated in real-time along with link performance evaluation metrics.

II. Testbed Design and Implementation

Our SDR platform is built on the Xilinx Zynq UltraScale+ RFSoC ZCU111 evaluation kit, which is based on the XCZU28DR-2FFVG1517E RFSoC Gen1 chip. The kit is paired with the XM500 RFMC balun transformer add-on card and commercial-off-the-shelf (COTS) amplifiers (Nooelec Vega Barebones - ultra low-noise variable gain amplifier), filters (BLK-89-S+ DC block and VBFZ-925-S+) and VERT900 monopole antennas that are omnidirectional in azimuth with an estimated gain of $3\ \mathrm{dBi}$ at $900\ \mathrm{MHz}$. The XM500 add-on card features 4 Digital-to-Analog-Converters (DACs)/4 Analog-to-Digital-Converters (ADCs) routed to high-frequency and low-frequency baluns and 4 DACs/4 ADCs routed to SMAs for use with external custom baluns and filters. The PL and the ARM PS give us the opportunity to examine hardware-software co-design tradeoffs. We use MathWorks Simulink and Xilinx Vivado to target the RFSoC PL and PS. We leverage the high level of parallelism in FPGAs to implement all the baseband processing of our MIMO transceiver as a non-feedback pipelined architecture on the PL fabric.

We perform over-the-air (OTA) experiments in an indoor laboratory environment. Each transceiver hosts 8 antenna for a 4x4 MIMO implementation. A 16-QAM spread-spectrum modulation is employed resulting to a bandwidth of 92.16 MHz. The FPGA runs at clock rate of 245.76 MHz. The full-duplex adjacent FDD links are designed using two adjacent frequencies of 840 MHz and 930 MHz. Each provide a transmit and receive channel of 61.44 Mbps for each direction and aggregated data rate of 122.88 Mbps. The SDRs ADCs and DACs are both set to 3.93216 GSPS with digital down converter (DDC), digital up converter (DUC) factors of 4, acquiring 4 samples per FPGA clock. We use an 4 samples-per-chip for pulse upsampling/downsampling. The spreading code length is set to 4, giving a sample interval of 4 nsec with a chip rate of 61.44 Mchips/sec.

Transmitter Chain: Each data frame begins with a preamble sequence which is Complementary Golay Sequence (CGS) and the frame detection is an FIR MF sliding correlator. For each frame, four MIMO training sequences are allocated for channel estimation per transmit and receive channels. An finite-state-machine (FSM) controller controls frame structure with logical signaling which appends payload, header, CRC, and training sequences. A MIMO arrangement block carries out channel estimation and creates parallel streams to each transmit antenna. A spreading block applies signal spreading using a complex signature vector. A packetization block appends preamble and adjusts signal energy. We use SRRC pulse shaping which is an FIR interpolation and handles upsampling. Application of a complex weight vector prepares the MIMO streams for transmission with a valid flag delivered to DAC channels.

Receiver Chain: The receiver first performs a chip matched filter using SRRC filter coefficients following timing acquisition and synchronization tasks. The core of the receiver chain is channel estimation and space-time matched filtering which has been carried out using the a priori known four MIMO training sequences implemented in the frame structure. Furthermore, the receiver takes care of decoding and evaluates experimental metrics such as EVM, SINR and BER. The decoded data bytes are flushed into a FIFO which is controlled by the PS.

Demonstration: We demonstrate two high-throughput low-latency links which are symmetric and work in a full-duplex manner in real-time on our designed 4x4 MIMO RFSoC SDR platforms. The testbed required two distinctive FPGA bitstream designs, each including Tx and Rx chains with two uncorrelated 128 bytes preamble. The link division is achieved through 90 MHz adjacent FDD in combination with orthogonal spread-spectrum signatures. Two HD webcams are directly connected to the two RFSoC SDR platforms via USB. The PS handles processing of generated video bytes, which are finally streamed through AXI4-Stream to the PL. This is achieved using TX and RX FIFOs of size 61440x32 bits shared between PL and PS. The developed application on the PS is capable of configuring resolution sizes including RAW JPEG format, HD, and Full-HD 1080p. To demonstrate the highest possible throughput of the two links, we intentionally use uncompressed video frames to generate large chunks of data. The PL design is high throughput with deterministic latency which takes care of all baseband processing and RF signalling. The decoded received bytes are streamed through the AXI4-Stream to the PS, where a TCP connection between the PS and a GigE-connected host computer is established. The host computer playbacks the video stream. An application graphical user interface (GUI) is also designed and controlled by the host which controls in real-time link parameters and demonstrates link performance evaluation parameters such as SINR, BER, received signal spectrum, and received constellations (Fig. 1).

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