Resilient Communications with Lightweight Signature Synchronization on MPSoC Radios

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2025 IEEE 22nd Consumer Communications & Networking Conference (CCNC) | 979-8-3315-0805-0/25/$31.00 ©2025 IEEE | DOI: 10.1109/CCNC54725.2025.10975913

***Abstract*—In highly dynamic and contested RF environments, communication systems must swiftly adapt to fluctuating spectral conditions while ensuring network quality of service (QoS). Maintaining link synchronization and spectral efficiency during waveform adaptation is particularly challenging due to the high mobility and autonomy of devices, coupled with the possibility of operating in GPS-denied environments. In this demo, we introduce a scalable, high-speed FPGA-based parallel decoding algorithm that leverages the HORNets signature adaptation protocol to address these challenges. Our solution preserves link synchronization within a multi-node network and enables efficient, lightweight waveform adaptation without reliance on GPS. The algorithm's resilience and effectiveness are demonstrated using a three-node cluster configuration, all subjected to non-colored or colored intentional interference.**

***Index Terms*—HORNets, Field Programmable Gate Array (FPGA), Quality of Service (QoS), waveform adaptation.**

I. Introduction

Communication systems operating in dynamic and contested RF environments must swiftly adapt to evolving spectral conditions while mitigating signal impairments such as path loss, multipath effects, Doppler shifts, and interference. The high mobility and autonomy of network nodes, combined with the potential for GPS-denied operations, further complicate the task of sustaining link synchronization and optimizing spectral efficiency [1], [2]. In [3] [4], HORNets was developed to facilitate real-time waveform optimization in contested, interference-limited environments. HORNets dynamically adjusts the spreading code based on the sensed Signal-to-Interference-plus-Noise Ratio (SINR) at the receiver, evaluating candidate waveforms and selecting the optimal code that maximizes SINR while minimizing interference. However, the current version of HORNets faces two key limitations in signature and carrier frequency synchronization.

First, the highly dynamic environment and electronic noise can cause drift in the local oscillators (LO) of both the transmitter and receiver, leading to a dynamic carrier frequency offset (CFO). Traditionally, this drift is corrected using a common reference clock or GPS-disciplined oscillators (GPSDOs), but not all devices support such external references. To overcome this, we design and evaluate a GPS-free synchronization technique that estimates and compensates for CFO at the receiver, enabling operation without GPSDOs in GPS-denied environments.

Second, adapting the spreading code can disrupt link synchronization in multi-hop networks. To address this, we design and implement a parallel decoding technique to ensure seamless synchronization during code adaptation. By employing multiple parallel despreading chains with zero cross-correlation of antipodal codes, our algorithm enables efficient adaptation with minimal signaling overhead. We implement this solution on FPGA fabric to achieve low-power, real-time processing crucial for resource-constrained applications.

This work was supported in part by the National Science Foundation (NSF) under Grant SWIFT-2229563, and the U.S. Air Force Research Laboratory under Contracts FA8750-21-F-1012 and FA8750-20-C-1021.
Distribution A. Approved for public release: Distribution Unlimited: AFRL-2024-6364 on 14 Nov 2024.
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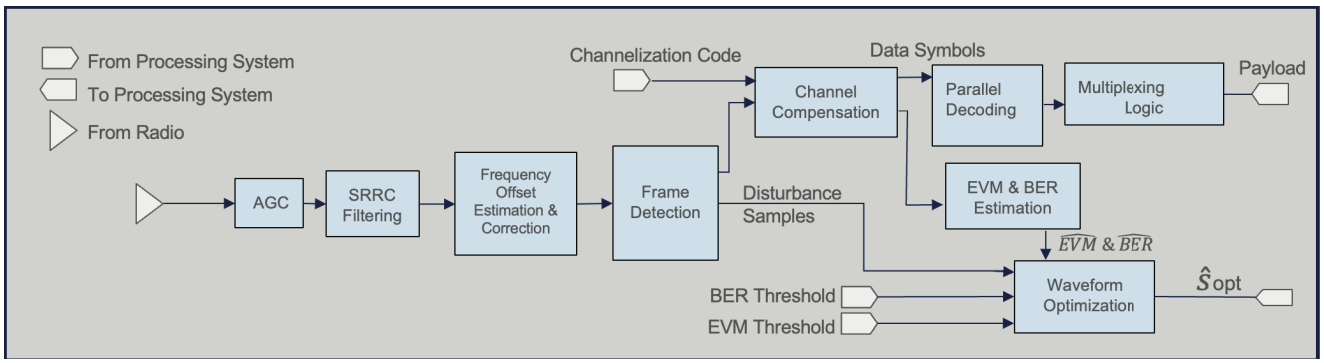

Fig. 1: FPGA implementation of the receiver chain for lightweight waveform adaptation.

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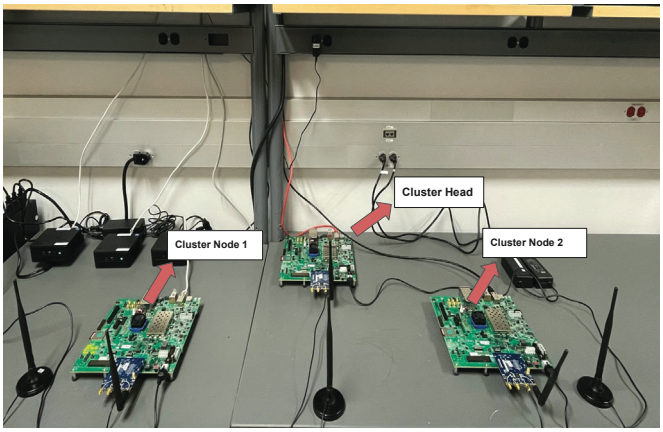

Fig. 2: Testbed Setup

In this demo, we develop two novel algorithms for code adaptation and frequency synchronization and integrate them into the original HORNets protocol. We demonstrate that these algorithms can enable GPS-independent synchronization and parallel decoding, ensuring seamless waveform adaptation in highly dynamic RF environments.

II. Framework Design and Implementation

Figure 1 shows the FPGA-based implementation of the receiver chain logic of the upgraded HORNets waveform adaptation protocol. The frequency offset estimation block processes the output from the Square-Root-Raised-Cosine (SRRC) filter, calculates the carrier frequency drift, and compensates for it using the synchronization technique described below. The parallel decoding block consists of 16 matched filtering and despreading chains. A state machine in the multiplexing block manages control signals and selects the correct despreading chain based on the code identifier embedded in the payload.

CFO Estimation. The CFO estimation is performed using the Correlation and Accumulation algorithm [5], which detects periodicity in the received signal introduced by the training sequence in the PHY header. The algorithm computes the autocorrelation and variance of the received signal, comparing these values against a user-defined threshold to identify the start of the sequence. Once detected, the CFO estimate is calculated and scaled to determine the phase increment for a numerically controlled oscillator (NCO). The final CFO compensation is achieved by multiplying the received signal with the output of the NCO.

Parallel Decoding. The parallel decoding module equips each receiver with multiple despreading chains, enabling it to handle any waveform the transmitter may adapt to in real time. This is facilitated by pre-programming the network with selected antipodal spreading codes that have zero cross-correlation, significantly enhancing responsiveness and streamlining the code adaptation process. Each transmitted packet includes a spreading code identifier in its header, which dictates the specific code used. Upon reception, all parallel decoders in the receiver chain simultaneously despread the packet, selecting the decoder that matches the spreading code identifier in the packet header for further processing. The implementation of this parallel decoding algorithm on FPGA fabric ensures no computational overhead during the entire adaptation process and maintains constant time complexity as the network scales.

III. Demonstration

We will demonstrate the effectiveness and resilience of our lightweight code adaptation protocol in different interference-limited scenarios. As shown in Fig. 2, we will set up an experimental testbed consisting of a cluster network with one cluster Head (CH) and two Cluster Nodes (CNs). All baseband signal processing for the physical layer is implemented and runs on the FPGA fabric of Zynq Ultrascale ZCU102 MPSoC Evaluation Kits [6] interfaced with Analog Devices AD-FMCOMMS3-EBZ Radio front ends. MAC layer protocols, including waveform adaptation and parallel decoding, are also implemented on the FPGA for efficient edge computing. Live video streams captured by a webcam on a host computer (Intel NUC) are first transmitted via the ARM processor of the MPSoCs over an Ethernet connection using UDP, and then piped to the FPGA fabric using the AXI Stream Protocol. An Ettus Research USRP B210 [7] software-defined radio is programmed to act as a hostile jammer.

Demo 1: Carrier Frequency Synchronization. To demonstrate GPS-free synchronization, the CH captures a live video stream and broadcasts it to both CNs. As shown in Fig. 1, on the receiver side of the FPGA fabric, the frequency offset estimation and correction block can be programmatically enabled or disabled in real time. We will demonstrate the resulting phase shift in the receiver's constellation when the CFO compensation block is turned on and off.

Demo 2: Signature Synchronization. In this demo, we will demonstrate the effectiveness of the lightweight signature synchronization in both jammed and interference-free scenarios. Under normal conditions without interference, the CNs successfully receive and decode the video stream. However, when jamming is introduced, the resulting drop in SINR at the CNs leads to significant video degradation or loss. We will showcase how the CNs, in coordination with the CH, leverage the lightweight adaptation algorithm to mitigate interference and recover the link with enhanced SINR and video quality.

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