

# Low-Power Adiabatic/MTJ LiM-Based XNOR/XOR Synapse and Neuron for Binarized Neural Networks

Milad Tanavardi Nasab and Himanshu Thapliyal

**Abstract**— Using binarized neural network (BNN) as an alternative to the conventional convolutional neural network is a promising candidate to answer the demand of using human brain-inspired in applications with limited hardware and power resources, such as biomedical devices, IoT edge sensors, and other battery-operated devices. Using nonvolatile memory elements like MTJ devices in a LiM-based architecture can eliminate the need to access and use external memory which can significantly reduce the power consumption and area overhead. In addition, by using adiabatic-based designs, a significant part of the consumed power can be recovered to the power source which leads to a huge reduction in power consumption which is vital in applications with limited power and hardware resources. In this paper by using nonvolatile MTJ devices in a LiM architecture and using adiabatic-based circuits, an XNOR/XOR synapse and neuron is proposed. The proposed design offers 97% improvement in comparison with its state-of-the-art counterparts in case of power consumption. Also, it achieves at least 7% lower area compared to other counterparts which makes the proposed design a promising candidate for hardware implementation of BNNs.

## I. INTRODUCTION

Hardware-implemented neural networks have higher performance in comparison with software implementations [1]. However, hardware-implemented neural networks have significant area and power overhead. This makes it very difficult to use these hardware-implemented neural networks in battery-operated devices such as mobile and IoT edge devices [2]. Therefore, an investigation into energy-efficient designs of hardware-implemented networks is needed to satisfy the power and energy budget.

Further, efficient design in every abstraction level of design is needed due to (i) the huge number of weights in the structure of neural networks, (ii) the need to consistently access these stored weights, and (iii) the huge number of required operations. Nonvolatile memory devices, like magnetic tunnel junctions (MTJs) [3] can be used to implement novel logic-in-memory (LiM) [4-7] to reduce the power and area overhead of hardware-implemented neural networks. Also using hardware-aware approaches and algorithms in the definition of networks (using binarized neural networks instead of convolutional neural networks)[1], and exploiting energy-efficient approaches like using adiabatic-based circuits [2] will reduce power and area overhead of hardware-implemented neural networks. Accordingly, it can be beneficial for efficient hardware

implementation of human-brain-inspired networks in battery-operated devices.

Accessing the numerous stored weights of neural networks can be the bottleneck of every design [3]. In the existing literature, by using nonvolatile memory elements like MTJ in the structure of the LiM architecture, promising candidates have been designed, but the dynamic power consumption is still relatively high in these designs. The adiabatic-based circuits can reduce dynamic power by recycling the power to the voltage source. In this paper, an adiabatic-based nonvolatile LiM XNOR/XOR synapse and neuron has been proposed to address the high dynamic power consumption issue of the hardware-implemented binarized neural network. This novel approach can be a new direction in the hardware implementation of neural networks. The main contribution of this paper can be listed as:

- A low-power hardware efficient LiM adiabatic/spintronic-based XNOR/XOR synapse and neuron.
- Investigating the power and area of a binarized neural network, utilized by the proposed neuron and comparing these factors with other state-of-the-art counterparts.
- Investigating the use of adiabatic-based circuits in hardware implementation of neural networks.

The rest of this paper is organized as: A brief review of the fundamental backgrounds of the study is presented in Section II. In Section III other state-of-the-art counterparts are reviewed followed by the description of the proposed design in detail in Section IV. In Section V the result of the simulation of the proposed design is investigated and its functionality has been studied. Furthermore, the result of the hardware implementation of the BNN using the proposed design and other counterparts is also investigated in this Section. Finally, Section VI concludes the paper.

## II. BACKGROUNDS

### A. Magnetic Tunnel Junction

MTJ is one of the most important and used devices in magnetic-based designs. It is a magnetic memory element that benefits from nonvolatility which has two ferromagnetic layers, separated by an oxide layer. The magnetic direction of these ferromagnetic layers specifies the mode of the MTJ. If the magnetic direction of these two layers is the same, the MTJ is in parallel mode and the electrical resistance of the device is relatively low ( $R_p$ ). If the magnetic direction of

these layers is not the same, the device is in anti-parallel mode the electrical resistance of the device is relatively high ( $R_{ap}$ ). Accordingly, this device can store two values which can be considered as logical '1' and '0'. Due to the fact that the magnetic direction of one of these two layers can be changed (free layer) and the magnetic direction of the other layer is always the same (fixed layer), the write operation is changing the magnetic direction of the free layer.

One of the most important parameters of the MTJs is tunnel magnetoresistance which is calculated using Eq. 1.

$$TMR = \frac{R_{ap} - R_p}{R_p} \quad (1)$$

TMR ratios of 604% and 249% are reported for in-plane MTJ and perpendicular MTJ, respectively [4].

Another important criterion of MTJs is the retention time which is of double importance in mobile devices. The retention time can be calculated by Eq. 2.

$$\tau = \tau_0 \exp\left(\frac{H_k M_s A_r t}{2k_B T}\right) \quad (2)$$

in which  $\tau_0$  is equal to 1 nanosecond,  $H_k$  is uni-axial anisotropy,  $M_s$  is saturation magnetization,  $A_r$  is the area of the MTJ, and  $k_B$  is Boltzmann constant.  $\frac{H_k M_s A_r t}{2k_B T}$  is called thermal stability and is shown by  $\Delta$  and it must be more than 75 for a storage class memory [5].

The nonvolatility of MTJ makes them a promising candidate for hardware implementation of BNN, especially in battery-operated and mobile devices. In addition, the compatibility of the manufacturing process of this device with CMOS technology, high density, intrinsic immunity to soft errors, and low power consumption, attract much attention in recent research for LiM-based architecture.

### B. Adiabatic Logic

Adiabatic logic reduces the dynamic power by using power clocks and recycling the stored charges to the power supply by using adiabatic switching. Ideal adiabatic switching is performed using a constant current source [6]. In this case, the dissipated energy is calculated by Eq. 3.

$$E_{diss} = \frac{RC}{T} CV_{dd}^2 \quad (3)$$

in which  $T$  is the time in which the load capacitance is charged/discharged,  $R$  is the electrical resistance of the charging/discharging path,  $C$  is the load Capacitance and  $V_{dd}$  is the full swing of the power clock. The dissipated energy in adiabatic logic depends on the  $T$  and it is less than the dissipated energy in conventional CMOS logic if  $T$  is much bigger than the time constant ( $RC$ ).

### C. Binarized Neural Network

The binarized neural network is a promising candidate to overcome the challenges of the efficient hardware implementation of the convolutional neural network (CNN) in power/hardware-limited resources. In binarized neural networks, floating-point operations are replaced by binary operations. In the case of binarizing weights, the convolution, which consists of floating-point multiplications and additions, is replaced by a signed add operation. In the case of binarizing both weights and inputs, the convolution operation is replaced by a binary XNOR-bitcounting operation. The second approach is used in XNOR-network

[1]. In this network, a filter  $W$  can be estimated by a binary filter  $B$  and a scaling factor  $\alpha$ . The filter  $B$  and the scaling factor  $\alpha$  can be calculated using Eq. 5. and Eq. 6.

$$W = B \times \alpha \quad (4)$$

$$B = \text{sign}\{W\} \quad (5)$$

$$\alpha = \frac{1}{k} \|W\|_{n_m} \quad (6)$$

In Eq. 6.  $k$  is the total number of weights in the  $m^{\text{th}}$  filter in the  $n^{\text{th}}$  layer. For binarizing the inputs, a similar approach is used in which the input matrix of  $X$  is estimated by a binary matrix of  $H$  and a scaling factor of  $\beta$ . The matrix  $H$  and scaling factor  $\beta$  can be calculated using Eq. 8. and Eq. 9. respectively.

$$X^T = H^T \times \beta \quad (7)$$

$$H = \text{sign}\{X\} \quad (8)$$

$$\beta = \frac{1}{k} \|X\|_{n_m} \quad (9)$$

Consequently, a convolution operation can be estimated by Eq. 10.

$$X * W \cong (\text{sign}\{X\} \odot \text{sign}\{W\}) \odot \alpha \beta \quad (10)$$

$$= (H \odot B) \odot \alpha \beta$$

In Eq. 10.,  $\odot$  is XNOR-bitcounting operation and  $\odot$  is element-wise multiplication.

By using the XNOR network instead of conventional CNN, the required hardware and power for hardware implementation is reduced which is of double importance in mobile and battery-operated devices. In addition, the complexity of the hardware will be decreased, too.

## III. PREVIOUS WORK

In the literature, much research has been conducted and several designs have been proposed [7-14]. The following state-of-the-art designs are considered for comparison with the proposed design.

In [13] an XNOR neuron for implementing BNN has been proposed. In this design, by using two MTJ devices to store each binary weight, a sense amplifier, and a current source the neuron has been designed. According to the use of a current source, the power consumption of this design is high which is not desirable in battery-operated devices.

In [10] an XNOR/XOR gate for implementing BNNs is proposed. This design is based on the voltage division between two MTJs which are used to store one-bit weight. Due to the structure of this design, it has a high power and energy consumption.

Another design for XNOR/XOR neurons is proposed in [9]. This design benefits lower energy power consumption in comparison with the other two counterparts, but due to the daily-increasing need for using human brain-inspired technologies in devices with limited power resources, the need for more efficient design is always needed.

In [14] an XNOR/XOR neuron based on two 1-transistor 1-RRAM has been proposed. Due to using a constant current source in the structure of the design as a reference, the power consumption of this design is relatively high which undesirable in battery-operated devices.

Although using novel architecture like LiM alongside nonvolatile memory devices, like MTJ, can reduce the power and energy consumption, using low-power approaches like using adiabatic circuits alongside this architecture and devices can significantly reduce the power and energy consumption which is desirable in power-limited applications.

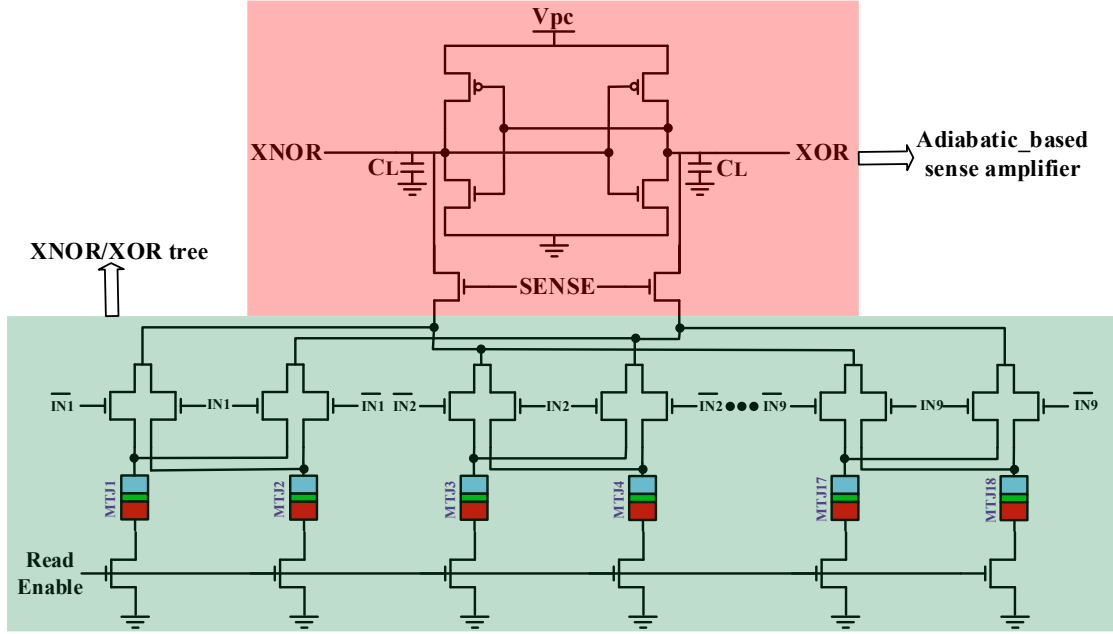


Fig. 1. Proposed MTJ-based Adiabatic XNOR/XOR synapse and neuron

#### IV. PROPOSED DESIGN

In this paper, an energy-efficient nonvolatile adiabatic XNOR/XOR neuron and synapses based on LiM architecture and MTJ device is proposed. The proposed design is shown in Fig. 1. Due to the structure of this design, its functionality is independent of the type of MTJ used to implement the circuit. Also, different writing methods can be used to write on MTJs. Furthermore, it is noteworthy that in hardware implementation of the BNNs, due to the nonvolatility of MTJ, the weights need to be written only one time which makes the MTJs a promising candidate for implementing BNNs.

##### A. Retention time and MTJ sizing

An important parameter which is needed to be handled carefully in designing LiM architecture-based circuits is the retention time. Since in the hardware implementation of BNNs, the weights are needed to be written one time, the absence of external memory in the design (due to the hardware resources limitation in IoT devices, mobile devices, and other battery-operated devices), and also the lack of access to the device in many applications, the retention time of MTJ must be high and in storage class memory. Consequently, the size of MTJs must be designed carefully. By increasing the size of MTJs, their retention time will increase significantly and their electrical resistance will reduce. Consequently, a bigger size of MTJ leads to higher retention time. But, the power and energy consumption of the proposed design is proportional to the resistance of MTJs and lower resistance will lead to higher power and energy consumption. Another parameter that affects the retention time is the thickness of the barrier layer of the MTJs. Higher thickness of the barrier layer leads to higher retention time and increases the resistance of the MTJ exponentially, but also increases the needed voltage for a write operation on the MTJ. Accordingly, the selected values

for the size of MTJs and their barrier layer thickness must be in a way that they provide a reasonable retention time, and power consumption, and also be in a way that write operation can be done using the circuit's VDD.

##### B. Functionality

The proposed energy-efficient nonvolatile adiabatic XNOR/XOR neuron and synapses based on LiM architecture and MTJ device is shown in Fig. 1. Due to the function of the proposed design that acts as a neuron, there is no need to use auxiliary circuits to perform activation function which leads to more efficiency in case of area and power overhead. Also, due to the use of MTJs and their nonvolatility feature, the need to store the weights in an external memory and restore them at the first of each use will be eliminated which leads to lower area and power overhead in the system level. Furthermore, using LiM architecture leads to the elimination of the need to access external memory which in turn reduce the power and area overhead at the system level. In addition, by using an adiabatic-based sense amplifier (SA) in the structure of the proposed design, the energy and power consumption will be significantly reduced. Also, the proposed design is scalable and can be used to implement filters with different sizes.

Each weight is stored on two MTJs with different states. To store '1' ('-1'), MTJ1 must be in antiparallel (parallel) mode and MTJ2 must be in parallel (antiparallel) mode. This difference between the state of the MTJs will lead to different path resistance of node XNOR and XOR to the ground. Consequently, during the read operation, the outputs will be determined based on the difference between the path resistances.

In the adiabatic circuits, a signal named power-clock signal  $V_{pc}$  is used as a clock signal and voltage supplier. This signal can be trapezoidal or sinusoidal. Generating a sinusoidal signal has less complexity than generating a trapezoidal signal. Accordingly, a sinusoidal power-clock

signal has been used in this paper. Based on this signal the operation of the proposed design can be determined. From the aspect of the power-clock signal, the read operation has two phases, the evaluation and recovery phase. The power-clock signal rises from 0 to VDD in the evaluation phase and the recovery phase is operated while the power-clock signal falls from VDD to 0.

In the evaluation phase, the signal Read Enable must be '1', so the output can have an activated path to the ground. The signal SENSE rises from '0' to '1' for a small period of time, so the residual charge of the output of the previous input can be discharged to the ground and the adiabatic SA can sense the resistance of paths and produce the proper output. The signal SENSE must be activated when the power-clock signal is zero, so the discharge operation can be done before sensing (since the power-clock signal is '0', the SA is not activated). After the discharging operation, while the signal SENSE and Read Enable are both '1', the power-clock signal starts to rise and the voltage of XNOR and XOR will start to rise, but since they have different paths to the ground with different resistances, they will have different voltage. In the next step, the signal SENSE fall from '1' to '0'. Consequently, the SA will sense the voltage of the node XNOR and XOR both and produce the proper output based on the difference in voltage between XNOR and XOR nodes. Consequently, one of the nodes XNOR or XOR will be discharged to the ground and the other one will rise, following the power-clock signal. When the power clock signal reaches the VDD, the evaluation phase is over.

In the recovery phase, the power-clock signal will fall gradually from VDD to the ground. By failing the power-clock signal, one of the nodes XNOR or XOR which has followed the power-clock signal in the evaluation phase, will have higher voltage in comparison with the voltage of the power-clock signal. Consequently, a current will flow to the power-clock node from this node and the charges in that node will be recovered to the power-clock node. It is noteworthy that this node will be discharged to the power-clock node until its voltage reaches the threshold voltage of the PMOS transistor.

## V. SIMULATION

In this section, various aspects of the performance of the proposed design and its counterparts are simulated, evaluated, and compared. To have a better comparison, the results of implementing a whole BNN have been studied to reach a better insight into the performance of the proposed design and its counterparts in the hardware implementation of BNN.

### A. Functional Simulation

The proposed design and its counterparts have been simulated using HSPICE. For the simulations of the proposed design and its counterpart predictive technology model for 32nm [15] and the STT-MTJ model [16, 17] have been used. The counterparts have been redesigned and optimized to have a fairer comparison. The critical parameters of the MTJ and transistors are shown in Table I. The size of MTJ has been chosen in a way that the retention time of the MTJs can be classified in the storage memory

class (Retention time=1.36e15) and simultaneously has relatively high resistance without making the write operation have an additional voltage source.

The results of the functionality simulation of the proposed design with 3 weights are illustrated in Fig. 2. which is consist of power-clock signal, Read Enable signal, SENSE signal, inputs and corresponding weights, and XNOR and XOR as outputs. It is noteworthy that the proposed neuron is scalable and for simplicity of validating the functionality of the proposed design, a neuron with 3 weights is shown in Fig. 2. As shown in Fig. 2. during 0 ns to 40 ns (160 ns to 200 ns) the circuit is in the evaluation phase of read mode. During this period, weight 1, weight 2, and weight 3 are '-1', '1', and '-1' respectively, and input 1, input 2, and input 3 are '0' ('1') and the Read\_Enable signal is '1'. While the SENSE signal is '1', both output XNOR and XOR start to rise and follow V<sub>pc</sub>, but when the SENSE signal falls, the XOR (XNOR) output falls and XNOR (XOR) output follows the V<sub>pc</sub> signal toward VDD. So, the output of a 3-input XNOR/XOR neuron with a hard limit activation function is produced. Next, from 40 ns to 80 ns (200ns to 240 ns) the circuit is in the recovery phase of the read operation. During the time that the Read\_Enable signal is '0', the circuit is in Idle mode. In these periods, writing operations can be done. It is noteworthy that the weights are written on the MTJs only one time after the training process.

Table II shows the consumed energy in each cycle (E/cycle) and the average power consumption of the proposed design with 1, 3, and 9 weights. Since the power and energy consumption depends on the duty cycle of the SENSE signal, the results in Table II are obtained by applying a SENSE signal with a duty cycle of 25% (the SENSE signal is '1' for 20 ns)

TABLE I. CRITICAL PARAMETERS OF THE SIMULATIONS

| Description                            | Value          |
|----------------------------------------|----------------|
| Transistors                            |                |
| NMOS gate length                       | 32 nm          |
| PMOS gate length                       | 32 nm          |
| NMOS gate width                        | 48 nm          |
| PMOS gate width                        | 96 nm          |
| MTJ                                    |                |
| Oxide barrier thickness                | 0.9 nm         |
| TMR under zero voltage bias            | 300%           |
| Minimum TMR under operational voltage  | 270%           |
| Free layer thickness                   | 2 nm           |
| MTJ surface                            | 60 nm ×60 nm   |
| Resistance area product (RAP)          | 10             |
| MTJ resistance under zero bias voltage | 4.1 KΩ-16.2 KΩ |
| Simulation frequency                   | 12.5 MHz       |

TABLE II. ENERGY AND POWER CONSUMPTION OF THE PROPOSED ADIABATIC-BASED NEURON

| Number of weights and input in neuron       | 1 weight and input | 3 weights and inputs | 9 weights and inputs |
|---------------------------------------------|--------------------|----------------------|----------------------|
| Average power consumption (nW)              | 5.2                | 6.5                  | 7.1                  |
| Energy consumption in each cycle (nJ/cycle) | 416                | 520                  | 568                  |

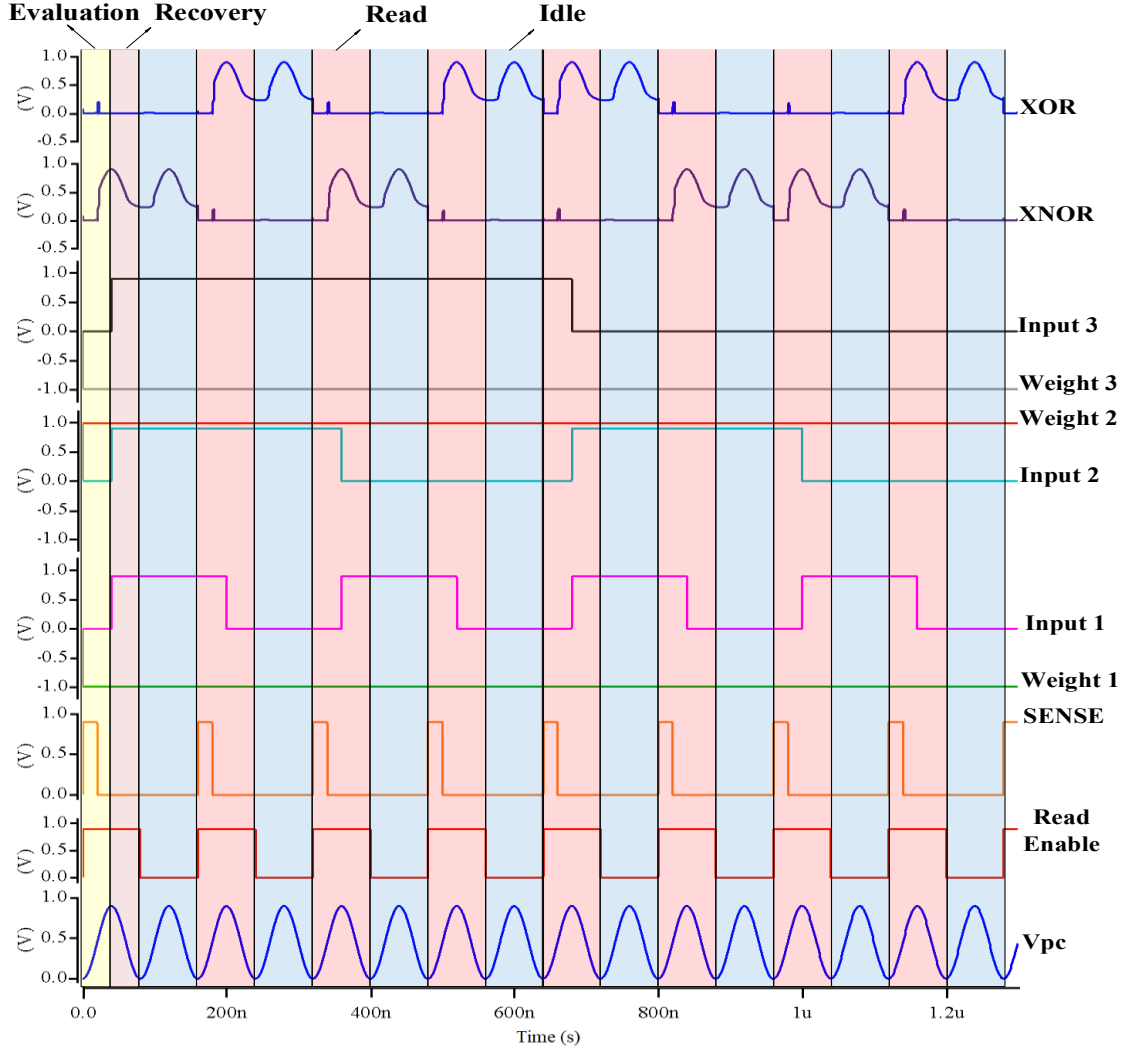


Fig. 2. Simulation result of the proposed neuron and synapse

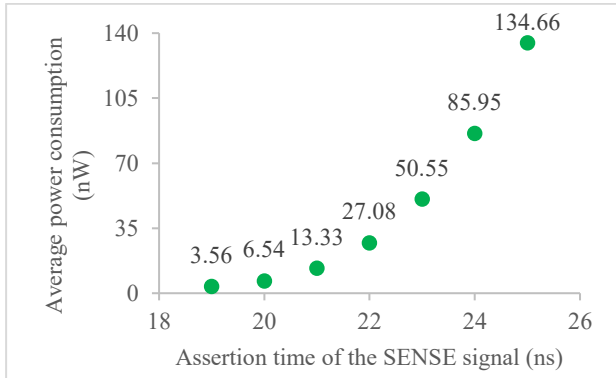


Fig. 3. Power consumption of the proposed neuron and synapse with 3 weights and different activation duration of the SENSE signal

In order to study the effect of the duty cycle of the SENSE signal, simulations with different duty cycles for the SENSE signal have been carried out. In this simulation, a neuron with three weights has been simulated. The results are shown in Fig. 3.

As it is shown in Fig. 3, the power consumption of the proposed design is dependent on the assertion time of the

SENSE signal. The minimum assertion time of the SENSE signal by which the neuron can produce the output correctly is 19 ns (with the power-clock signal frequency of 12.5MHz). By considering 5% and 10% error for the timing of the SENSE signal, the minimum time for the SENSE signal to be asserted and still the neuron works properly is 20 ns and 22 ns, respectively. The results in Table II are based on a simulation in which the assertion time for the SENSE signal is 20 ns.

### B. BNN Implementation

To have a better comparison with other counterparts and better insight into the implementation of BNN, utilized by the proposed design in this paper and in other counterparts, the power consumption of the whole network has been studied. The architecture of the network used for this study is  $2 \times (64C3)_{\text{MP2-2}} 2 \times (128C3)_{\text{MP2-2}} 2 \times (256)_{\text{MP2-2\_AP4-2\_256FC\_Softmax}}$ . In this notation 64C3 stands for a convolutional layer with a kernel size of  $3 \times 3$  and feature size of 64, MP2-2 stands for a max-pooling layer with a kernel size of  $2 \times 2$  and stride of 2, AP4-2 stands for an average pooling layer with a kernel size of  $4 \times 4$  and stride of 2, and 256FC stands for a fully connected layer with 256 neurons. The number of required transistors and power

consumption of the implemented network are shown in Table III. It is noteworthy that the assertion time of the SENSE signal is 22 ns for this simulation.

TABLE III. RESULTS OF THE HARDWARE IMPLEMENTATION OF BNN

| Design                   | [13]    | [10]    | [9]   | [14]    | Proposed |
|--------------------------|---------|---------|-------|---------|----------|
| Average power ( $\mu$ W) | 41932.8 | 24837.1 | 985.6 | 37094.4 | 27.7     |
| Transistor number        | 50176   | 64512   | 49280 | 49280   | 45696    |

As results in Table III shows, the proposed design in this paper offers at least 97% and 7% improvement in comparison with its state-of-the-art counterparts in the case of power consumption and transistor number, respectively. According to the results of Table III, using adiabatic-based circuits can reduce the power consumption of the hardware-implemented BNN significantly which is vital in battery-operated devices such as biomedical devices, IoT edge sensors, and other mobile devices. Also, in terms of area and transistors number, the proposed design in this paper provides more efficiency which leads to a lower price of hardware implementation of BNNs.

## VI. CONCLUSION

In this paper, a scalable nonvolatile spintronic LiM adiabatic-based XNOR/XOR synapse and neuron based on MTJ devices has been proposed. Using nonvolatile MTJs in a LiM architecture in an adiabatic-based architecture, in addition to eliminating the need to external memory and accessing this memory, also reduce the power consumption significantly. Due to the increasing demand for hardware implementation of human brain-inspired technology in battery-operated devices, such as biomedical devices and IoT edge sensors, the proposed power and area-efficient design is a promising candidate to answer this demand. The result of the hardware implementation of the implemented BNN in this paper utilized by the proposed design in this paper offers 97% improvement compared to its state-of-the-art counterparts in case of power consumption. Also, the proposed designs occupy at least 7% lower area compared with other counterparts, which makes the proposed design a promising candidate for the application of hardware implementation of the BNN.

In the future works, different aspects of scalability of the proposed design, regarding functionality and reliability will be investigated.

## REFERENCES

- [1] M. Rastegari, V. Ordonez, J. Redmon, and A. Farhadi, "XNOR-Net: ImageNet Classification Using Binary Convolutional Neural Networks," Cham, 2016, pp. 525-542: Springer International Publishing.
- [2] W. Yang, A. Degada, and H. Thapliyal, "Adiabatic Logic-based STT-MRAM Design for IoT," presented at the 2022 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2022.
- [3] M. BahmanAbadi, A. Amirany, K. Jafari, and M. H. Moaiyeri, "Efficient and Highly Reliable Spintronic Non-volatile Quaternary Memory Based on Carbon Nanotube FETs and Multi-TMR MTJs," *ECS Journal of Solid State Science and Technology*, vol. 11, no. 6, 2022.

- [4] M. Wang *et al.*, "Current-induced magnetization switching in atom-thick tungsten engineered perpendicular magnetic tunnel junctions with large tunnel magnetoresistance," *Nat Commun*, vol. 9, no. 1, p. 671, Feb 14 2018.
- [5] A. Nigam, C. W. Smullen, V. Mohan, E. Chen, S. Gurumurthi, and M. R. Stan, "Delivering on the promise of universal memory for spin-transfer torque RAM (STT-RAM)," in *IEEE/ACM International Symposium on Low Power Electronics and Design*, 2011, pp. 121-126: IEEE.
- [6] S. Dinesh Kumar, H. Thapliyal, A. Mohammad, and K. S. Perumalla, "Design exploration of a Symmetric Pass Gate Adiabatic Logic for energy-efficient and secure hardware," *Integration*, vol. 58, pp. 369-377, 2017.
- [7] A. Samiee, P. Borulkar, R. F. DeMara, P. Zhao, and Y. Bai, "Low-Energy Acceleration of Binarized Convolutional Neural Networks using a Spin Hall Effect based Logic-in-Memory Architecture," *IEEE Transactions on Emerging Topics in Computing*, pp. 1-1, 2019.
- [8] M. Natsui, T. Chiba, and T. Hanyu, "Design of an energy-efficient XNOR gate based on MTJ-based nonvolatile logic-in-memory architecture for binary neural network hardware," *Japanese Journal of Applied Physics*, vol. 58, no. SB, 2019.
- [9] M. T. Nasab, A. Amirany, M. H. Moaiyeri, and K. Jafari, "High Performance and Low Power Spintronic Binarized Neural Network Hardware Accelerator," presented at the 2022 30th International Conference on Electrical Engineering (ICEE), 2022.
- [10] M. T. Nasab, A. Amirany, M. H. Moaiyeri, and K. Jafari, "High-Performance and Robust Spintronic/CNTFET-Based Binarized Neural Network Hardware Accelerator," *IEEE Transactions on Emerging Topics in Computing*, pp. 1-6, 2022.
- [11] M. T. Nasab, A. Amirany, M. H. Moaiyeri, and K. Jafari, "Hybrid MTJ/CNTFET-Based Binary Synapse and Neuron for Process-in-Memory Architecture," *IEEE Magnetics Letters*, vol. 14, pp. 1-5, 2023.
- [12] B. J. Obradovic, R. M. Hatcher, J. A. Kittl, and T. Rakshit, "FE-FET-based XNOR cell usable in neuromorphic computing," ed: Google Patents, 2019.
- [13] A. Musello, E. Garzón, M. Lanuzza, L. M. Prócel, and R. Taconi, "XNOR-Bitcount Operation Exploiting Computing-In-Memory With STT-MRAMs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 3, pp. 1259-1263, 2023.
- [14] X. Sun, S. Yin, X. Peng, R. Liu, J.-s. Seo, and S. Yu, "XNOR-RRAM: A scalable and parallel resistive synaptic architecture for binary neural networks," in *2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2018, pp. 1423-1428: IEEE.
- [15] N. Group, "Predictive Technology Model (PTM)(Arizona State University, 2008)," ed.
- [16] Y. Wang, Y. Zhang, E. Y. Deng, J. O. Klein, L. A. B. Naviner, and W. S. Zhao, "Compact model of magnetic tunnel junction with stochastic spin transfer torque switching for reliability analyses," *Microelectronics Reliability*, vol. 54, no. 9-10, pp. 1774-1778, 2014.
- [17] Y. Zhang *et al.*, "Compact Modeling of Perpendicular-Anisotropy CoFeB/MgO Magnetic Tunnel Junctions," *IEEE Transactions on Electron Devices*, vol. 59, no. 3, pp. 819-826, 2012.