A 16–32 GHz RF Photonic Front-End With 22 nm CMOS Driver and Silicon Travelling-Wave Mach-Zehnder Modulator

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***Abstract*—Analog photonic links that leverage silicon photonic components offer potential advantages for building future wireless communication systems. A wideband electrical front-end circuit and a high speed electro-optic modulator are essential parts of the photonic receiver links. This paper presents a co-integrated 16–32 GHz front-end link with an electrical driver in a 22 nm CMOS FD-SOI process and a silicon photonic travelling-wave Mach-Zehnder modulator (TW-MZM) in a 220 nm SOI process. A Magnetically-coupled resonator technique is adopted to realize wideband impedance matching network and a stack-FET structure is utilized for higher supply voltage operation, providing 13 dBm output power from the driver. In the TW-MZM, a slow-wave transmission line electrode is implemented to improve its bandwidth by impedance and velocity matching. The CMOS and silicon photonic chips are co-designed considering the bond-wire and input impedance of TW-MZM. The calculated spurious free dynamic range (SFDR) of the link with a grating coupler is 89 $dB * Hz^{(2/3)}$ and it is possible to achieve 105 $dB * Hz^{(2/3)}$ using a lower-loss edge coupler.**

***Index Terms*—CMOS, driver, low-noise amplifier, Mach-Zehnder modulator, microwave photonics, radio-over-fiber, silicon photonics.**

I. Introduction

RADIO-OVER-FIBER (RoF) systems offer cost-effective and flexible solutions for emerging wireless communication systems. Fig. 1 shows an example of a RoF system that involves modulating the received wireless signal onto an optical carrier wave that is then distributed through optical fiber networks. The low-loss characteristics of the fiber enable locating the baseband processing unit in the central station (CS) [1]. Therefore, the front-end photonic receiver only needs to convert electrical signal to optical and transmit the modulated optical signal to the CS. This unit, called the remote antenna unit (RAU), significantly reduces system complexity by aggregating all demanding baseband computation in the CS. Moreover, wireless service can be enhanced by deploying multiple RAUs or by establishing innovative wireless systems such as road vehicle communication systems [2]. Additionally, fibers are highly secure, provide high bandwidth, have long life span and are easy to maintain. Furthermore, the system can leverage optical signal processing techniques to augment its functionality.

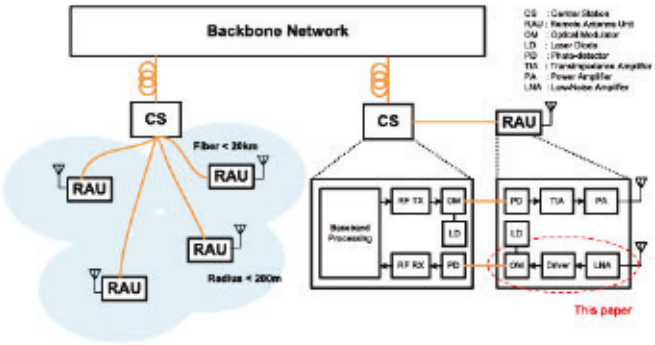

Fig. 1. RAU system example.

Many directly-modulated analog RoF links have been studied that do not incorporate or take into account the electrical front-end circuit within the system [3], [4]. Some other works chose not to integrate the electrical driver section with the photonic unit and instead utilize external drivers [5], [6]. Those works validate the RoF system concept and focus on the photonic chip design. However, it is imperative to integrate the front-end electrical circuit into the entire electronic-photonic system. For example, a 20 GHz broadband SiGe driver co-integrated with silicon photonic MZM was reported in [7], [8]. This process inherently offers higher current driving capability and lower noise figure compared to a CMOS process. Additionally, their segmented driving scheme helps enhance the optical and RF velocity matching and extend the bandwidth. However, this performance is achieved by adopting multiple power-hungry drivers that dramatically increases power consumption. To address the requirements of modern wireless communication systems, there is demand for low-cost, power-efficient, and highly-integrated RoF systems implemented in CMOS processes.

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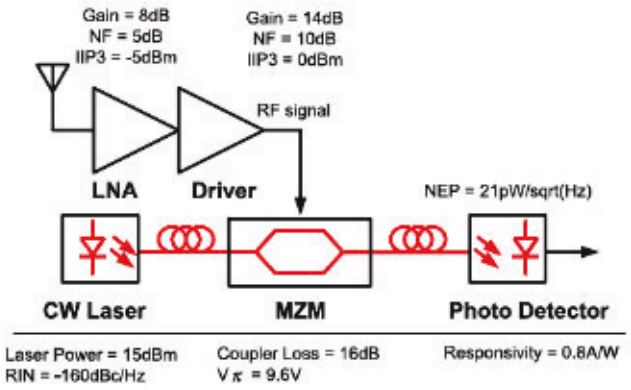


Fig. 2. Silicon photonic RoF link.

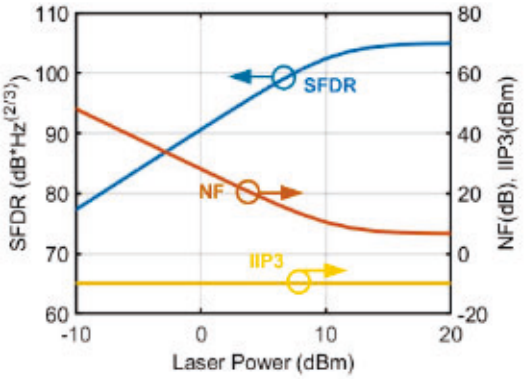
This paper presents a co-integrated silicon RoF link comprising of a wideband CMOS amplifier and a silicon photonic traveling-wave Mach-Zehnder modulator (TW-MZM). Expanding upon the RoF receiver described in [9], this work includes detailed system analysis, design details of the TW-MZM and electrical driver, and additonal measurement results with improved TW-MZM termination. The proposed RoF link operates within the frequency range of 16–32 GHz with a peak gain of 0 dB, IIP3 of 1 dBm and a driver power consumption of 209 mW. Section II presents analysis of the overall photonic receiver. Section III delves into the design of the silicon photonic TW-MZM. Detailed discussion on electrical driver circuit design techniques are provided in Section IV. Experimental results including the TW-MZM, driver, and integrated receiver are outlined in Section V. Lastly, Section VI concludes this work.

II. System Analysis

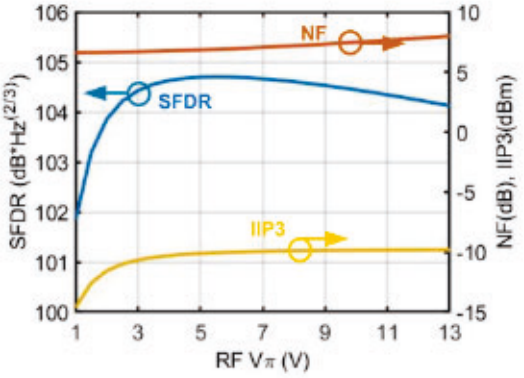
A testbench of the RoF system for link budget analysis is depicted in Fig. 2. The RoF receiver comprises of a front-end driver, optical modulator, photodetector and transimpedance amplifier. The overall system performance is evaluated using RF metrics for each component in the receiver link, primarily focusing on gain, noise figure, and IIP3, which describe the signal level, noise performance, and linearity of the overall system, respectively. To improve the minimum detectable signal and meet signal-to-ratio (SNR) requirements, an electrical driver is employed as the front-end circuit at the cost of linearity. The driver amplifies the received signal from the antenna and delivers a linear voltage swing to modulate the TW-MZM. The electrical gain (G_{MZM-PD}), noise figure (NF_{MZM-PD}) and $IIP3_{MZM-PD}$ of the optical link including TW-MZM and PD are represented by the following equations [10].

$$G_{MZM-PD} = aI_{dc}^2\pi^2 R_i R_o / \left(4V_\pi^2\right) \tag{1}$$

Here a is the electrode loss of the TW-MZM, I_{dc} is the sensed DC current of photodetector, and R_i and R_o are input and output resistances, generally 50 Ω. V_π is the RF half-wave voltage of the TW-MZM. The NF_{MZM-PD} is calculated by finding the ratio of total output noise over the thermal noise generated by input termination multiplied by gain.



(a)



(b)

Fig. 3. Link budget simulations that show the impact of (a) laser power and (b) RF-V_π on NF, IIP3, and SFDR performance for 15 dBm laser power.

$$NF_{MZM-PD} = \frac{N_o}{G_{MZM-PD}k_B T_s}, \tag{2}$$

where

$$No = \frac{1}{4}(RIN)I_{dc}^2 R_o + (NEP * R_{PD})^2 R_o + k_B T_s + k_B T_s G_{MZM-PD}. \tag{3}$$

Here RIN is the source laser relative intensity noise, NEP is the photodetector (PD) noise equivalent power, R_{PD} is the PD responsivity, K_B is the boltzmann constant, and Ts is the temperature during the operation. Assuming a linear PD, the IIP3 of MZM-PD is function of V_π.

$$IIP3_{MZM-PD} = \frac{4V_\pi^2}{\pi^2 R_i} \tag{4}$$

Assuming that the MZM operates at quadrature bias for maximum linearity, the impact of laser power on the Fig. 2 RF metrics is shown in Fig. 3(a). The gain of the MZM is a quadratic function of laser power. When laser power is too low, both the loss of MZM and the overall NF increase significantly. Consequently, the front-end circuit cannot solely dominate the noise performance for the overall system. It is noteworthy that

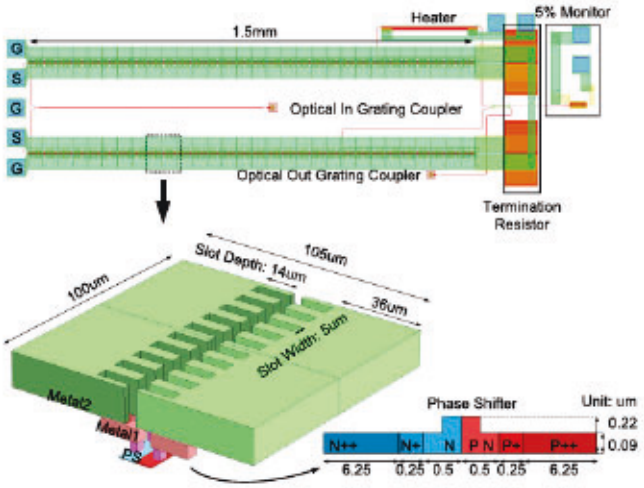


Fig. 4. Top and cross-section views of the proposed travelling-wave MZM in a 220 nm SOI process.

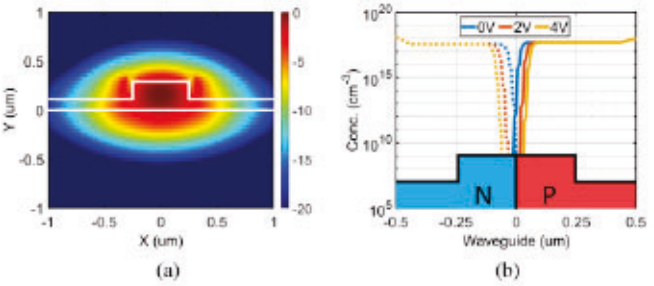


Fig. 5. Phase shifter (a) optical field and (b) charge distribution as a function of V_{RB}.

higher laser power contributes to higher RIN noise. Therefore, the gain value of the front-end circuit needs to be designed accordingly. In addition, as shown in Fig. 3(b), the MZM V_π stands out as one of the most critical parameters in the RoF link system. Its value determines the gain and the linearity of the MZM. When V_π is too low, it limits the linearity, whereas, a high V_π increases the MZM loss, thereby degrading the overall system noise figure.

III. Silicon Photonic MZM Design

A. Design Overview

Silicon photonic MZM plays a pivotal role in integrated wireless RoF links. Differentially driven MZM offers higher efficiency and eliminates second-order nonlinearity [11]. As illustrated in Fig. 4, the input optical signal is split into two arms of TW-MZM using a low loss Y-junction [12]. Each arm of the TW-MZM comprises of a 1.5 mm long PN depletion-based phase shifter, driven by a slow-wave transmission line (SW-TL). To achieve a precise control over the quadrature bias point operation for optimal gain and linearity, a thermal phase shifter is incorportaed along one arm. The output of the two arms are then combined using another low loss Y-junction. At the output, a 5% tap coupler facilitates closed loop bias control. In this design, the TW-MZM exhibits a simulated $V_\pi * L$ of 1.45 V-cm and 3-dB bandwidth of 39 GHz at 2 V reverse bias voltage (V_{RB}).

B. Phase Shifter Design

The PN-depletion based phase shifters are extensively researched for their high-speed operation and straightforward fabrication process [13]. The doping concentration and the geometry of the phase shifter greatly influence its optical performance. In this design, a lateral PN junction depletion based phase shifter is used. Upon applying a reverse bias voltage across the PN junction, a depletion layer forms, leading to a change in the number of free charge carriers within the waveguide core. The depletion of free charge carriers induces change in complex effective index of the optical mode, resulting in phase shift and absorption loss. An imbalance in the phase shift between both arms could cause either constructive or destructive interference at the MZM output, thus modulating the optical signal based on the applied voltage on the phase shifter. The efficiency of the phase shifter is typically characterized by $V_\pi * L$ (V-cm) representing the voltage required to achieve π phase shift for a 1 cm long phase shifter at a specific V_{RB}.

As shown in Fig. 4, the silicon waveguide is doped with P and N type carriers at the waveguide core. A low resistance path to the contact via is created by using higher doping levels. A higher concentration of the free charge carriers in the waveguide core produces large phase shift at the cost of high absorption loss. Considering the trade-off between phase shift and loss at the desired operating V_{RB} of 2 V, iterative simulations are performed to determine the N/P and N+/P+ lengths of the doping regions. The length of N++/P++ region is extended to reach the contact vias of signal and ground electrode of the SW-TL.

The phase shifter in this paper is designed using a MATLAB based algorithm in conjunction with the commercial solvers. Initially, the waveguide width and height are determined using effective index method, set at 500 nm and 220 nm, respectively, to allow a single TE mode propagation. This waveguide is simulated using Lumerical MODE [14] solver to obtain the 2D optical field profile for different wavelengths to extract optical group index (n_{opt}). The wavelength of interest for this design is 1550 nm. Next, Synopsys Sentaurus [15] is used to obtain 2D charge carrier distribution for different reverse bias voltages. The doping values are estimated using mobility models [16] and the typical sheet resistance values provided by the foundry [17]. Fig. 5 shows the optical field profile and charge profile for V_{RB} values of 0, 2 and 4 V. The simulated optical field (E), electron (Δe) and hole (Δh) carrier concentration profile are used in the following equations to calculate the change in effective index $\Delta n_{eff}(V)$ and loss $\alpha(V)$ where V is the applied reverse bias voltage [18].

$$\Delta n = -3.64 * 10^{-10}\lambda^2 * (\Delta e) - 3.51 * 10^{-6}\lambda^2 * (\Delta h)^{0.8} \quad (5)$$

$$\Delta\alpha = 3.52 * 10^{-6}\lambda^2 * (\Delta e) + 2.4 * 10^{-6}\lambda^2 * (\Delta h) \quad (6)$$

$$\Delta n_{eff}(V) = \frac{\int_x \int_y E^*(x,y) * \Delta n(x,y,V) E(x,y) dx dy}{\int_x \int_y E^*(x,y) * E(x,y) dx dy} \quad (7)$$

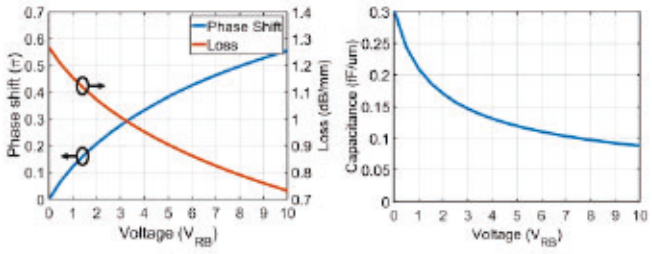


Fig. 6. (a) Phase shift, loss, and (b) capacitance of PN phase shifter for different reversed bias voltages.

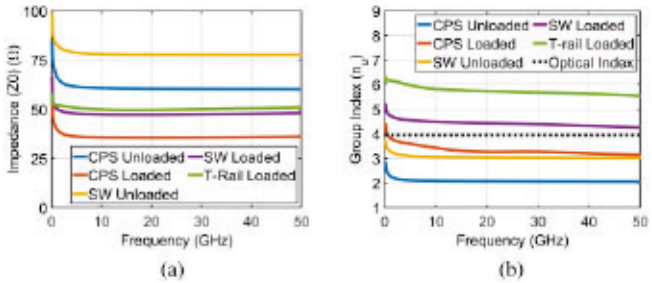


Fig. 7. Simulated (a) impedance and (b) group index of CPS, SW-TL, and T-rail-based electrodes of the TW-MZM.

$$\alpha(V) = \frac{\int_x \int_y E^*(x,y) * \Delta\alpha(x,y,V) E(x,y) dxdy}{\int_x \int_y E^*(x,y) * E(x,y) dxdy} \quad (8)$$

A MATLAB algorithm is developed to post-process the data obtained from the two solvers and perform numerical integration. The calculated $\Delta n_{eff}(V)$ is converted to phase shift using $\Delta\phi(V) = 2\pi\Delta n_{eff}(V) * L/\lambda$, where L is the length of the phase shifter. The simulated phase shift and loss at different V_{RB} are shown in Fig. 6(a). From the simulated phase shift data, $V_\pi * L$ is calculated as 1.45 V-cm at 2 V for a 1.5 mm long phase shifter. Finally, the capacitance in Fig. 6(b) is extracted from the charge profile data and used in the design of the SW-TL discussed next.

C. Slow-Wave T-Line Structure

Traditionally, electrodes with T-rails are used to design the SW-TL to achieve index matching by increasing capacitance of the transmission line. However, this practice tends to reduces the Z_0 and increases the RF index (n_u) of the transmission line. As shown in Fig. 7, n_u is much higher than n_{opt} to maintain the T-rail electrode Z_0 at 50 Ω. At RF frequency, impedance mismatch presents an undesired loading impedance to driver stage, while index mismatch reduces the MZM bandwidth. In [19], waveguide loops are periodically added to compensate the mismatch between n_{opt} and n_u and maintain the characteristic impedance (Z_0) of 50 Ω. Nevertheless, this approach incurs additional optical loss and increased device length compared to an MZM with no optical loops, for same modulation efficiency. We propose an inductive loaded SW-TL to attain a 50 Ω impedance and simultaneously match the optical and RF velocities.

According to transmission line theory, a lossless transmission line impedance is $\sqrt{(L/C)}$ and the RF index is $\sqrt{LC}$, where L and C are unit-inductance and unit-capacitance. In TW-MZM, the depletion capacitor (C_j) of the phase shifter acts as the dominant unit-capacitance of the transmission line. As shown in Fig. 6(b), C_j decreases with increasing V_{RB}. Lower C_j improves the SW-TL bandwidth, but compromises the phase shift efficiency. Thus, it is crucial to find the optimal C_j for high bandwidth, while achieving reasonable phase shift at a desired V_{RB}. Additionally, C_j influences the n_u of the SW-TL and causes optical and RF index mismatch, thereby reducing the electrical-electrical bandwidth (EE_{S21}) of the TW-MZM. EE_{S21} is defined as the ratio of electrical output power from photoreceiver to electrical input power and can be calculated using (9) shown at the bottom of this page [20], where L is the length of the SW-TL and β^u_{opt} is the difference between the RF and optical propagation constants. The S21 of the SW-TL structure ($S21_{SW-TL}$) captures RF loss and impedance mismatch effects and is primarily limited by the electrode length and PN phase shifter capacitance. This results in trade-offs between the TW-MZM bandwidth and efficiency, with a longer electrode length providing a lower V_π at the cost of reduced bandwidth. The 3-dB EE_{S21} is approximated to 6.4 dB $S21_{SW-TL}$ under perfect velocity and impedance matching conditions [20]. The reduction in 3-dB EE_{S21} from the 6.4 dB $S21_{SW-TL}$ is defined as bandwidth penalty. Hence, n_u of SW-TL should be as close as possible to n_{opt} to minimize bandwidth penalty.

Ansys HFSS [21] is used to run the electromagnetic simulation for the complete SW-TL structure. First, an unloaded co-planar stripline (CPS) is simulated to derive the RLGC parameters and determine the Z_0 and n_u. Fig. 7 shows the Z_0, n_u, and n_{opt} for an unloaded CPS and CPS loaded with C_j. However, the loaded n_u is 15% less than the n_{opt} of 3.95 and loaded Z_0 is 30% lower than 50Ω at the target bandwidth of 40 GHz. Adjusting L by maintaining constant C can increase the Z_0 and n_u due to their direct proportionality to $\sqrt{L}$. Using slow wave techniques described in [22], slots are adjusted by parameterizing the slot depth, shown in Fig. 4. Tuning the slot width affects both L and C, while changing slot depth solely increases L to better match the large optical group index. To achieve a target bandwidth of 40 GHz with minimal impedance and index mismatch a parameter sweep of slot depth is performed in HFSS as shown in Fig. 8(a). For a slot width of 5um and slot depth of 14um, the 6.4 dB $S21_{SW-TL}$ bandwidth is

$$EE_{S21} = 10\log\frac{|S21_{SW-TL}|^2 - 2 * |S21_{SW-TL}| * \cos(\beta^u_{opt} * L) + 1}{(ln\,|S21_{SW-TL}|)^2 + (\beta^u_{opt} * L)^2}, \beta^u_{opt} = \frac{\omega}{c}(n_u - n_{opt}) \quad (9)$$

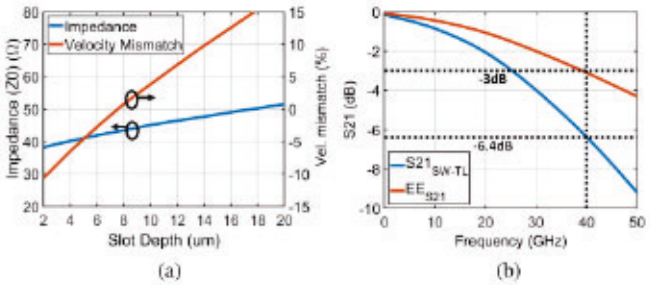


Fig. 8. (a) Impedance and velocity mismatch of SW-TL for different slot depths and (b) simulated TW-MZM EE_{S21} and $S21_{SW-TL}$ with 5 um slot width and 14 um slot depth.

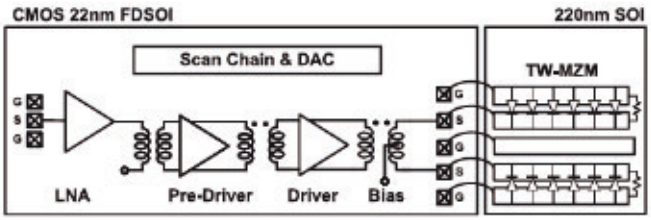


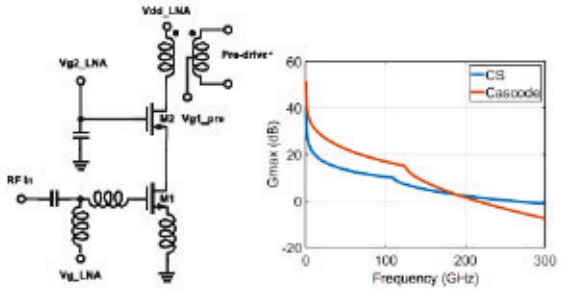
Fig. 9. Photonic link receiver architecture.

40 GHz with a Z_0 of 48Ω and index mismatch below 10% resulting in a bandwidth penalty of only 2.5%. Fig. 8(b) shows the simulated 6.4-dB $S21_{SW-TL}$ bandwidth of 40 GHz and 3-dB EE_{S21} bandwidth of 39 GHz.

IV. Electrical Driver Design

A. Overall Architecture

Fig. 9 illustrates the block diagram of the proposed differential MZM driver, realized in CMOS 22 nm FD-SOI process, alongside the TW-MZM shaping the entire photonic receiver link. An LNA serves as the first stage to improve the overall link noise performance followed by balun which is integrated into loading of the LNA. The pre-driver is a 2-stack-FET structure designed to provide gain to compensate the balun loss and enable high supply voltage operation with advanced CMOS technology nodes. The driver stage, employing a 3-stack-FET structure, further enhances the headroom of the supply voltage and is tailored to deliver a large voltage swing to modulate the MZM. The co-designed output matching network with magnetically coupled resonator (MCR) technique, at all inter and output stages, ensures optimal impedance matching for the driver and provide RF bandwidth extension. As it is crucial to minimize the inductance of the bond-wire of the connecting interface, the two chips, assuming similar height, are placed as close as possible. The inductance of the bond-wire is simulated as 150 pH using electromagnetic (EM) simulation. A GSGSG configuration is utilized for the interface between electrical chip and photonic chip. This configuration offers co-planar structure to help RF signal transition and allows individual characterization of two chips using RF probes. Detailed explanations and simulations results of each critical component are presented in the following subsections.



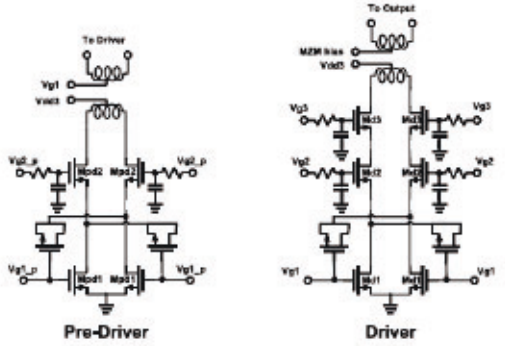


Fig. 10. (a) LNA schematic and simulated $G_{\max}$ of common-source and cascode topologies. (b) Pre-driver and driver schematics.

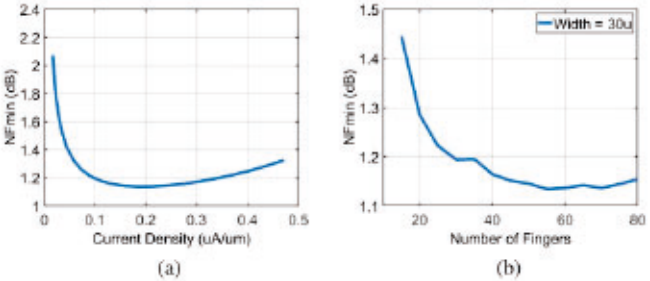
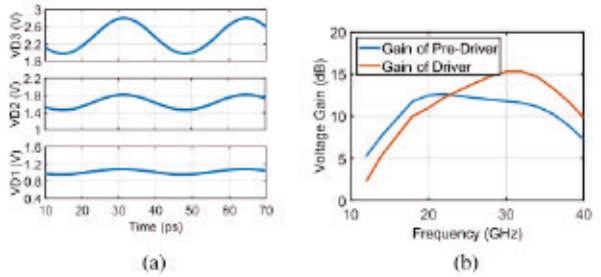


Fig. 11. (a) Optimal current density for $NF_{\min}$ and (b) optimal number of fingers for 30 um cascode transistor.

B. Cascode Low-Noise Amplifier

The first stage of the receiver front end circuit adopts a conventional cascode LNA shown in Fig. 10(a) [23]. The cascode structure is preferred for its high gain and high isolation performance within our target frequency range. A simulated maximum achievable gain ($G_{\max}$) is also shown in Fig. 10(a). The initial step in designing the LNA involves setting proper bias obtaining the optimum current density for achieving the minimum noise figure ($NF_{\min}$). The total transistor width is determined through iterative simulations considering noise and parasitics. The $NF_{\min}$ for this process is shown in Fig. 11(a). The optimal current density is determined to be approximately 160 uA/um. Subsequently, the optimal number of fingers can be determined through simulation as depicted in Fig. 11(b) where 40 fingers are chosen for compact layout. The input



(a) (b)

Fig. 12. Simulated (a) waveforms at the drain nodes of each transistor and (b) gain distribution of pre-driver and driver.

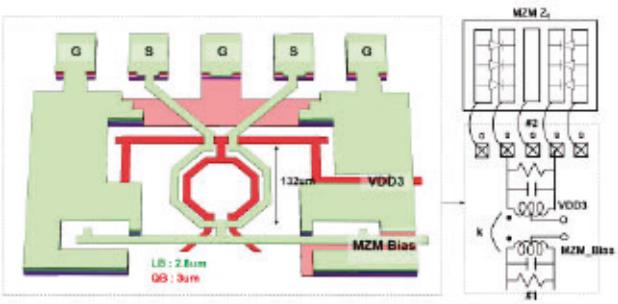
matching is implemented using an L-C network with inductive degeneration. The loading transformer is implemented using the MCR technique facilitating single-ended to differential signal conversion [24].

C. Stack-FET Amplifier

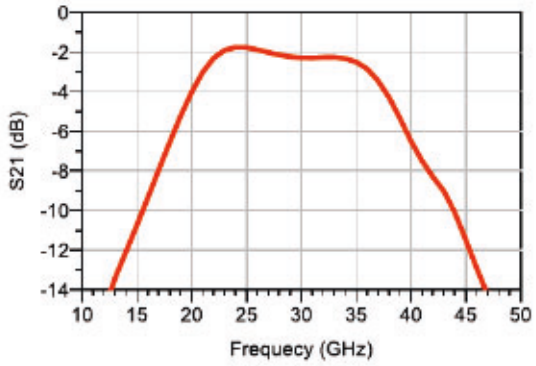
The schematic of pre-driver and driver are shown in Fig. 10(b). The stack-FET configuration involves connecting a common-source transistor in series with a common-gate transistor as a stack transistor. This arrangement differs from a cascode circuit, where the gate of the common-gate transistor is typically AC-grounded during operation. Instead, in the stack-FET configuration, the transistor that functions similar to a common-gate has its gate attached to a specific impedance, which allows the gate voltage to vary along with the signal. Theoretically, the output voltages of the transistors should add in-phase, ensuring that the current flows constantly through each transistor. To regulate the gate voltage swing of the stack transistor, capacitance at the gates of stack transistor needs to be designed. These capacitors, together with the transistor's inherent gate-source capacitance, create voltage dividers that establish the gate voltages. This technique differs from cascode amplifiers because it reduces the voltage changes across the drain-gate and drain-source when dealing with high-power signals, ensuring the reliability of the transistors even with a higher overall voltage swing [25].

A simulated waveform of the drain node of driver at 25 GHz is shown in Fig. 12(a). The waveform gradually amplifies along the common-gate transistor. The sizing of the transistor entails a trade-off between current driving capability, parasitic capacitance presented to previous stage and output stage. Specifically, eight parallel connected transistors with 40 fingers of 0.7 um width each are utilized for all transistor in the driver and pre-driver stages. For the driver stage, the output matching networks are designed to transform a 50 Ω to a 40Ω driver loading. The gain distribution is shown in Fig. 12(b). With proper design of matching networks, each stage exhibits a wideband response. The driver is designed for a high pass response to compensate for the output routing and bond-wire interface loss.

Additionally, at higher frequencies, capacitive neutralization techniques are adopted in the pre-driver and driver stages. Cross-coupled capacitors are implemented using MOSFET capacitors. The capacitance is designed as half of the main transistor to achieve the best isolation performance [26].



(a)



(b)

Fig. 13. (a) Layout and schematic of output stage with MCR structure and (b) simulated loading impedance of the output stage.

D. Interstage and Output Network Design

The MCR technique is used in the inter and output stage matching networks. This technique allows achieving a wideband bandpass response by splitting the resonant pole to higher and lower frequencies, respectively [24]. Additional parallel capacitors and resistors are incorporated to fine tune the flatness of the frequency response. Fig. 13(a) illustrates a 3D graph and equivalent schematic of output matching network. To co-design the photonic interface, the output stage needs to account for pad capacitance, bond-wire inductance and the input impedance of the TW-MZM. Fig. 13(b) demonstrates the wideband bandpass response of the matching network, considering all the parasitic effects. The transformed loading impedance is crucial for the driver stage because it determines the maximum output power of the driver stages. Detailed electromagnetic (EM) simulations are performed using ADS Momentum on the broadside-coupled transformer that implements the MCR layout [27].

V. Experimental Results

Fig. 14 displays the micrograph of the co-integrated CMOS driver and silicon photonics MZM. The bias voltages for the LNA and drivers are generated from an internal digital-to-analog converter (DAC) controlled by the scan chain. The RF input signal is applied via GSG probe, and the output of the driver connects to the input of the TW-MZM through bond-wire in GSGSG configuration. Two chips are mounted on a FR-4 PCB

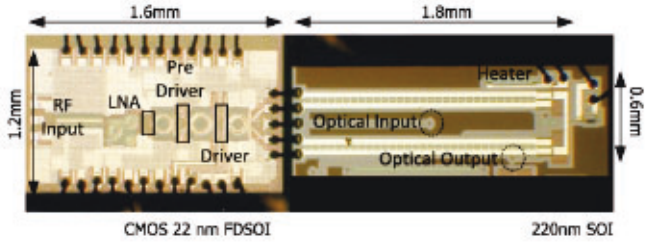
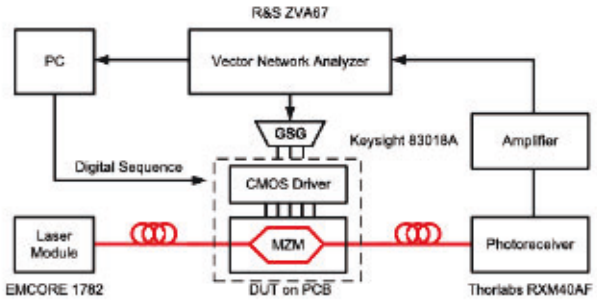


Fig. 14. Chip micrograph of driver and TW-MZM.



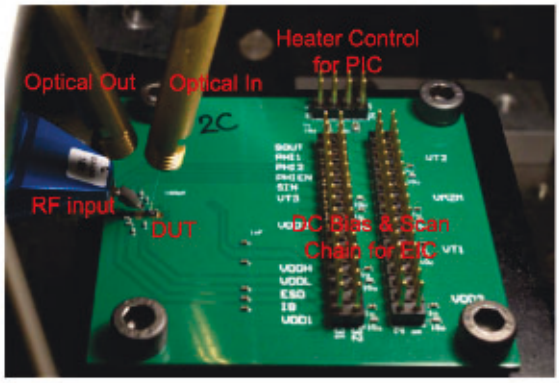


Fig. 15. RoF link measurement setup for frequency response and linearity measurements.

and placed as close as possible to minimize the bond-wire inductance. Fig. 15 illustrates the diagram and photo of the measurement setup. Probes, fibers and jumpers are arranged properly during the design phase to avoid physical hindrance. The supply voltage and heater control of the PIC are supplied externally through the PCB. A high power continuous-wave laser source (EMCORE 1782) is coupled via a grating coupler to the TW-MZM. The output modulated optical signal is connected to a photoreceiver module (Thorlabs RXM40AF) and an amplifier (Keysight 83018 A).

For individual TW-MZM measurement, GSG probe is changed to GSGSG probe to stimulate differential signal directly into the TW-MZM. For stand-alone driver characterization, it is performed by standard 4-side probe landing to supply the in/out RF and biasing signals simultaneously. Signal stimulation and s-parameter characterization are conducted using a vector network analyzer (R&S ZVA67). Noise figure measurement is carried out using a spectrum analyzer (R&S FSV) with a noise source (Pasternack PE85N1008).

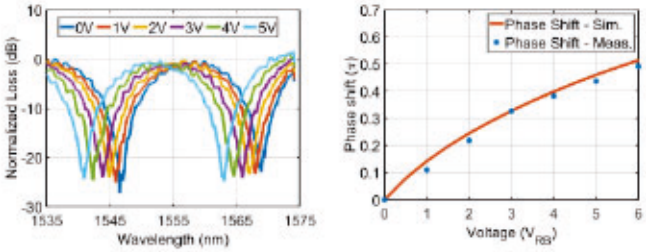


Fig. 16. Measured silicon TW-MZM (a) transfer function for different values of V_{RB} and (b) extracted phase shift.

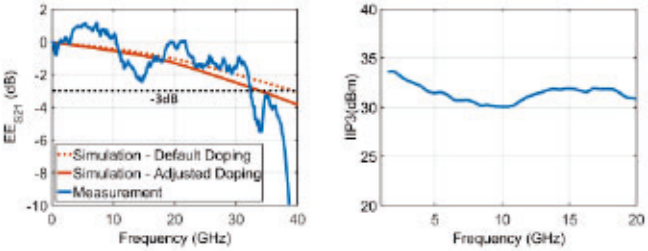


Fig. 17. Measured silicon TW-MZM (a) frequency response and (b) IIP3.

A. TW-MZM Measurement

The designed TW-MZM is characterized by first measuring the phase shift response, followed by the small signal response. Phase shift efficiency is evaluated by calculating the wavelength shift of the null in the imbalanced TW-MZM transfer function. A DC voltage sweep is applied to one arm of the TW-MZM while the other arm is set to 0 V. The imbalance in the TW-MZM is created by implementing a rib waveguide-based thermal phase shifter in one arm, resulting in an free spectral range (FSR) of 22 nm. The optical transfer function is measured using optical vector network analyzer (LUNA 5100), as shown in Fig. 16(a) . The total measured insertion loss of this differential TW-MZM is 11 dB in addition to 8 dB loss per grating coupler. The doping concentration of the fabricated TW-MZM is higher than the estimated doping during design, resulting in 3 dB higher loss than expected. Using the equations $\Delta\phi = 2\pi\Delta\lambda/FSR$ and $V_\pi * L = V_{RB} * L * \pi/\Delta\phi$, the phase shift efficiency $V\pi * L =$ 1.2 V-cm at 2 V is extracted, as shown in Fig. 16(b), where $\Delta\lambda$ is the shift in wavelength of null with respect to 0 V transfer function and L is length of the phase shifter in cm. Ideally, in a silicon photonic phase shifter, the phase shift should saturate with increasing V_{RB}; however, thermal effects were observed, causing additional phase shift at higher V_{RB}. The primary contribution of these thermal effects is the heat dissipation from the 50Ω termination resistor. To eliminate this effect, the shift ($\Delta\lambda$) in null of optical transfer function is extracted for lower V_{RB} values and extrapolated. In a future design, the termination resistor location could be altered to reduce thermal crosstalk on the adjacent waveguides. The photonic chip could also be thinned and placed on a thermoelectric cooler to stabilize the temperature.

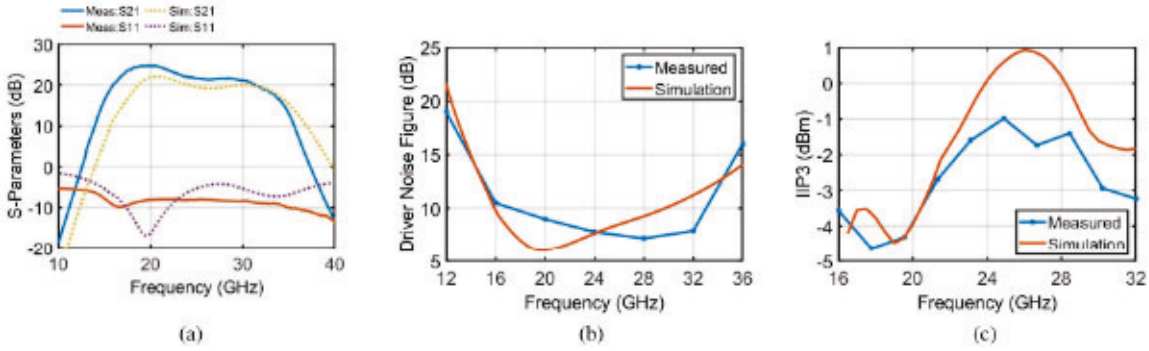


Fig. 18. Measured and simulated (a) *S*-parameters, (b) NF, and (c) IIP3 of the driver.

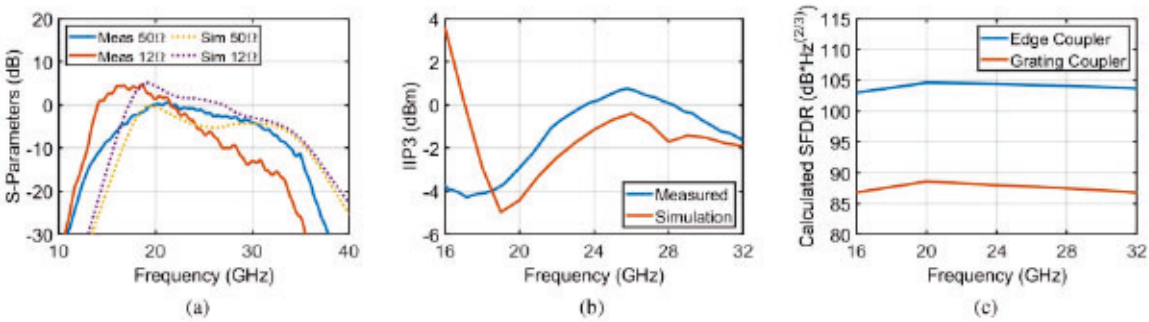


Fig. 19. Measured and simulated (a) *S*-parameters and (b) IIP3 of the RoF link. (c) Calculated SFDR of the link using 15 dBm laser power with −3 dB edge-coupler loss and −16 dB grating coupler loss.

For high-frequency measurements, a balun (Marki BAL-0036) is used to generate a differential signal from a R&S ZVA67 and this RF signal is applied to the TW-MZM using a GSGSG probe. Previous measurements in [9] showed a lower bandwidth due to a layout error with the TW-MZM termination resistor having a low 12Ω value. Using a focused ion beam technique, this termination resistor is trimmed to obtain 50Ω. Fig. 17 shows the measured EE_{S21} and IIP3 of the 50Ω terminated TW-MZM. Note that the IIP3 measurement is limited to 20 GHz because the IM_3 product is lower than the noise floor of the measurement setup at higher frequencies. Overall, the TW-MZM measurements exhibit a 3-dB EE_{S21} bandwidth of 32 GHz and a superior IIP3 of 30 dBm. Compared to the simulation results, the measurements show lower V_π, higher loss, and lower bandwidth, implying a higher doping level than expected. Figs. 16(b) and 17(a) demonstrate agreement between measurement and simulation results after adjusting for this doping variation. Incorporating process variations and designing for worst case doping during the design phase could help in better estimation of the overall TW-MZM performance. Further optimization could be achieved by shortening the MZM length and adding an additional electrical driver stage with increased transistor stacking for higher output swing. If higher linearity is required, the proposed TW-MZM structure could be modified to a dual-parallel Mach–Zehnder modulator topology [32] with an additional parallel version of the implemented MZM.

B. Driver Measurement

As the font-end stage of the RoF link, the driver performance is critical for the overall link. Fig. 18(a) demonstrates the measured and simulated S-parameters of the standalone driver (on-wafer probing). By adopting MCR techniques, the bandwidth of the driver covers 16-32 GHz and S_{11} is lower than -8 dB within the bandwidth. Fig. 18 also presents the simulated and measured noise figure and IIP3 of the driver. The noise figure varies from 7 to 10 dB within 16–32 GHz bandwidth, while the IIP3 ranges from −1 to −5 dBm. The power consumption of the driver is 209 mW.

C. Link Measurement

The frequency response of the RoF receiver for 12Ω and 50Ω terminated links is depicted in Fig. 19(a). Improper termination resistance corrupts the frequency response of the TW-MZM and provides incorrect loading impedance to the driver. The co-simulation is performed using a verilog-A based TW-MZM model [33]. The measured link performance of 50Ω terminated link achieves 16-32 GHz wideband response and follows the measured bandwidth of the driver. The measured and simulated IIP3 of the RoF link are shown in Fig. 19(b), which is dominated by the driver linearity. The simulated IIP3 is deviated from measurement because the bandwidth in simulation does not cover 16 GHz at the lower edge of the band as depicted in Fig. 18(b). Due to the high coupling loss of the grating coupler at the

TABLE I
PERFORMANCE COMPARISON

Reference	[28]	[29]	[8]	[7]	[30]	This work
Frequency (GHz)	1-18	2-30	0.5-20	1-20	20-35	16-32
Process	LiNbO3	LiNbO3	Si-SiGe	Si-SiGe	CMOS	CMOS
Power Consumption (mW)	N/A	N/A	1700*	1650*	180	209
Max Voltage Swing (Vpp)	N/A	N/A	2	3	2.5	2.5
IIP3 (dBm)	39.4	6.2	22	6.8	4.8** / -15$^{\triangle}$	1
Supply Voltage (V)	N/A	N/A	3.3	N/A	0.9 /1.6	0.8/1.6/2.4
NF	17-22	N/A	14-20	14-20	22 / 6$^{\triangle}$	38.1/13.5***
SFDR	124	85-111	109-120	101-109	99 / 101$^{\triangle}$	86-89/103-105***
Technique	Dual Series MZM	Discrete Predistorter	Co-design & IM3 Predistortion	Co-design	Predistortion	Co-design
Integration	Discrete	Discrete	Hybrid	Hybrid	Discrete	Hybrid

$^{\triangle}$ Simulated results of the link with measured NF, IIP3 of the driver and LNA in [31]
* Total power of 4 segments
** Measured IIP3 with driver-only RoF link
*** Calculated NF and SFDR performance with grating coupler/potential edge coupler

input and output of TW-MZM in this measurement setup, noise figure measurement of whole link is not possible. Therefore, the SFDR, shown in Fig. 19(c), is calculated based on measured RF metrics of the TW-MZM, Fig. 17, and the driver, Fig. 18. While the calculated SFDR is between 86 to 89 $dB * Hz^{(2/3)}$ with grating coupler, with 8 dB loss per coupler, it is possible to achieve 103 to 105 $dB * Hz^{(2/3)}$ if edge couplers, with 3 dB loss per coupler, are used [8]. As shown in Table I, the proposed work only consumes 209 mW which is much lower than other works with integrated SiGe driver and silicon photonics MZM. The receiver in this work operates at 16–32 GHz bandwidth and consists of a tightly integrated CMOS driver with silicon TW-MZM using a simple bond-wire connection.

VI. CONCLUSION

This paper describes the integration of a CMOS driver and a silicon photonic TW-MZM. The stack-FET structure helps mitigate the limitations of low supply voltage operation in CMOS processes. With an electrical chip power consumption of only about 209 mW, the proposed silicon TW-MZM achieves 32 GHz bandwidth with acceptable linearity performance. Moreover, the MCR technique is employed to co-design the TW-MZM input impedance and the bondwire connection. The overall RoF link is validated with bandwidth and IIP3 performance, achieving a 16–32 GHz wideband performance. An anticipated calculated SFDR of 105 $dB * Hz^{(2/3)}$ is expected with an edge-coupler design.

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