A 15-25GHz RF Photonic Front-End with 22nm CMOS Dual-Differential Driver and Silicon Traveling-Wave Mach-Zehnder Modulator

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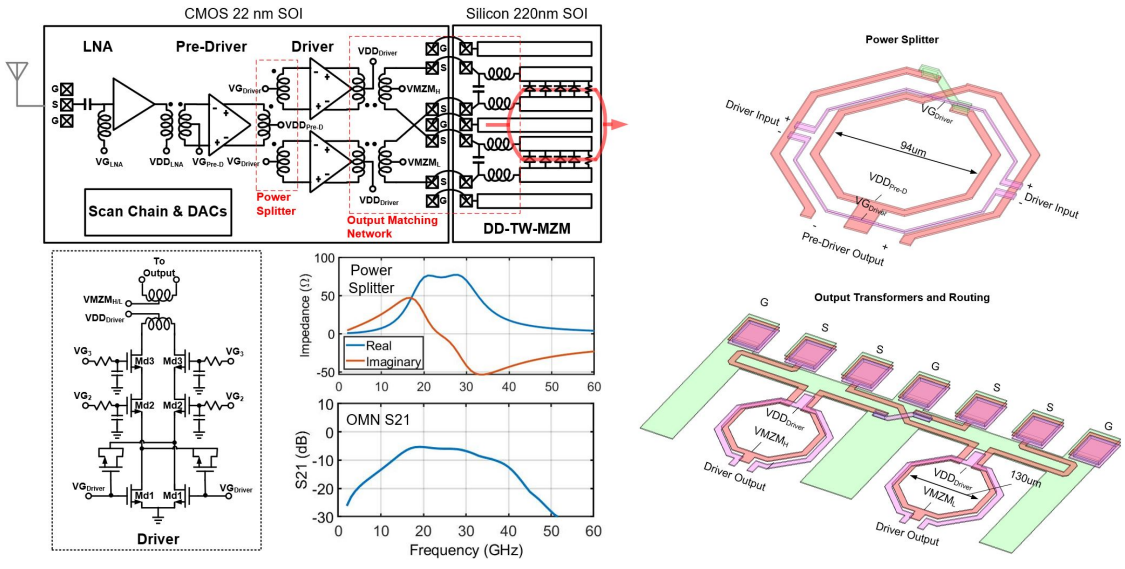
Abstract: A RF photonic front-end using dual-differential driving scheme is reported with a 22nm CMOS FD-SOI driver co-integrated with a silicon traveling-wave Mach-Zehnder modulator. The proposed front-end achieves 15-25GHz bandwidth with 2dBm IIP3 and consumes 448mW. © 2025 The Author(s)

1. Introduction

Radio-over-fiber (RoF) links convert RF signals into the optical domain for transmission through a fiber network. This approach enables future wireless communication systems by efficiently deploying RF receivers and heavy-processing central units [1]. The electrical driver circuit is expected to be linear, low-noise, and provide high gain to compensate for the high-speed travelling-wave Mach-Zehnder modulator (TW-MZM) loss. A differential driving scheme is preferable over a single-drive one, as it eliminates the second-order harmonic distortion effect. Dual-differential drive theoretically doubles the modulating driving voltage without deteriorating driver linearity [2] and allows for additional 6dB linear RF gain. Moreover, a dual-differential driver design can be naturally derived from a two-way power amplifier design, without the lossy power combiner at the output. In this work, the first wideband silicon RoF front-end using a dual-differential driving configuration is reported to the authors' knowledge. The proposed front-end consists of a 22nm CMOS FDSOI driver and a silicon photonic TW-MZM integrated circuit (Si-PIC) in a 220nm SOI technology. An impedance matching circuit is implemented on the Si-PIC and co-designed with the bondwires at the interface between two chips. The link operates over 15-25GHz and provides a peak 2dBm IIP3 over the band. The CMOS drivers consumes 448mW power.



(a) (b)

Fig. 1. (a) Dual-differential receiver font-end architecture and (b) layout of key passive structures implemented on the CMOS chip.

2. Dual-Differential Architecture and Driver Design

Fig. 1(a) shows the block diagram of the proposed dual-differential MZM driver and TW-MZM. The core circuit design of drivers and RF design techniques were explained in our previous work [3]. A compact power splitter and balanced output routing are added to complete the dual-differential driving scheme. A received wireless signal is be amplified by the input low-noise amplifier (LNA) and then converted to a differential signal by a balun. This differential signal is then amplified by the pre-driver and split into two ways by a power splitter. Three-stack-FET output drivers further amplify the signals to modulate each arm of the TW-MZM in the dual-differential configuration.

The dual-differential driving scheme can linearly double the modulation depth at the cost of design complexity. As illustrated in Fig. 1(a), a vertically-coupled power splitter is adopted to divide the signal for driving the two TW-MZM arms. An output matching network is designed to provide the desired loading impedance to the driver circuit with a low-loss transition over the entire operating frequency range for both drivers. The output matching network design consists of two output transformers, cross-routing, bonding-wires, pad capacitance, dedicated matching circuit on Si-PIC, and the characteristic impedance of the TW-MZM electrode. Fig. 1(a) also show the EM simulation results for the input impedance of the power splitter and S21 of the OMN covering the targeted frequency range. Fig. 1(b) shows the layout of the power splitter and output matching network units on the CMOS chip. The cross-routing is critical for the dual-differential drive and needs to be phase-matched between each signal to avoid gain penalty. DC biases are also labeled in the figure, with the MZM reversed-bias voltage fed from the center tap of the passive transformer layout to prevent high-voltage breakdown of the 22nm CMOS devices.

3. Dual-Differential Traveling-Wave MZM

Fig. 2 shows the layout of the dual-differential TW-MZM (DD-TW-MZM) with the LC matching circuit implemented on the Si-PIC. The overall length of the DD-TW-MZM is 2mm with 70% phase shifter loading. The depletion-mode PN phase shifter includes the doped 220nm waveguide core region connected to the slow-wave transmission line (SW-TL) using medium and high doped regions, N+/P+ and N++/P++ respectively in the 90nm thick slab. The N++ doping is also used for the 45Ω termination resistor. The electrode for each arm of the DD-TW-MZM is designed as a differential SW-TL in GSSG configuration. The SW-TL deploys capacitive T-rails and inductive slots [4] to achieve the desired bandwidth, while controlling the characteristic impedance Z_0 and index matching. However, the dominant loading of the PN phase shifter junction capacitor C_j creates a challenge in balancing the design specifications due to it's direct proportionality to RF index n_u and inverse proportionality to Z_0 and bandwidth. To address this, an LC matching network is added on Si-PIC to transform 100Ω at the CMOS driver output to DD-TW-MZM Z_0 of 45Ω including bond-wire inductance. The advantage of the matching circuit can be observed in S11, Fig. 2(b), which is below -10dB up to 40GHz. The simulated SW-TL 6.4dB bandwidth of 34GHz is also shown in Fig. 2(b). Secondly, the index mismatch is addressed by adding optical phase recovery loops after every 250um that reduce the delay mismatch between optical and electrical paths to approximately 5%.

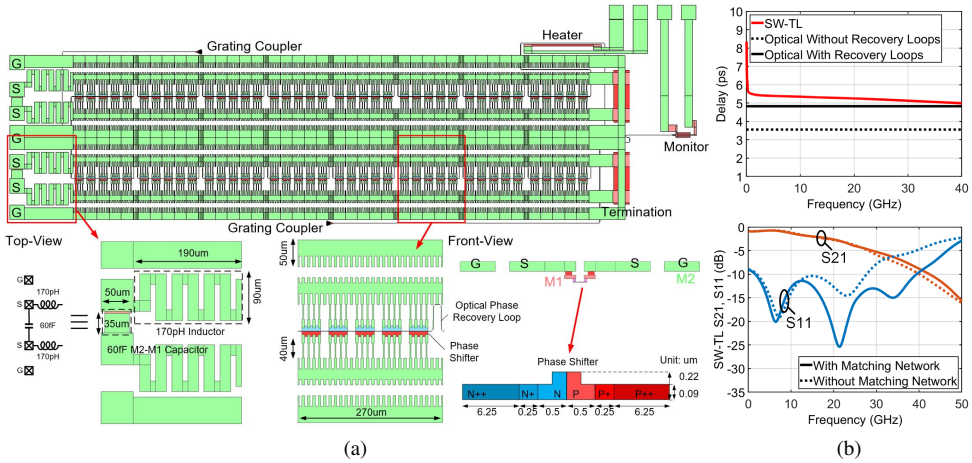


Fig. 2. (a) Layout of DD-TW-MZM including matching circuit and phase shifter. (b) Simulated delay time over 250um length and S-parameters of the proposed SW-TL in the DD-TW-MZM.

4. Experimental Results

Fig. 3(a) displays the micrograph of the co-integrated CMOS driver and Si-PIC. The output of the driver is connected to the input of the DD-TW-MZM through bond-wires in a GSSGSSG configuration. Both CMOS and

Si-PIC chips have approximately same height and are mounted on a FR-4 PCB as close as possible to minimize the bond-wire inductance. Fig.3(b) shows the measurement setup with a high-power continuous-wave laser source (EMCORE 1782) coupled via a grating coupler to the TW-MZM. The output modulated optical signal is connected to a photoreceiver module (Thorlabs RXM40AF) followed by an amplifier (Keysight 83018A). A vector network analyzer (R&S ZVA67) is used to measure the link gain. Fig. 4(a) shows that the driver and link frequency response covers 15-25GHz with S11 lower than -9dB. The link gain and the S21 can reach up to 6dB, excluding the grating coupler loss. Two-tone measurement are also performed to verify the linearity of the link as shown in Fig. 4(b,c). The input third-order intercept point (IIP3) of the link ranges from -4 to 2dBm over the operational bandwidth.

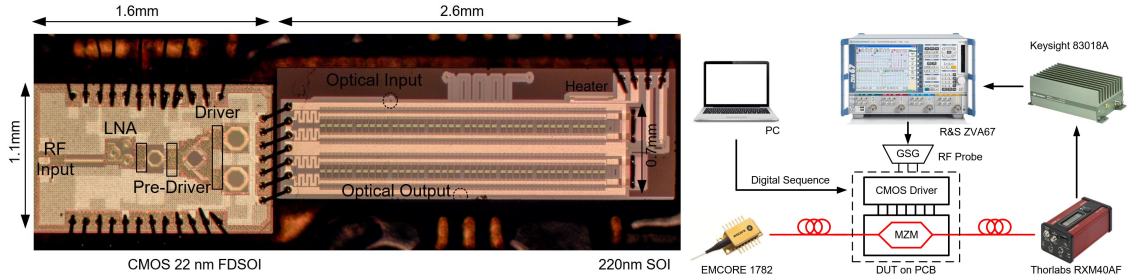


Fig. 3. Proposed RF photonic front-end (a) micrograph and (b) measurement setup.

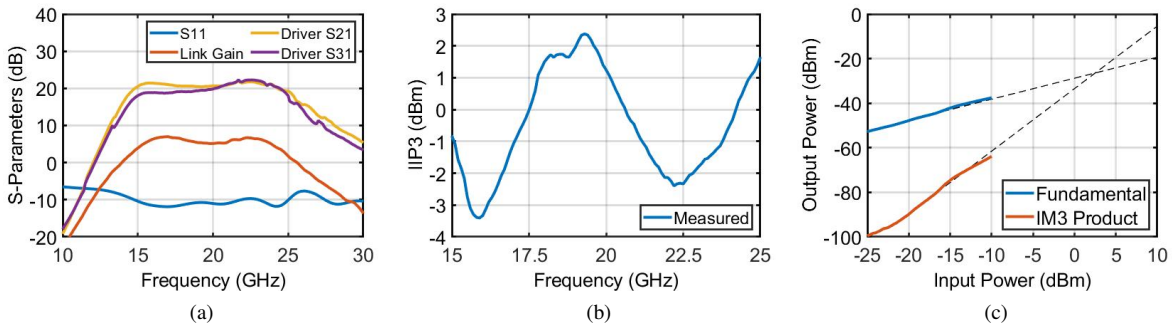


Fig. 4. Measured RF silicon photonic front-end (a) frequency response and two-tone measurement over (b) frequency and (c) input RF power at 20GHz.

5. Conclusion

This paper demonstrates an integrated RoF receiver front-end using an advanced dual-differential driving scheme to improve overall link gain of 5dB over a standard differential scheme. The silicon photonic DD-TW-MZM adopts SW-TL and optical phase recovery loop techniques to meet the bandwidth requirement while matching the optical and electrical group velocities. The interface between CMOS chip and Si-PIC is co-designed with bond-wire inductance and an LC matching network is implemented on the Si-PIC to improve impedance matching. The overall RoF link is validated with gain-bandwidth and IIP3 measurement, achieving a 15-25GHz bandwidth with peak IIP3 of 2dBm, while consuming 448mW DC power in the CMOS driver.

6. Acknowledgements

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