Computational Vector Stimulation for Spatially Targeted, Low-Latency Adaptive Neuromodulation With Common-Mode Artifact Suppression

Arindam Mandal, *Member, IEEE*, Diego L. Peña-Colaiocco, *Student Member, IEEE*, V. Rajesh Pamula, *Member, IEEE*, Steve I. Perlmutter, Forrest Pape, Jacques C. Rudell, *Senior Member, IEEE*, and Visvesh S. Sathe, *Senior Member, IEEE*

***Abstract*—This paper presents a technique for achieving spatially targeted neural stimulation with suppression of driver nonideality-induced common-mode (CM) artifact in low-latency closed-loop neuromodulation applications. The proposed approach utilizes computationally guided concurrent stimulation across multiple electrodes to achieve spatial selectivity in stimulation. The proposed architecture supports flexible storage of multiple, precomputed vector stimulation patterns in integrated memory. A selected stimulation pattern can be quickly accessed and administered in response to decoded neural activity. Additionally, a combination of the stimulator circuit architecture and mixed-signal current imbalance compensation techniques effectively suppress CM artifacts to below 50 mV. These techniques are demonstrated in a 180 nm HV CMOS test-chip containing 46 stimulation drivers of 26 V compliance and validated through a combination of bench, saline, and in vivo tests.**

***Index Terms*—Electrocorticography (ECoG), closed-loop neuromodulation, BCI, stimulator, targeted stimulation, vector stimulation, concurrent multichannel stimulation, artifact, high voltage (HV), digital-to-analog converter (DAC), current imbalance compensation.**

I. Introduction

ADAPTIVE neuromodulation has emerged as a groundbreaking approach in medical therapy, revolutionizing the treatment of neurological and neuropsychiatric disorders [1], [2], [3]. Unlike traditional open-loop systems, adaptive neuromodulation incorporates real-time feedback from the patient's neural activity to dynamically modulate and optimize the stimulation parameters. By directly interfacing with the nervous system, adaptive neuromodulation has the potential to provide significant therapeutic benefits for Parkinson's disease, epilepsy, chronic pain, and psychiatric disorders [4]. Furthermore, adaptive neuromodulation offers a deeper understanding of the underlying neural mechanisms involved in various disorders [5].

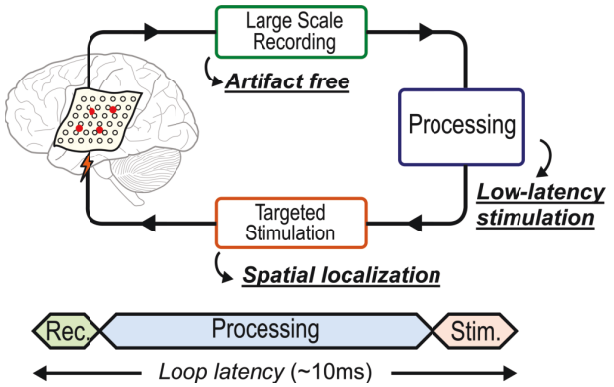

Fig. 1. Conceptual diagram of an adaptive neuromodulation system which includes neural recording, real-time digital signal processing with biomarker detection, and stimulation. Requirements on the stimulator for the next-generation neuromodulation system are underlined.

Fig. 1 depicts an instance of next-generation adaptive neuromodulation using a high-density microelectrode array. While large-scale, low-latency adaptive neuromodulation offers substantial therapeutic benefits, it introduces stringent demands on recording, processing, and stimulation components. The need for stable, low-latency control has heightened the need for continuous, uninterrupted neural recording, free of stimulation-induced artifacts. In conventional low channel-count stimulation systems, the recording front-end is typically "blanked" (disabled) during stimulation to prevent stimulation artifacts from saturating the recording front end [6]. However, high channel-count systems that look to stimulate different neuronal populations in response to recorded activity may experience a higher frequency of stimulation events. Mitigating the effect of increasingly frequent stimulation artifacts involves either more extensive blanking (resulting in blind spots) across recording channels, or a linearity degradation

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Arindam Mandal, Diego L. Peña-Colaiocco, and Visvesh S. Sathe are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: amandal41@gatech.edu; depenacol@gatech.edu; vsathe@gatech.edu).

V. Rajesh Pamula was with the School of Electrical and Computer Engineering, University of Washington, Seattle, WA 98195 USA. He is now with Medtronic Inc., Minneapolis, MN 55432 USA.

Steve I. Perlmutter is with the Department of Physiology and Biophysics, University of Washington, Seattle, WA 98195 USA.

Forrest Pape was with Medtronic Inc., Minneapolis, MN 55432 USA.

Jacques C. Rudell is with the School of Electrical and Computer Engineering, University of Washington, Seattle, WA 98195 USA.

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in the recording channels. Consequently, next-generation neuromodulation requires stimulation with artifact mitigation.

Latency requirements in adaptive neuromodulation – from neural sensing to stimulus delivery– typically lie in the range of within tens of ms [1], [7]. This loop delay is further burdened by increasingly complex signal processing, classification, and control algorithms that continue to be developed. Thus, it becomes necessary to facilitate the rapid selection and deployment of stimulus waveforms.

It is highly desirable that the stimulator activate only the desired regions of interest (ROIs) in neural tissue and suppress stimulation in unintended areas [8], [9]. Previous studies in neuroscience proposed the use of concurrent stimulation on multiple electrodes to achieve this spatial localization. However, only a limited number of prior stimulator circuits have demonstrated this benefit of multi-electrode stimulation. Valente et al. [10] were the first to demonstrate a 3-channel stimulator IC to achieve limited electric field shaping. More recently, [11] explored stimulation across a limited number of configurations of 8 electrodes to inhibit or evoke specific responses. However, a mathematical framework to systematically select the stimulus current amplitudes based on a desired stimulation target is lacking, and there continues to be a need for spatially localized stimulation. Previous stimulator circuits [12], [13], [14], [15], [16], [17], [18], [19] also lack the capability to rapidly recall and administer specific patterns while suppressing artifacts. To the best of our knowledge, our work presented in [20] is the first IC demonstration of ROI-targeted stimulation using both, algorithmic and circuit techniques. We define simultaneous stimulation of a large number of electrode channels, guided by a computational method, as *vector stimulation*.

Building on our prior work in [20], this paper focuses on addressing the requirements of next-generation preclinical adaptive neuromodulation research platforms utilizing localized stimulation. Here, we detail the following contributions: 1) Delivery of spatially selective stimulation using multi-channel current delivery and a computational framework; 2) Active mitigation of stimulator driver mismatch which impacts CM artifact amplitude and stimulation localization; 3) Low-latency selection and delivery of stimulus waveform by leveraging on-chip SRAM memory. These techniques are demonstrated and validated using an IC containing 46 stimulation drivers.

This paper is organized as follows: In Section II we discuss the system overview and architecture. The implementation of spatial targeting of neural tissue is explained in Section III. Section IV describes the details of the fabricated test-chip. Bench, in vitro, and in vivo measurements are presented in Section V. The limitations of the proposed stimulator are addressed in Section VI. Finally, we discuss the conclusions of this work in Section VII.

II. Proposed Stimulator Overview

A. Spatially Targeted Current Mode Vector Stimulation

Concurrent stimulation has been shown to achieve a targeted spatial activation profile [8], [9]. The spatial profile of the stimulation current shapes the electric field in the neural tissue. This electric field can thus be manipulated to evoke activity in the ROI while suppressing it elsewhere, as shown in Fig. 2. The *current vector* ($i_{\mathrm{STIM}} = [i_0, i_1, \ldots, i_{\mathrm{N}}]^T$, where N is number of stimulation electrodes), the collection of stimulus current assignment to each electrode, is determined by solving an optimization problem outlined in Section III.

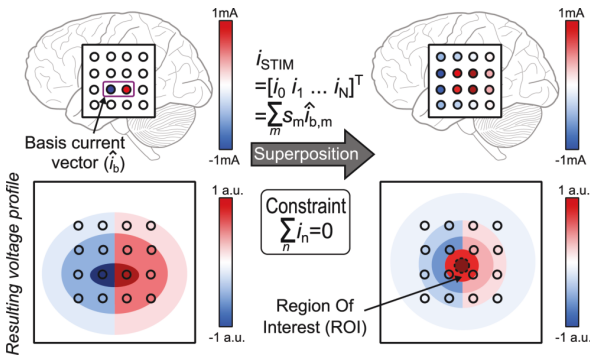

Fig. 2. Spatial voltage profile, that targets a ROI, arises from a combination of basis current vectors (right). The intrinsic voltage spread from an example basis current vector which consists of a source-sink pair is shown on the left. The scaling factors, s_{m}, of the basis vectors are determined by solving an optimization problem. A 4×4 rectangular electrode array is used for illustration. The number of electrodes is N and the number of basis current vectors is M.

Despite its potential to realize targeted stimulation, vector stimulation imposes additional challenges and requirements on the stimulator. These challenges, that arise at both the circuit and system level, are described in the following subsections.

B. Vector Stimulator Circuit Architecture

Vector stimulation requires the simultaneous delivery of source and sink currents across different electrodes. Hence, the proposed stimulator is equipped with 46 stimulation current drivers (shown in Fig. 3), each capable of delivering bipolar stimulation currents (source and sink). The amount of stimulus current (I_{STIM}) delivered by each driver is programmed by adjusting the current-DAC (IDAC) code at different time instants.

The optimization problem gives us a vector that achieves spatial localization. The end-user then scales this vector at different time values to form the stimulus waveforms. The timestamp and I_{STIM} value pairs are stored the integrated SRAM, which is partitioned to allow concurrent access by each stimulator channel. The architecture also offers flexibility in storing multiple stimulation waveforms. A digital controller allows for subsequent rapid recall of the I_{STIM} waveforms from the memory. The ability to generate arbitrary waveform shapes by storing timestamp and value pairs offers adaptability to meet the needs of various applications, such as achieving greater stimulation efficacy and energy efficiency [21], [22], [23].

C. Net-Zero Stimulus Current Delivery

It is crucial to ensure a net zero sum of applied stimulus currents at any given time ($\Sigma i_{\mathrm{n}}(t) = 0\ \forall t$). Henceforth we define this constraint as *current neutrality*. This prevents current flow

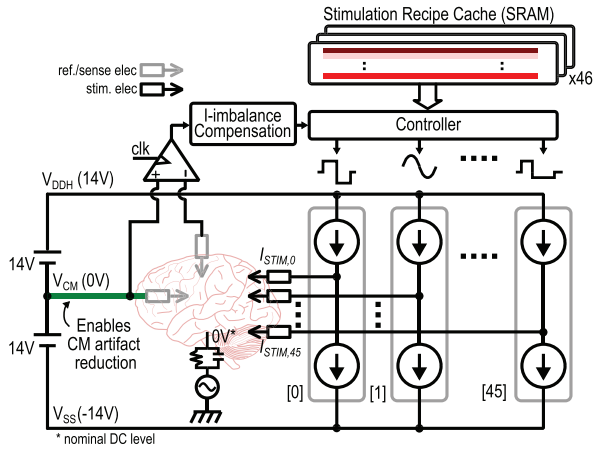

Fig. 3. Architecture of the proposed vector stimulator. The human body is modeled as a resistor connected in parallel with a parasitic coupling capacitance. An AC source is included to represent the effect of environmental noise coupling into the body relative to the earth ground.

through the ground electrode and prohibits undesired neural activation. However, previous spatially targeted stimulation implementations [8], [24], [25], [26], [27] have not maintained this neutrality of the stimulus currents. Achieving net-zero stimulus current delivery is particularly challenging in multi-channel stimulation setups.

In this work, we propose to satisfy the neutrality constraint by expressing the required current vector as a linear combination of basis current vectors, each ensuring net-zero current delivery. Fig. 2 illustrates how the combination of various source-sink pairs, used as basis vectors, can yield the desired voltage spread in neural tissue.

D. Artifact Free Stimulation

Any stimulation of neural tissue creates artifacts that interfere with the recording of the desired neural activity. We can classify the generated artifacts in two components: intrinsic and extrinsic. We refer to the artifact created by the voltage distribution in the tissue due to stimulus current flow as intrinsic artifact. The amplitude of this artifact is determined by the magnitude of the stimulation current and the relative distance and orientation of sense and stimulation electrodes. Meanwhile, the magnitude and waveform of extrinsic stimulation artifacts are influenced by the architecture of the stimulator circuit. Since this extrinsic artifact is seen by all sensing channels, we also define it as CM artifact. In this section we describe the mechanism that generates artifacts in vector stimulation and subsequently discuss how our proposed stimulator circuit mitigates this artifact.

The vector stimulation applies I_{STIM} concurrently across multiple electrodes. However, absence of any stimulus current neutrality constraint and on-chip variation across the IDACs and drivers results in an imbalance between the aggregate source and sink current being delivered at any given time. To mitigate the impact of this aggregate current imbalance, we introduce a low-impedance connection between the mid-rail of the supply (V_{CM}) and the brain using a dedicated electrode to provide a low-impedance path for I_{STIM} imbalance currents, shown in Fig. 4. Such a configuration sets the V_{SS} voltage

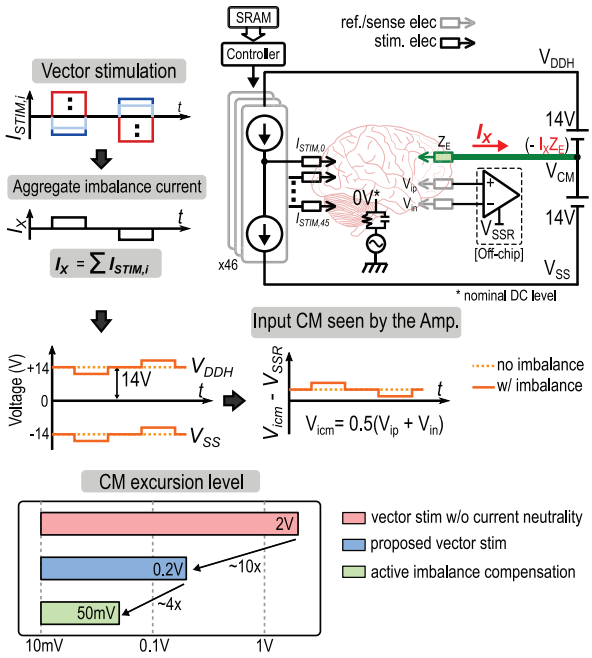

Fig. 4. Impact of current imbalance in vector stimulation. (Left) The aggregate source-sink imbalance current pushes one of the supply rails toward the brain/body potential. Consequently, this excursion appears as CM artifact at the input of a recording front-end which shares its ground with the stimulator. (Bottom) The proposed basis vector based stimulation approach, combined with imbalance compensation, significantly reduces the CM artifact level. Note that the supply rail (V_{DDH}, V_{SS}) potentials are referenced with respect to the brain/body potential.

to $-V_{DDH}/2$ (−14 V) which influences design of driver and comparator circuits, but is necessary in the absence of a deep N-well technology option. This anchor connection is similar in principle to the use of a reference electrode in [12], [28], and [29] where a deep N-Well was available.

When the imbalance current I_X flows through the anchor electrode of impedance Z_E, the worst-case supply excursion will be I_XZ_E. This excursion manifests as a CM artifact seen by the recording front-end, as illustrated in Fig. 4. This artifact affects the sensing capabilities of the recording analog front-end (AFE) in several ways: 1) The artifact amplitude can exceed the input CM range; 2) Sensing electrode impedance mismatches coupled with low input impedance of capacitively coupled AFE at high frequencies translates the CM artifact to a differential-mode (DM) voltage.

In the absence of the neutrality constraint, simulations show that I_X reaches the order of mA, leading to CM excursion levels as high as several volts. The proposed targeted stimulation approach, based on basis current vectors, ensures neutrality in DAC code assignments to the drivers, reducing CM excursion levels by nearly 10× (Fig. 4). The remaining CM excursion is primarily limited by the nonlinearity in the driver. If the metal encasement is used as the anchor electrode, its large surface area can further minimize the voltage excursion and the resulting artifact amplitude. However, additional V_{CM} excursion suppression mechanisms that do not depend on the geometry of the anchor electrode are well motivated to improve robustness. Therefore, the proposed stimulator architecture incorporates two additional current drivers for I_X compensation.

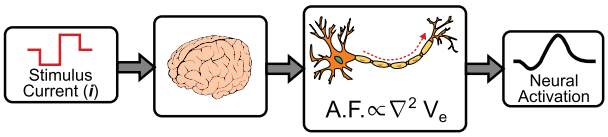

Fig. 5. Application of a stimulus current, $\boldsymbol{i}$ over a neural channel creates an electric field. The resulting spatial second derivative of extracellular voltage along the axon direction is considered as a metric for neural activation.

III. Spatially Targeted Stimulation Implementation

A. Background Theory

The mechanism of electrical stimulation in neurons has been extensively studied [30], [31]. Applying a stimulus current vector (i) to neural tissue generates an electric field that can activate or inhibit neurons, depending on their location. The activating function (AF) describes the direct stimulating influence of the extracellular potential (V_e) on a neuron fiber, induced by the application of i. For a long straight fiber with constant diameter, the AF is proportional to the second derivative of V_e along the fiber direction [30]. Fig. 5 illustrates this process behind neural activation. To approximate neural activation in a tissue volume, we define a scaled activating function (H_u) at location r as an inner product (quadratic form) of the Hessian matrix ($\nabla^2 V_e$), H, and the unit vector, u, along the direction of the axon fiber [8]. Thus, the approximate AF is written as

$$H_u(r) = \frac{\partial^2 V_e}{\partial r^2} = u(r)^T H(r) u(r). \tag{1}$$

AF based neural activation has been extensively investigated for deep brain stimulation (DBS) [8], [24], [25], [26], [27]. These studies explored formulating optimization problems (as functions of AF) to determine the electrode current settings that will achieve the desired neural activation patterns. They have mainly utilized electrode arrays with a single common return path. The computational models presented did not ensure net-zero current delivery through the stimulation electrodes. As a result, the previous approaches would induce significant voltage drops across the return electrode and create prominent CM artifacts in the recorded signals. To ensure the current-neutrality constraint, we propose to represent the stimulus current vector as a linear combination of basis current vectors, each of which constitutes net-zero current.

B. Selection of Optimal I_{STIM}

The I_{STIM} assignments are obtained by solving an optimization problem which is adapted from [8]. Here, we define the scaled activating function (SAF) that results from the application of the stimulus current vector as

$$SAF = H_{ub} \cdot i_b, \tag{2}$$

where H_{ub} is the Hessian projection matrix of the medium and i_b presents the coefficients of the basis current vectors. The H_{ub} matrix is partitioned into two distinct parts, corresponding to the target and the avoidance region. Thus, eq. 2 can be rewritten as

$$\begin{bmatrix} SAF_{targ} \\ SAF_{avoid} \end{bmatrix} = \begin{bmatrix} H_{ub,targ} \\ H_{ub,avoid} \end{bmatrix} \cdot i_b. \tag{3}$$

A convex optimization problem is formulated to maximize the average value of SAF (SAF_{avg}) in the ROI, while ensuring that SAF remains below the sensitivity threshold in the avoidance volume. Formally, the convex optimization problem is defined as

$$\text{Maximize} \quad SAF_{targ,avg}, \quad s.t. \quad SAF_{avoid} < \alpha \tag{4}$$

The solution to the problem provides the coefficients for the basis current vector, and subsequently the individual electrode currents are computed.

To solve the optimization problem outlined above, we first estimate the H_{ub} matrix. When i_b is an identity matrix, SAF equals H_{ub}. Using the superposition principle for the applied basis current vectors, the evaluated SAF for a basis vector corresponds to each column in the H_{ub} matrix. We calculate SAF by observing the voltage profile in the 3D tissue volume and taking the Hessian projection along the direction of the axon.[1] Fig. 6 illustrates this process of formulating H_{ub}.

Due to the unavailability of an FEM model of the neuron, we employed a 3D resistive mesh to emulate an isotropic conductive tissue. In this emulation, we assume that the target axon is oriented in a specific direction within a defined region.

Use of (linearly independent) basis current vectors minimizes the size of the Hessian projection matrix. Since any non-adjacent source-sink pair can be expressed as the sum of neighboring source-sink pairs, the chosen unique set of basis vectors is composed of neighboring source-sink pairs. Note that the choice of the basis vector will also vary depending on the geometry of the electrode array.

IV. Circuit Implementation

A. Memory Architecture & Controller

Fig. 7 depicts the SRAM architecture and the associated controllers. The SRAM cache stores the pre-computed I_{STIM} waveforms to facilitate rapid retrieval and application by the controllers. The collection of current waveforms required for a specific activation is defined as a *stimulation recipe*. A complete stimulation trace/waveform is characterized by the following parameters: timestamp, DAC code, output current direction, and passive regeneration enable logic. Each stimulation phase is followed by a passive regeneration phase, which serves to discharge any residual electrode voltage resulting from cathodic-anodic imbalance. The 14-bit timestamp allows for the generation of a 16 ms long trace with a 1 MHz system clock.

The integrated memory is partitioned into 6 segments, each with a capacity of 828 Bytes. Each SRAM segment is dedicated to storing the stimulation recipes for 8 channels. The memory architecture supports a maximum stimulus waveform length of 90 time-steps. To accommodate variable waveform lengths for each channel, the corresponding cache segments are addressed by separate scan-chain programmable *Begin* and *End* address pointers.

A recipe look-up table (LUT) stores the location information of the cache segment responsible for storing the specific

[1]This operation is analogous to channel estimation that is performed in communication systems.

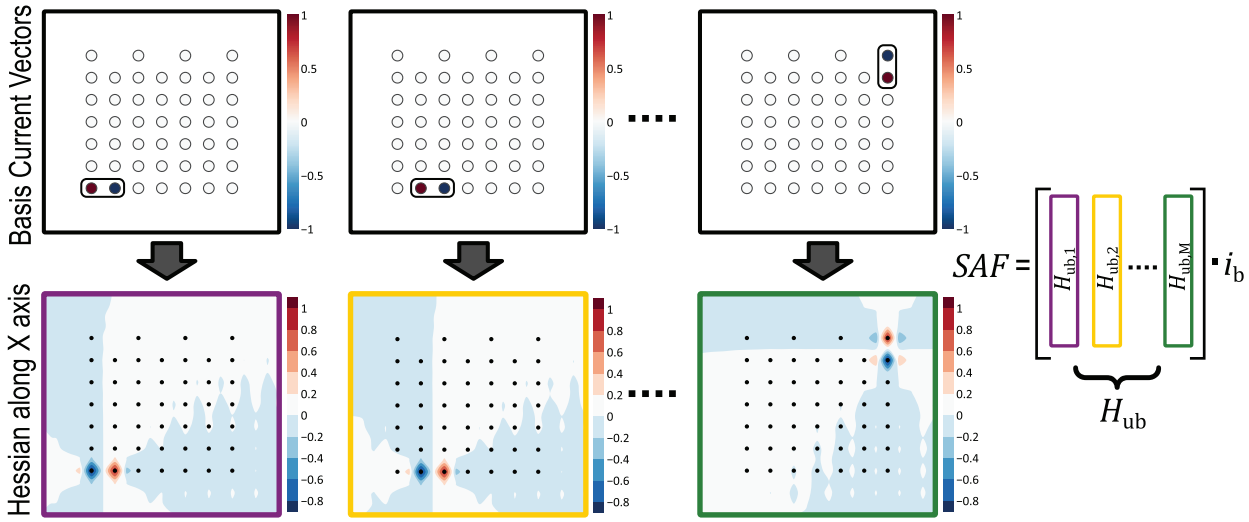

Fig. 6. The spatial second derivative of the generated voltage profile along the axon direction (X axis in this example) in response to different basis current vectors. The Hessian projection associated with a basis vector corresponds to each column in the H_{ub} matrix. Hessian values are normalized. The number of unique basis vectors is M.

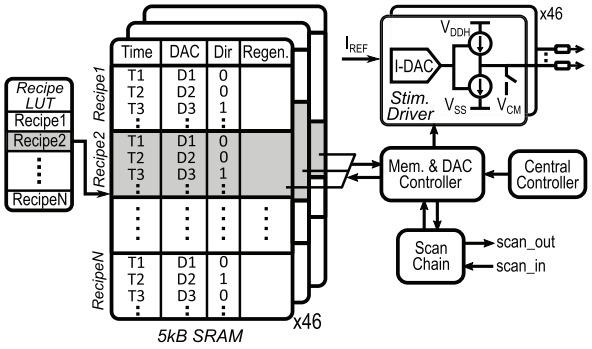

Fig. 7. Architecture of the memory and associated digital controllers.

stimulation recipes corresponding to each channel. This LUT organization enabled rapid switching between different stimulation recipes, enabling neuroscientists to efficiently explore various stimulation parameters and adapt them to specific experimental requirements.

A memory controller retrieves the traces from the memory with a single clock-cycle latency. Subsequently, a DAC controller is responsible for transmitting the appropriate DAC code and current direction to the stimulation driver at the designated time.

In typical neural stimulation applications, a single stimulation cycle often lasts several seconds. However, memory limitations restrict trace lengths to 16 ms. A central controller is incorporated to introduce additional delay between each stimulation event and allow low-frequency stimulation. This controller also enables the delivery of the current waveform in a free-running manner or for a finite number of cycles as defined by the user.

B. Imbalance Compensation Controller

To suppress the imbalance current (I_X in Fig. 8) in vector stimulation and mitigate the associated stimulation artifact, as well as prevent electrode charge accumulation, our proposed approach combines two novel techniques: concurrent imbalance compensation (CIC) and residual imbalance compensation (RIC). The compensation DAC code, computed by the CIC and RIC controllers, is subsequently fed to two dedicated stimulation drivers. Fig. 8 provides a visual representation of how these techniques effectively reduce I_X and discharge the resulting residual electrode charge.

Both techniques require the AC voltage across the CM anchor electrode – resulting from I_X flow – to be fed back for compensation. This voltage drop can also be inferred by observing the difference between V_{CM} and sensed brain potential (V_{CM_SEN}) which is obtained using another dedicated electrode adjacent to the CM anchor electrode. To ensure compatibility with HV inputs, the comparator inputs undergo capacitive division and are reduced below 5 V before sampling by a strong-arm latch [32]. A differential divider is used for symmetry. However, this capacitive division floats the latch inputs, requiring a periodic reset to a common bias voltage (V_{BIAS} prior to performing any imbalance compensation. The capacitor division ratio used is 100fF: n 100fF, where n is programmable between 1 to 7. The kT/C noise introduced due to the reset switch is less than 0.15 mV. Simulations of the comparator indicate a mismatch-induced offset (1σ) of 5 mV, and an input-referred thermal noise less than 1 mV.

1) Concurrent Imbalance Compensation (CIC): The objective of CIC is to generate a compensation current (I_{CIC}) with a waveform opposite to that of the imbalance current (I_X). I_{CIC} waveform is unique to each recipe and, therefore, needs to be determined only once during initial stimulation. Afterwards, the I_{CIC} waveform is stored in an on-chip register file and delivered together with the stimulation recipe.

The I_{CIC} waveform is designed to compensate for any changes in I_X resulting from magnitude changes in I_{STIM} waveforms. The potentially nonuniform time interval between successive changes in I_X is defined as a time-slice. The controller performs a successive approximation register (SAR) based search to determine the 5-bit DAC code for the CIC driver at each successive time-slice (Fig. 8(b)). In the first stimulation cycle, the polarity of the imbalance during the

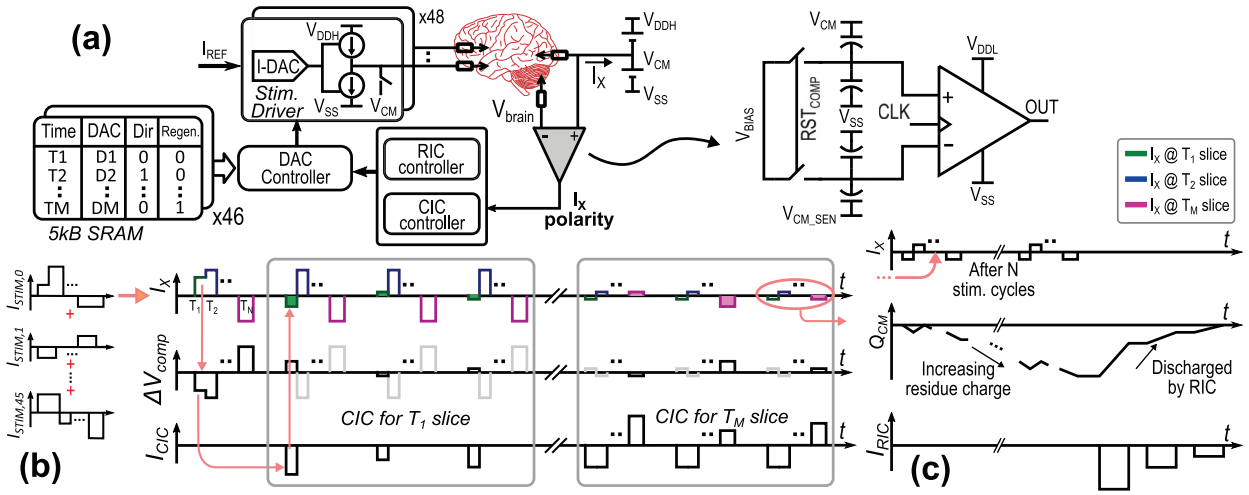

Fig. 8. (a) Implementation of the current imbalance compensation scheme. A capacitively coupled clocked comparator is used to sense the polarity of the AC voltage across the CM anchor electrode, which represents the imbalance current flow direction. (b) Concurrent imbalance compensation (CIC) in action. The required I_{CIC} for each time-slice is computed consecutively. The shaded pulses in the I_{X} waveform indicates the associated time-slice (T_{m}) for which CIC is active (c) Residual imbalance compensation (RIC) transient waveforms.

first time-slice is sensed and half of the maximum allowable I_{CIC} with the correct polarity is applied. The remainder of the stimulation trace continues without any further adjustment. In subsequent stimulation cycles, the I_{CIC} update step size (I_{s}) is halved and I_{CIC} is adjusted based on the feedback from the comparator. This process continues for the current time-slice until the CIC step size reaches unity. Subsequently, the following time-slices are compensated in the same manner. The following equations summarizes this SAR-based search for the required CIC DAC code:

$$I_{\mathrm{CIC,Ti}}[n] = I_{\mathrm{CIC,Ti}}[n-1] + I_{\mathrm{s}}[n]\ \mathrm{sign}(I_{\mathrm{X}}[n])\ \ for\ i = m, \quad (5)$$

$$I_{\mathrm{s}}[n] = 0.5\ I_{\mathrm{s}}[n-1], \quad (6)$$

$$I_{\mathrm{CIC,Ti}}[n] = I_{\mathrm{CIC,Ti}}[n-1]\ \ for\ i \neq m, \quad (7)$$

where, $I_{\mathrm{CIC,Ti}}$ is the CIC DAC code at T_{i} time-slice, m is the time-slice index for which CIC is taking place, n is the stimulation cycle index during ongoing CIC for T_{m} slice and it varies up to the CIC DAC bit-width. CIC results in I_{X} cancellation up to the CIC DAC resolution limit. Improved resolution can be achieved by scaling the CIC driver reference current.

Due to memory size constraints, the CIC is limited to defining compensation current waveform with a 5-bit resolution for up to 32 time-slices. The worst-case CIC waveform computation latency is therefore $32 \times 5/f_{\mathrm{stim}}$, where f_{stim} is the stimulation frequency.

2) Residual Imbalance Compensation (RIC): The sub-LSB (least significant bit) residual imbalance current waveform may not be charge neutral, accumulating charge on the CM anchor electrode interface capacitor. RIC is introduced to address this challenge. The modest residual charge is allowed to accumulate over a user-programmable number of stimulation events before a compensatory charge is provided through the residual imbalance compensation current (I_{RIC}).

I_{RIC} injection is initiated between two consecutive stimulation cycles and passive regeneration is disabled until the RIC process is complete. The initial scan-programmable I_{RIC} pulse discharges the residue using polarity feedback from the comparator. The pulse continues until this polarity reverses. However, electrode I-R drop introduces an error in the sensed voltage resulting in under-compensation. Therefore, subsequent discharge operations are performed, each with successively halved I_{RIC} pulse magnitude (Fig. 8(c)). Thus, RIC presents an effective way to discharge any residual charge.

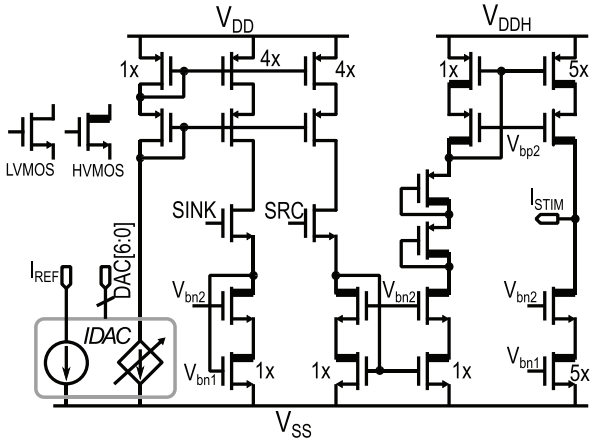

Fig. 9. Schematic of the stimulation current driver with internal IDAC.

C. Stimulation Driver

Fig. 9 shows the schematic of the stimulation driver. Each stimulation driver incorporates a 7-bit binary weighted nMOS current DAC (IDAC). The output current from the DAC is directed to the source and sink drivers. To conserve power, the IDAC and its output mirror are implemented using 5 V devices. The source and sink current drivers utilize HV LDMOS transistors, and the mirror ratio for both is set at 1:5. To maximize driver compliance and maintain an output impedance of at least 4MΩ, a wide-swing cascode current mirror is employed. The maximum deliverable I_{STIM} is 2.5mA, and it can be adjusted by tuning the bias current of the IDAC. With the stimulator supply voltage set at 28 V, the dropout voltage at maximum output current is limited to 1 V to lower per-channel area usage.

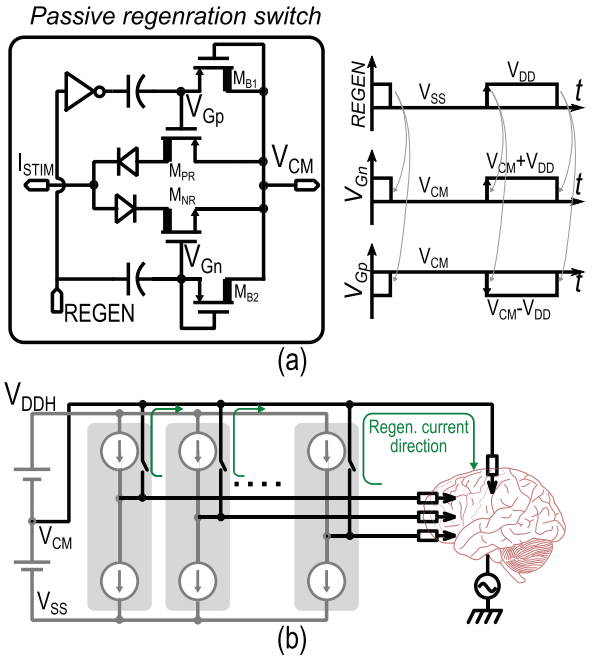

Fig. 10. (a) Schematic of the passive regeneration switch with switching waveforms; (b) passive regeneration current flow direction in a vector stimulation.

The cascode bias voltages (V_{bn2} and V_{bp2}) are shared among the drivers and generated using an on-chip bias generation circuit. To minimize area usage, the driver control switches SRC and SINK are located in the 5 V domain. The output impedance of the HV devices degrades at high drain-source voltages. To reduce the voltage stress on the HV nMOS stack in the bias leg of the source current mirror, a series of diode-connected transistors are inserted there.

Each stimulation driver also includes a passive regeneration switch. The schematic of this switch is shown in Fig. 10. The switch connects the stimulator output to the V_{CM} node through the electrode-tissue interface, discharging any residual charge in the electrode capacitance. All passive regeneration switches in the drivers are enabled together when no channel is delivering stimulation current. Accumulation of residual voltages is inevitable as a result of the inherent impedance mismatch of the electrode. By shorting all electrodes together through the anchor electrode, this residual voltage is significantly lowered. The path of current flow during passive regeneration is illustrated in Fig. 10(b).

The core of the switch consists of a HV transmission gate (Fig. 10(a)). Since the rated gate-to-source voltage of the HV devices is limited to 5 V, the gate voltages the transmission gate devices must be elevated relative to V_{CM} depending on the 5 V control logic, REGEN, which is referred to the chip V_{SS}. To achieve this level shift, we employ a bootstrapping technique utilizing two metal-oxide-metal capacitors. Two p-n junction diodes are placed in the current flow path of the transmission gate to prevent undesired conduction current flow arising from the polarity of the voltage difference across the stimulator output and V_{CM}. Under typical stimulation intervals and pulse-widths, the diodes discharge electrodes with adequate effectiveness, bringing their potential to below 150mV.

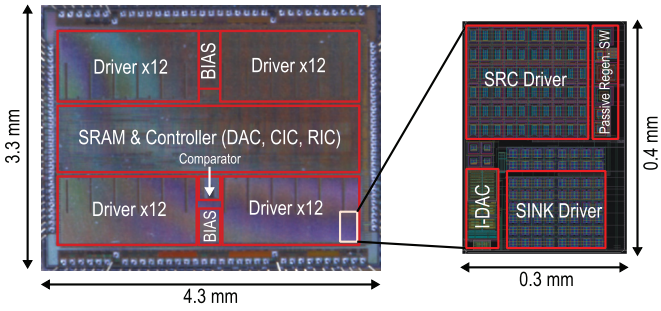

Fig. 11. Microphotograph of stimulator test-chip.

V. Measurement Results

The prototype stimulator chip is fabricated using the TSMC HV 180 nm 1P6M BCD process. The die microphotograph is shown in Fig. 11. Each current driver has an area of 0.12 mm^2. The total silicon area is 4.3 mm $\times$3.3 mm. The chip features 3 voltage domains: the digital logic and SRAM operates at 1.8 V, the biasing circuit and IDACs are supplied by 5 V, and the HV supply of the drivers can go up to 28 V.

As the proposed stimulator operates in a floating configuration relative to the brain/earth-ground potential, all internal power supplies are derived from a 5 V Li-ion battery bank. The required HV supplies (14 V, 28 V) are generated using two DC-DC boost converters, while lower voltage levels are generated using off-the-shelf, low dropout (LDO) regulators.

The boundary scan of the chip, managed by a PC, requires consideration for signals referenced to the earth-ground interfacing to a chip whose substrate is held at V_{DD}. A digital isolation circuit (Si862x) is integrated on the PCB to provide galvanic ground isolation between the chip's boundary scan and the data acquisition system connected with the PC.

Several experiments are conducted with various electrode configurations to validate the performance of the stimulator. Measurement results from these experiments are described below.

A. Measurements With Passive Electrodes

The test-PCB incorporates passive electrodes constructed with discrete resistors and capacitors to emulate the tissue-electrode interface. For these emulated electrodes, the resistance can be chosen between 560 Ω, 4.7 kΩ, and 10 kΩ. A combination of 10 nF or 22 nF capacitors emulates the double-layer capacitance of the electrode-tissue interface. Additionally, a 5 GΩ resistance is connected in parallel with the capacitors to represent the charge transfer resistance.

Fig. 12 shows demonstrative current waveforms that can be generated on four source-sink pairs. These waveforms exemplify the ability to deliver various types of stimulation waveforms, such as sinusoidal, exponential, rectangular, or even arbitrary shapes. The stimulator output currents are measured by looking at the voltage difference across the resistive electrodes.

We observe significant variation across the output current of the 46 stimulation drivers associated with the same DAC code. Fig. 13(a) presents the histogram of the average LSB current observed in each stimulation driver. The standard deviation

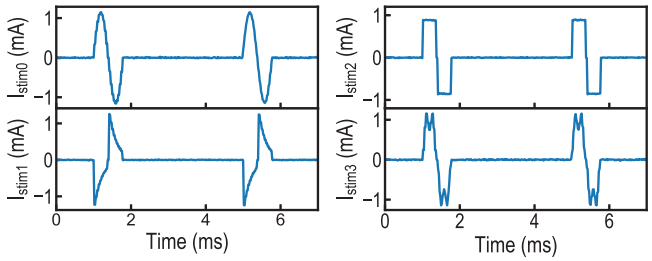

Fig. 12. Arbitrary stimulus current waveforms between four source-sink pairs. Resistive electrodes (4.7 kΩ) were used for this measurement.

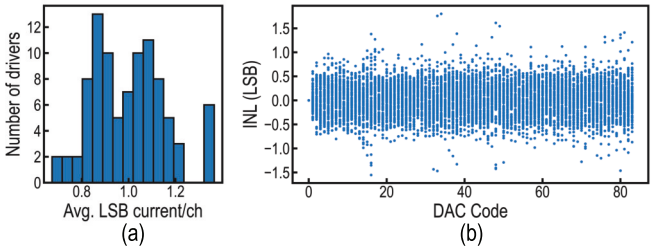

Fig. 13. (a) Variation of the average LSB current in each stimulation driver (consisting both source and sink driver) across the chip. The X-axis is normalized with respect to the overall average of all drivers' LSB current (I_{AG}). (b) Post-calibration INL of all drivers based on the overall average LSB current.

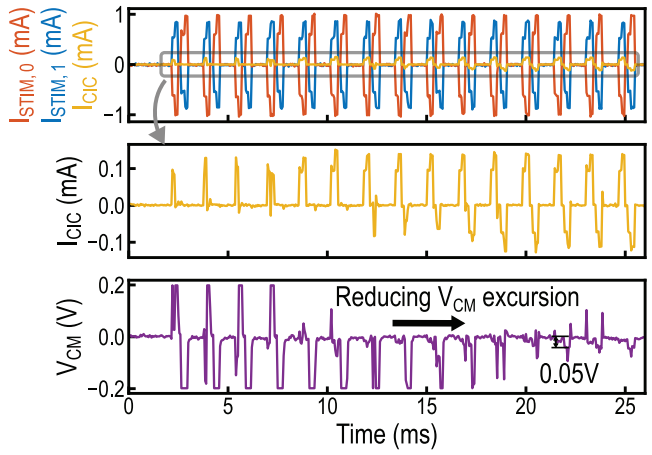

Fig. 14. Measurement results for CIC techniques in action.

from the average LSB current, denoted I_{AG}, is measured to be 15.4%. We employ a calibration technique to address this variation across all 46 channels and improve the accuracy of the stimulation current. This calibration process involves sweeping the scan settings programmed by an FPGA to cover the entire range of DAC codes. A calibration table is generated based on the measured output DC currents. The post-calibration integral non-linearity (INL) of the stimulation drivers with respect to I_{AG} is depicted in Fig. 13(b). The INL is observed to be bound within $+/-1.5$ LSB except a few outliers. As a result of the calibration, the allowable DAC settings are restricted to 84, reducing the effective number of bits to 6.4.

Transient waveforms corresponding to the proposed imbalance compensation techniques are shown in Fig. 14, for an arbitrarily shaped two-channel stimulation. In this experiment,

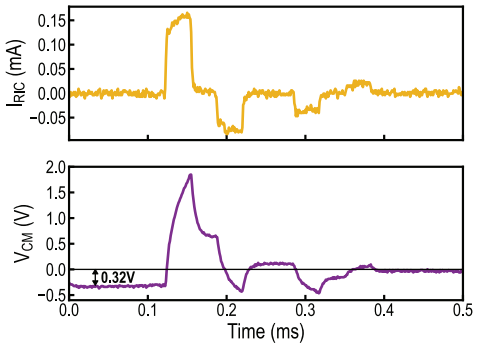

Fig. 15. Measurement results for RIC technique in action.

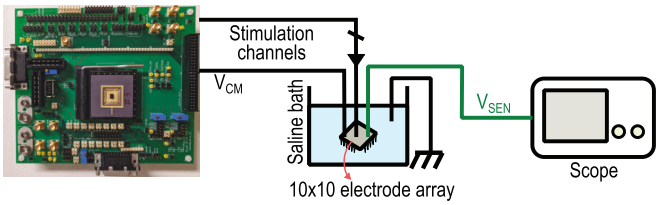

Fig. 16. Test setup for measurements in saline bath.

the power supplies of the stimulator are floated, and the "tissue" side of all electrodes is connected to a single node representing the pseudo-brain. The pseudo-brain node is connected to the earth ground through a 10 MΩ discrete resistor.

An imbalance between the source and sink current is introduced for demonstration. When CIC enabled, current imbalance is compensated for each time slice using I_{CIC}, causing the residual voltage at the CM anchor electrode goes below 50 mV (Fig. 14). Since the current through the CIC and V_{CM} electrode is not charge neutral, passive regeneration was enabled after each stimulation cycle to discharge the residual voltage.

In Fig. 15, the residual voltage on the electrode capacitance is intentionally increased by reducing the duration of passive regeneration for demonstration purposes. Once the V_{CM} potential reaches −0.32 V, the RIC activates and, at the end, the V_{CM} residue goes below 50 mV.

The average power consumption of the digital circuit during typical low-frequency (10 - 100 Hz) biphasic stimulation is measured to be less than 20 μW/channel.

B. Measurements in Saline Bath

The ability of the proposed architecture to suppress stimulation artifacts and deliver localized stimulation is evaluated through experiments in a saline bath. The test setup is illustrated in Fig. 16. The dimension of the electrode tip is 0.5 mm $\times$0.3 mm and they are arranged in a 10 $\times$ 10 grid at at a pitch of 2.54 mm. One of the corner electrodes in the array was chosen as the anchor. A separate wire is used to connect the solution to the earth-ground.

1) Stimulation Artifact Reduction: A 200 μA bipolar, biphasic stimulation (post-calibration) over 200 μs duration is applied to the saline bath using an arbitrarily chosen source and sink pair (with relative distance of 4 electrodes). The voltage measurements of interest are V_{CM}, measured relative to earth- ground and the voltage at a nearby recording site

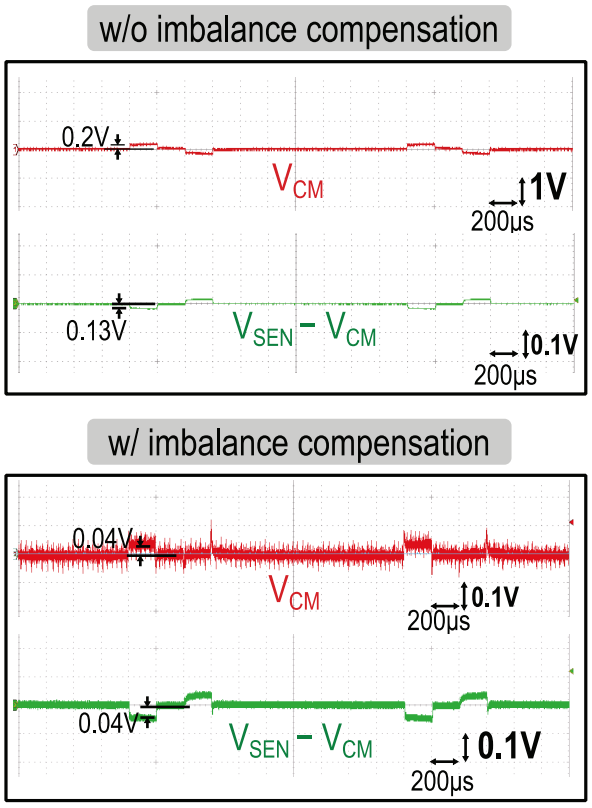

Fig. 17. Potential (with relative to V_{CM}) seen at a recording electrode site in the saline bath. After CIC is applied with the anchor electrode providing a CM connection, the artifact is significantly reduced.

(V_{SEN}) with respect to V_{CM}. The latter represents the voltage seen by a recording front-end whose ground supply, V_{SSR}, is shared with V_{CM}.

By introducing an electrode to anchor the tissue/saline potential to V_{CM}, the V_{CM} excursion is limited to $I_X Z_E$ – approximately 200 mV in this experiment. The artifact amplitude seen by the recording system also reduces to 130 mV. The application of the imbalance compensation further reduces this imbalance-induced CM artifact to less than 50 mV.

2) Spatially Targeted Stimulation: To demonstrate the capability of delivering localized stimulation, we have chosen four sites between electrodes where fictitious axons are located and their positions are marked in Fig. 18. They are also assumed to lie along the X-axis without loss of generality.

It is essential to achieve good confidence between the emulated 3D volume resistive mesh and the saline before computing the required stimulus currents. Because saline is an isotropic conductive medium, resistors can be used to model the behavior of this medium. However, it is necessary to determine the size of the mesh volume and the relative scaling between the electrode interface impedance and the mesh resistance. Initially, a few dipole currents are applied to both the SPICE model and the saline bath. The resulting voltages at the other electrode sites are observed and compared. The model parameters, including the mesh size and resistance scaling, are adjusted iteratively until a high correlation confidence exceeding 0.99 is achieved. Using the optimization process described in Section III, the SPICE model is used to compute the I_{STIM} required at each site to achieve the desired localized

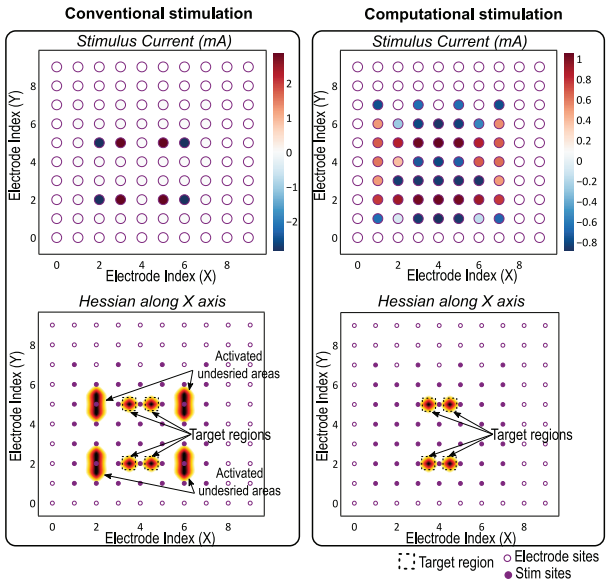

Fig. 18. Activation of four target ROIs in the plane of the electrode tips using computational vector stimulation versus a conventional naive approach. The stimulus currents are normalized with respect to the maximum current in the computational stimulation. Please note that the actual Hessian projections are not shown, instead a certain threshold (required for neural activation) is applied to designate the regions of activation.

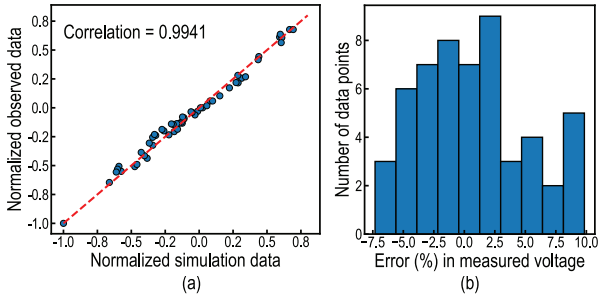

Fig. 19. (a) Trend of normalized voltages observed at non-stimulating sites in simulation versus measurements (b) Histogram of error in the measured voltages.

stimulation. A Python-based convex optimization solver [33] is utilized to solve the optimization problem.

Since it is not feasible to continuously measure the activating function across the entire physical electrode array, a cross-validation approach is adopted. The measurements obtained at the non-stimulating electrode sites are compared with the associated locations in the SPICE simulation. Fig. 19 compares this simulation result and the measurement data. An R^2 correlation score of 0.994 indicates a high level of confidence between the simulations and the measurement data. It is therefore reasonable to conclude that the same locations in saline would achieve neural activation when stimulated using the computed currents.

The activation achieved by the proposed technique is contrasted with a conventional approach in which stimulation currents are applied at nearby electrode sites and their amplitude is increased until the desired activation is observed. From Fig. 18 it is evident that the conventional approach results in a large volume of undesired activation outside of the target ROIs. Because current flows through all channels, the total stimulator power consumption in vector stimulation is 3.1×

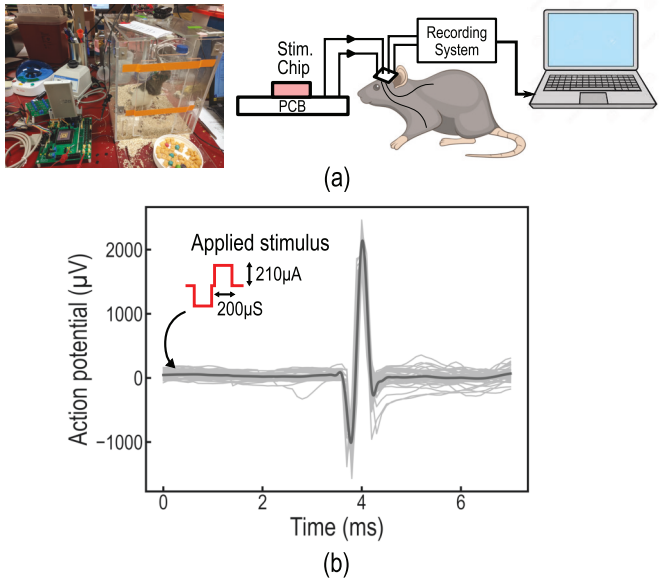

Fig. 20. In vivo measurements: (a) stimulation and recording system interfacing implanted electrodes in the spinal cord and triceps muscle through a headstage (b) evoked action potential in the triceps muscle.

higher than a conventional approach that achieves excitation in the region of interest (among other undesired locations). However, the stimulus current amplitude required by the conventional approach to activate the intended locations is 2.8× higher than that using vector stimulation. The difference in I_{STIM} amplitudes is of significant importance when considering driver and electrode current limits.

C. In Vivo Stimulation

In the in vivo experiment depicted in Fig. 20(a), the designed stimulator is interfaced with implanted electrodes in the cervical spinal cord of a rat through a head-stage. Biphasic stimulus pulses with an amplitude of 210 μA and a width of 200 μs are applied at a frequency of 0.5 Hz. Motor-evoked potentials are recorded in the ipsilateral triceps muscle using an Intan RHD2000 IC mounted on Neurochip [34] and are shown in Fig. 20(b). The recording circuit ground was shared with the stimulator IC to emulate a low complexity closed-loop system [35]. The sensed response is determined to be an evoked potential for three reasons: 1) it was observed only after the stimulus current amplitude crosses a threshold, typical of evoked motor response; 2) the shape is consistent with an action potential; 3) visual twitch of the rat's forelimb. Successful recruitment of neural pathways in the spinal cord demonstrates the suitability of the proposed stimulator with the CM anchor electrode for in vivo experiments.

D. Comparison With State-of-the-Art

Table I provides a summary of specifications along with a comparison with state-of-the-art stimulator circuits [12], [13], [14], [17], [29]. Although the IC in [14] employs 64 stimulators, they are not used for concurrent multichannel stimulation, and therefore do not address issues due to aggregate source-sink imbalance. Additionally, the stimulator in [14] does not support low-latency reconfiguration. Pu et al. [29] demonstrates 2mV residual electrode voltage along with HV compliance. However, the presented charge balancing technique requires measuring the electrode impedance. Our work showcases competitive stimulus current drive and voltage compliance within a compact Si footprint. Notably, in contrast with previous work, this IC marks the first demonstration of spatial localization using a large channel count vector stimulation combined with low-latency delivery of arbitrarily shaped stimuli and output driver nonideality-induced CM artifact suppression by mixed-signal imbalance compensation techniques.

TABLE I
STIMULATOR COMPARISON TABLE

	TBioCAS 2019 [12]	VLSI 2017 [13]	JSSC 2017 [14]	JSSC 2024 [17]	JSSC 2021 [29]	This work
Technology	HV 180nm	HV 180nm	130nm	180nm	HV 180nm	HV 180nm
Stim drivers	8	4	64	10	4	**46**
Max. current	5.1mA	5.04mA	1.35mA	0.25mA	12.75mA	2.5mA
DAC res.	7bit	8bit	8bit	8bit	8bit	7bit
Area/ch(mm^2)	0.79 *	0.11 *	0.0016 *	0.05 *	2 *	0.12
Compliance	9V	12V	3.1V	5V	40V	**26V**
Stim width/res	N.R.	1ms/2μs	N.R.	256μs/1μs	N.R.	**16ms/1μs**
Stim method	Bipolar	Bipolar	Bipolar	Bipolar	Multipolar	**Vector**
Waveform	Arbitrary	Arbitrary	Arbitrary	Biphasic	Biphasic	**Arbitrary**
Targeted stim	No	No	No	No	No	**Yes**
Stim reconfig	No	Yes(4ms)	No	No	No	**Yes(10μs)**
V_{CM} excursion	N.R.	N.R.	N.R.	N.R.	2mV	**< 50mV**

* estimated from die-photo

VI. DISCUSSION

This section explores important considerations and limitations, both of the test-chip and the proposed stimulator system.

A. Targeted Stimulation Away From Electrodes

In this work spatial location is presented for a plane situated just below the electrode array. However, when the objective is to target deeper volumes within the tissue, it becomes necessary to utilize penetrating electrodes or consider alternative objective functions. The proposed approach, which emphasizes net-zero current delivery to minimize stimulation-induced artifacts, can be extended to accommodate other objective functions as required by specific applications.

B. Selection of Basis Current Vectors

Each basis current vector must maintain a net zero current delivery. Apart from this constraint, the selection of the basis current vectors is also determined by the geometry of the electrode array and its ability to generate various combinations of stimulus currents. Depending on the geometry of the electrode array (e.g. planar or cylindrical), the lead arrangement can be rectangular or hexagonal [36], [37]. For a hexagonal electrode arrangement, the basis vectors may consist of adjacent source-sink pairs at Euclidean distance of one electrode.

C. Impact of Electrode Imperfections and Driver Nonlinearity

When employing a recording front-end to detect neural activity using a point electrode while stimulation is ongoing, the amplitude of artifacts is determined by the voltage distribution within the conductive tissue. The presence of imperfections in the electrode can lead to the occurrence of circulating currents among non-stimulating electrodes. If such an electrode is used for recording purposes, it may result in the observation of artifacts with higher amplitudes [38]. These imperfections in the electrode can also exhibit time-dependent variations. This phenomenon has been observed saline bath experiments and that is one of the reasons behind the deviation of recorded voltages from that predicted by SPICE simulations. Another source of this deviation is driver nonlinearity, which alters the electrode current from its intended value. The off-chip calibration required to compensate for variation across stimulation drivers takes several hours, motivating integrated auto-calibration to support channel scalability. Notably, the integrated SRAM in the design can be used to enable parallel auto-calibration.

D. Limitation of the CIC and RIC Techniques

RIC and CIC techniques relax the anchor electrode's impedance requirement for a given CM artifact. Specifically, a 10 μA I-DAC driver LSB and a 10 mV CM excursion limit will allow for an anchor electrode resistance up to 1 kΩ. The number of stimulation cycles between applications of RIC is configured by the user based on the increase in the V_{CM} after each stimulation cycle and the allowed CM limit. Such an approach assumes either the ability to observe V_{CM} to determine this interval count, or a good estimate of the electrode capacitance. However, triggering RIC using closed closed-loop control is more advisable for an implant.

RIC introduces a significantly large compensation current into the tissue to rapidly remove any residual V_{CM}. However, this action introduces a significant artifact that requires the recording to be paused during RIC. In our experiments using typical neural implant electrodes, this "blank-out" duration was found to be brief. (256 μs seen in Fig. 15). User-programmable I_{RIC} pulse amplitude should be maintained below the stimulation threshold. RIC and passive regeneration offer complementary capabilities for residual charge removal on the anchor electrode. RIC enables faster and more controlled charge removal compared to passive regeneration. The latter performs charge balancing across each electrode while RIC balances aggregate charge to suppress V_{CM} buildup.

In the proposed stimulator architecture, the worst-case stimulation-induced artifact is ideally determined by the residual imbalance current after compensation and the anchor electrode impedance. However, in our measurements, the artifact is primarily limited by the ambient noise coupling on the floating system. The dominant contributor to the ambient noise is the 60Hz power-line noise. The PCB traces corresponding to V_{CM} and sensed brain potential were unequal in length since V_{CM} is to be routed along with the stimulator power supplies. Therefore, the ambient noise appears differentially to the feedback comparator and limits our capability to further reduce the V_{CM} excursion.

State-of-the-art AFEs [14], [39], [40] have demonstrated input dynamic range exceeding 100 mV and rapid recovery from artifact pulses. Based on these factors, the observed V_{CM} excursion of 50 mV is within permissible limit. In addition, much smaller trace lengths and footprints anticipated in implanted neural interfaces are expected to minimize the CM artifact amplitude. On-chip power management is anticipated provide further relief. Under these circumstances, we expect worst-case artifacts to be dominated by differences in electrode lead lengths.

E. Per-Channel Charge Balancing

The safety window for residual electrode voltage to prevent electrode and tissue damage is reported in [41] and [42] to be 0.6 V. Per-channel charge balancing is required to keep the electrode voltage below this limit. Existing stimulator circuits have demonstrated various methods for active charge balancing of individual stimulation electrodes: 1) adjusting the pulse duration of anodic phase [17]; 2) applying a series of compensating pulses [28], [29], [43]; 3) adjusting the amplitude of stimulus current [28], [43], [44]. Although these techniques can achieve minimal residual electrode voltage, they do not scale well with the number of channels and often require knowledge of electrode impedance value. Additionally, not all of these works support arbitrary waveform shapes.

Our stimulator relies on passive regeneration (Fig. 10) for individual-electrode charge balancing. Bench measurements show that the residual voltage at the stimulating electrodes remains below 150 mV, well within the safety window. Additionally, calibrating the stimulation currents within 1.5 LSB helps reduce the regeneration current amplitude, ensuring safe operation. This amplitude can be further suppressed by adjusting the anodic phase duration. RIC can be extended to support per-channel charge-balancing based on a comparison of the driver output of each channel with V_{CM}.

VII. Conclusion

This work demonstrates the effectiveness of vector stimulation and integrated memory in enabling spatially localized low-latency adaptive neuromodulation. Computationally guided vector stimulation of a large number of electrodes improves spatial targeting but exacerbates current imbalance. Consequently, the presented circuit architecture, coupled with mixed-signal imbalance compensation techniques, effectively mitigates both current imbalances and their associated CM artifacts. The demonstrated suppression of CM artifacts is substantial, making them compatible with state-of-the-art recording front-ends.

Acknowledgment

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Arindam Mandal (Member, IEEE) received the B.Tech. degree from IIT Kharagpur in 2015, the M.S. degree from the University of Maryland, College Park, in 2018, and the Ph.D. degree from Georgia Institute of Technology in 2024. He was a Junior Research Fellow on the design of dc-dc power converters at IIT Kharagpur till 2016. He is currently a Mixed-Signal Design Engineer at Nvidia Corporation. His research interests include analog and mixed-signal circuit design for biomedical applications.

Dr. Mandal received the Analog Devices Outstanding Student Research Award in 2022 and the Best Student Paper Award at the 2025 IEEE Custom Integrated Circuits Conference (CICC).

Diego L. Peña-Colaiocco (Student Member, IEEE) received the B.Eng. degree (summa cum laude) in electronics engineering from the Universidad Simón Bolívar, Caracas, Venezuela, in 2018, and the M.Sc. degree in electrical engineering and applied mathematics from the University of Washington, Seattle, WA, in 2022. He is currently pursuing the Ph.D. degree in electrical and computer engineering with Georgia Institute of Technology, Atlanta, GA, under the supervision of Prof. Visvesh Sathe. His research focuses on the intersection of circuit design and numerical optimization, with applications in signal processing, wireless communications, and power delivery.

V. Rajesh Pamula (Member, IEEE) received the B.Tech. degree in electrical engineering from IIT (BHU), Varanasi, India, in 2007, and the M.Sc. degree in electrical and electronics engineering from Imperial College London, London, U.K., in 2010.

From 2013 to 2017, he was a Research Assistant with MICAS/ESAT, KU Leuven, Leuven, Belgium, in collaboration with IMEC. He was a Visiting Research Scientist with the Processing Systems Laboratory (PSyLab), University of Washington. He is currently working on biomedical circuit design at Medtronic Inc. His research interests include biomedical circuits, low-power sensor circuit design, and hardware security circuits.

Mr. Pamula was awarded four Gold Medals by IIT (BHU) in 2007. He also received the Analog Devices Outstanding Student Designer Award in 2016.

Steve I. Perlmutter received the B.Sc. degree in biomedical engineering from Brown University, Providence, RI, USA, in 1979, the M.S. degree in biomedical engineering from the University of California at Los Angeles (UCLA), Los Angeles, CA, USA, in 1982, and the Ph.D. degree in physiology and neuroscience from Northwestern University, Evanston, IL, USA, in 1991.

He is currently a Research Professor with the Department of Physiology and Biophysics, University of Washington, Seattle, WA, USA, where he is also a Research Affiliate with Washington National Primate Research Center and a member of the Center for Neurotechnology and the University of Washington Institute for Neuroengineering. His research interests include spinal control of voluntary movements, neural plasticity, and neuroprosthetics. His lab is developing therapies for spinal cord injury and stroke that use activity-dependent, targeted, electrical, and optical stimulation of the nervous systems.

Forrest Pape received the M.S. degree in electrical engineering from Michigan Technological University. He was the Senior Program Manager of Medtronic Inc., where he led the development of electronics platforms for implantable medical devices for 35 years.

Jacques C. Rudell (Senior Member, IEEE) received the B.S. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley (UC Berkeley), Berkeley, CA, USA.

After finishing his Ph.D., he worked for several years as an RF IC Designer at Qualcomm Inc., Santa Clara, CA, USA, and Intel Corporation. In January 2009, he joined the Faculty of the University of Washington, Seattle, WA, USA, where he is currently a Professor of electrical and computer engineering. He is also a member of the Center for Neural Technology (CNT), University of Washington, and the Co-Director of the Center for Design of Analog-Digital Integrated Circuits (CDADIC), University of Washington.

Dr. Rudell received the Demetri Angelakos Memorial Achievement Award while he was a Ph.D. student at UC Berkeley, a citation given to one student per year by the Electrical Engineering and Computer Sciences (EECS) Department. He has twice been a co-recipient of the best paper awards at the IEEE International Solid-State Circuits Conference (ISSCC), the first of which was the 1998 Jack Kilby Award, followed by the 2001 Lewis Winner Award. He received the 2008 ISSCC Best Evening Session Award, and the best student paper awards at the 2011 and 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) and the 2022 IEEE European Solid-State Circuits Conference (ESSCIRC). He was a recipient of the National Science Foundation (NSF) CAREER Award. He served on the technical program committees of the ISSCC from 2003 to 2010 and the RFIC Symposium from 2002 to 2013, where he was the 2013 General Chair. At present, he serves on the technical program committees of the IEEE European Solid-State Circuits Conference (ESSCiRC) and the IEEE Custom Integrated Circuits Conference (CICC). He was an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2009 to 2015.

Visvesh S. Sathe (Senior Member, IEEE) received the B.Tech. degree from IIT Bombay, in 2001, and the M.S. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 2004 and 2007, respectively. He is currently an Associate Professor of electrical and computer engineering at Georgia Institute of Technology where his group, the Processing Systems Laboratory, conducts research in energy-efficient processing, self-optimizing systems, and implantable electronics. He held prior appointments at the University of Washington and Advanced Micro Devices (AMD). As part of the Low-Power Advanced Development Group, AMD, he worked on translating new technologies in the areas of high-performance digital circuits, clocking, and energy-efficient computing into production silicon. He has authored more than 50 articles in leading journals and conferences. He was a recipient of the NSF Career Award in 2019 and the Intel Outstanding Researcher Award in 2020. He served as a Distinguished Lecturer of the Solid-State Circuits Society for 2021–2022. He currently serves on the technical program committees for the Custom Integrated Circuits Conference (CICC) and the International Solid-State Circuits Conference (ISSCC). He currently serves on the IEEE SSCS Webinar Committee to promote student and professional learning, and an Associate Editor for the *Journal of Solid-State Circuits*.