PanTera: RF-SoC Testbed using PYNQ Platform for 147 GHz SDR with 64 Mbps at up to 2 km

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***Abstract*—Sub-terahertz (THz) wireless communication links require low-SWaP (size, weight, and power) software defined radio (SDR) modems to achieve efficient and reliable data transmission. This research presents the design, development, and experimentation of an SDR system operating in the 135-150 GHz frequency range, utilizing simple I/Q modulation techniques such as differential binary phase shift keying (DBPSK). The system integrates advanced components, including Virginia Diodes (VDI) 110-170 GHz compact upconverter (CCU) and compact downconverter (CCD), high-gain lens horn antennas from Anteral (40 dBi), and the Xilinx RF-SoC ZCU-111 for real time DSP. A 500 MHz IF is implemented on RF-SoC with baseband bandwidth 64 MHz and data rate 64 Mbps via DBPSK modulation. For 20 dBm transmit power at 147 GHz, the nearfield SNR was measured to be 55 dB at 1m lens-to-lens separation for a baseband of 64 MHz. Simulation models of propagation predict 64 Mbps is possibly viable at up to 2 km in a point-to-point connection for a BER of $< 10^{-3}$. The SDR was realized on the Xilinx PYNQ platform, offering a user-friendly interface while being adaptable to high data rate applications. This digital design is particularly suited for deployment in scenarios such as vehicle-to-vehicle communication, backhaul networks, and data center level interconnects. The research explored challenges related to synchronization, signal integrity, and environmental sensitivity, which are critical for maintaining reliable communication in a 147 GHz channel. A real-time text messaging application demonstrated correct operation of the PYNQ modem.**

***Index Terms*—Sub-THz, Wireless, RFSoC, PYNQ, SDR**

I. Introduction

For next few years, next-generation wireless networks would be exploiting spectrum bands in the frequency range 3 (FR3) bands (7-24 GHz). However, exponential growth in the computing and telecommunication sectors invariably require exponential growth in wireless capacity [1]. An unprecedented growth in compute capability and dataset size for emerging applications will require wireless transport of information at multiple scales. An impending move to carrier frequencies beyond 100 GHz is inevitable.For instance, communication will occur at various levels: inter-chiplet, inter-package at the circuit board level, between servers within data centers, and between data centers over multi-kilometer distances. Applications exist for next generation low-power wireless networks that require point to point connections, both long range and high capacity, for achieving backhaul between mobile radio systems. Further, new applications are emerging for airborne systems that require extensive communication capabilities. For instance, drone to drone, drone to ground, and drone to satellite systems all require low power wireless data connections at medium range (1-100 km) [2], [3].

II. D-Band Wireless Systems

Access to the radio spectrum is a crucial factor in the development of future medium to long range wireless point- to point communications. It is well known that upper mm-wave bands, typically above 100 GHz, offer abundant spectrum, which can be utilized for gaining high capacity provided sufficient transmit power levels can be engineered to enable the signal to noise ratio (SNR) levels at the receiver that is necessary to achieve capacity across a wide baseband bandwidth of operation [1], [4]. Because the total noise grows as N_oB where N_0 is the noise power spectral density, and B is the baseband bandwidth, any wireless system that exploits wider baseband bandwidths will necessarily scale its total output power as $P_t = kB$ where k is a constant simply to enable the SNR P_t/N_0B constant with increased bandwidth. Generally speaking, the amount of available power at higher frequencies is quite limited due to poor efficiencies and poor linearity of mm-wave power amplifiers. Typical lower mm-wave applications, such as long range space communications in the 10-40 GHz bands that are predominantly based on vacuum tube amplifiers such as travelling wave tubes (TWTs) that offer hundreds of watts of power. However, upper mm-wave (sub-THz) systems, such as emerging D-band systems, are not supported by corresponding vacuum electronics due to the challenges associated with the feature sizes of the TWT devices [5], [6]. In fact, most if not all communications at

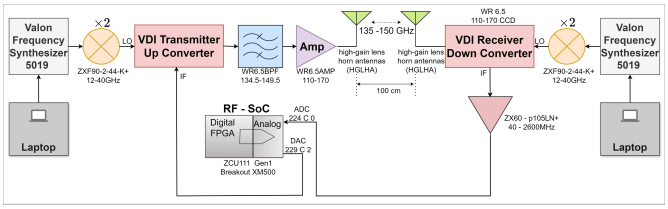

Fig. 1. The block diagram of the D-band communication experimental SDR.

the 100+ GHz bands must use wide bandgap semiconductor power amplifiers for transmission, which in turn brings in to the picture all of the problems associated with energy efficiency and linearity over wide bandwidths of operation. To wit, to make the best use of available PA technologies across D-band (110-170 GHz), we must drive the amplifiers at a bias point which offers best efficiency. That is, at low back off levels, such that we achieve energy efficiency at the cost of linearity. Fortunately, spectral efficiency is not yet a driving factor at 100+ GHz bands which means we can use simple modulation schemes, such as biphase shift keying (BPSK), quadrature phase shift keying (QPSK) and M-array PSK (e.g., 8-PSK) all of which are simple to demodulate, are operate at the peak to average power ratio (PAPR) of unity (i.e., at 0 dB) [7]. The unity PAPR allows PAs to be baised at saturation as the signal being amplified as a constant amplitude level [7].

Engineering an answer to the question of local oscillator synchronization can be difficult for D-band systems because of unstable channel conditions over long distances traversing the atmosphere. A workaround borrowed from the satellite community is to adopt differential modulation schemes. For example, BPSK will be replaced by DBPSK and QPSK will be replaced by DQPSK the common approach found in DVB-S2 type space-earth wireless modems. Replacing phase modulation with differential phase modulation makes the receiver agnostic to absolute phase of the carrier signal and thus allows operation without LO phase synchronization (thus removing a migraine for the system designer).

III. PanTera: FIU's D-Band Test Bed

This work is inspired by Northeastern University's TeraNova [8] which was the first communications SDR at D-band reported in the literature. TeraNova is based on non-real time modulation/demodulation using arbitrary waveform generators at the transmit side, and wideband oscilloscope for signal capture at the receive side. In this D-band SDR, we reduce the baseband bandwidth to about 64 MHz per RF-SoC channel but now facilitate real-time wireless communications using the RF SoC platform configured for communications via the Xilinx PYNQ framework. The modem operates at a digital IF of 500 MHz.

A. Experimental setup

1) Hardware Overview: Fig. 1 shows the radio design for the 135–150 GHz RF front end and DSP back end. The radio frequency (RF) section includes an up converter unit (UCU), power amplifier (PA), and down converter unit (DCU) sourced via Virginia Diodes Incorporated (VDI) [9]. A key feature of the UCU at the transmitting end is that the local oscillator (LO) signal is quadrupled and then added to the intermediate frequency (IF). This results in the RF signal frequency $RF = 4LO + IF$. the LO is maintained within a range of 33.75 GHz to 37.0 GHz. This range is achieved with the help of the Valon 5019 frequency synthesizer. The UCU includes a small signal amplifier followed by a mixer with a conversion loss of 10 dB. The modulated carrier RF is band limited to 135–150 GHz using a filter. The filtered RF signal is amplified by the PA thus providing 20 dBm of RF power at the transmitter lens loaded horn antenna. The DCU at the receiver provides an intermediate frequency (IF) output by subtracting the quadrupled LO from the RF, using the formula $IF = RF–4LO$. The Valon 5019 covers a broad frequency range from 10 MHz to 20 GHz and provides high resolution and accuracy for precise frequency adjustments, essential for advanced communication systems. Its adjustable output power and low phase noise ensure clean and stable frequency outputs.

2) LO Generation: The LO frequency is produced by first generating a signal with the Valon 5019 whose output is then fed into a ZXF90-2-44-K+ frequency multiplier, that operates within the frequency range of 12 GHz to 40 GHz. By doubling the output frequency from the Valon 5019, the ZXF90-2-44-K+ multiplier achieves the desired LO frequency. For instance, if the Valon 5019 outputs a signal at 17.5 GHz, the ZXF90-2-44-K+ will double it to produce a 35 GHz LO. This setup enables precise and high-frequency RF applications, crucial for reliable and high-quality signal performance. Additionally, the wireless transmit and receive interfaces are terminated by D-Band high-gain lens loaded horn antennas (HGLHA) sourced from Anterel, which offer a significant gain of about 40 dBi in the far-field region. These lens antennas are designed to provide directional performance and high signal gain, essential for effective communication and signal clarity in high-frequency RF applications in the D-band. The Fig. 2 illustrates the D-band front-end system.

3) Digital Backend: The digital back-end of the SDR includes a Xilinx RF-SoC chip XCZU28DR-2FFV1517E, which is hosted on the ZCU-111 evaluation board [10]. This high-performance solution, part of the Zynq UltraScale+ RF-SoC family, is designed for advanced RF and mixed-signal applications. The XCZU28DR features four 16-bit analog-to-digital converters (ADCs) and four 16-bit digital-to-analog converters (DACs), capable of operating at speeds up to 4.096 GS/s (giga samples per second) and 6.554 GS/s, respectively. The RF-SoC chip integrates a quad-core ARM Cortex-A53 processor and a dual-core ARM Cortex-R5 processor, along with an FPGA fabric for custom logic implementation. The ZCU-111 evaluation board supports these features by providing RF connectors, high-speed I/O interfaces, and a sophisticated power supply and cooling system, offering a comprehensive platform for development and testing of RF

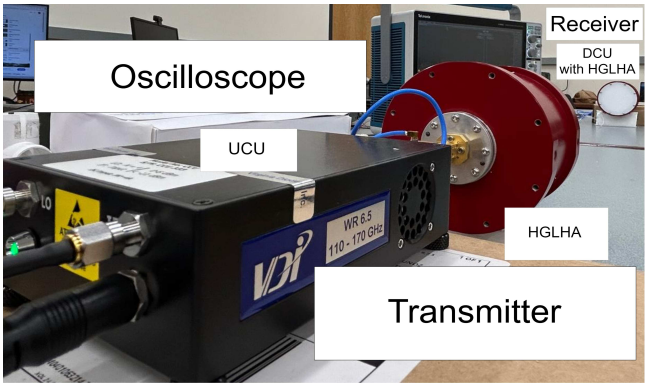

Fig. 2. The test-bed for the RF front end, including the UCU and DCU from VDI, and lens loaded horn antennas with 40 dBi gain.

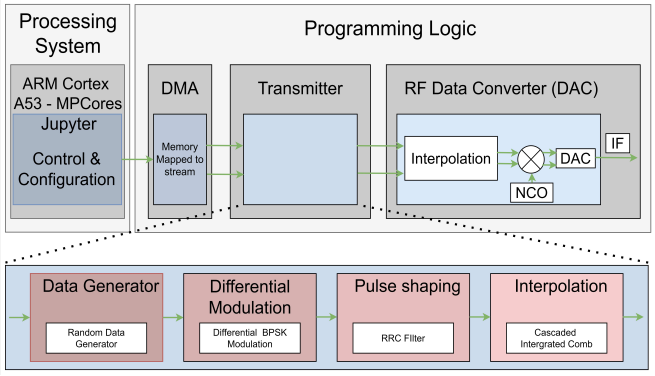

Fig. 3. Overview of the digital design at the transmitter.

and mixed-signal systems.

Jupyter is a platform for controlling the configuration and visualizing data. The RF-SoC runs jupyter on its ARM Cortex A-53 processing system. The transmit and receive functionalities are developed within the programming logic of the RF-SoC. Direct memory access (DMA) intellectual property (IP) serves as a bridge between the processor and the transmitter, which is connected to the RF data converter. The transmitter design includes three key stages: data generation, differential modulation, pulse shaping filter, and interpolation, ensuring efficient digital signal processing and transmission as it is demonstrated in Fig. 3 [11]–[13]. The modulated carrier signal is transmitted through DAC 229 channel 2 to the UCU of VDI at the IF level.

Furthermore, Fig. 4 illustrates the signal reception process. The received signal, sourced from the IF port of the DCU is directed to the RF data converter via ADC 224 channel 0. The signal is processed by the receiver IP, which includes several DSP stages, such as decimation, coarse frequency synchronization, matched filtering, time synchronization, phase synchronization, and frame synchronization. Finally, the processed signal is transferred to the jupyter SDR framework, which runs on the processing system on the RF-SoC via direct memory access (DMA).

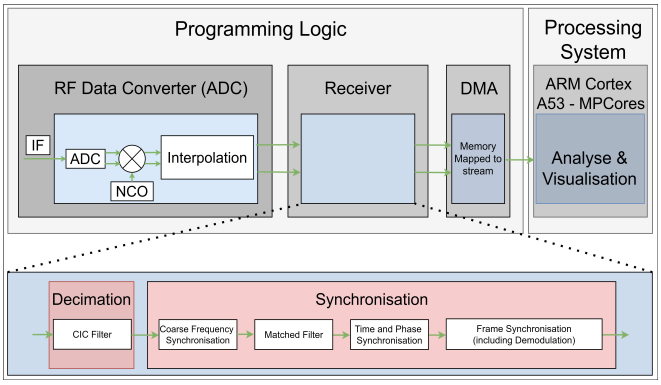

Fig. 4. Overview of the digital design at the receiver.

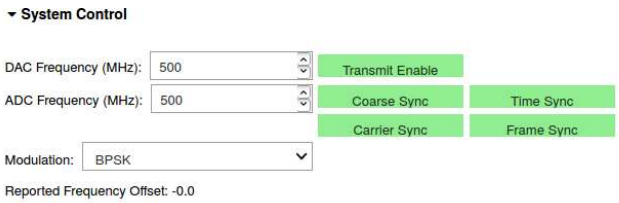

Fig. 5. The radio control interface: manages transmission start/stop, phase timing, and frame synchronization, ensuring precise and synchronized signal handling.

4) Software: The Figs. 5, and 6 illustrate how a user-friendly text messaging interface has been developed using the PYNQ platform to control, and receive signals [11], [13]–[15]. The control interface allows users to manage transmission settings and synchronization options, while the transmitting and receiving interface provides the capability to send characters as desired. This setup ensures an intuitive and accessible way to handle signal processing tasks, making it easier to interact with the system.

B. SDR Configuration

1) Setup: The RF-SoC DAC tile 1 and ADC tile 0 are configured to operate at a clock sample frequency of 409.6 MHz, with the DAC and ADC sampling frequencies set to 1024 MHz. Moreover, the digital mixer related to DAC

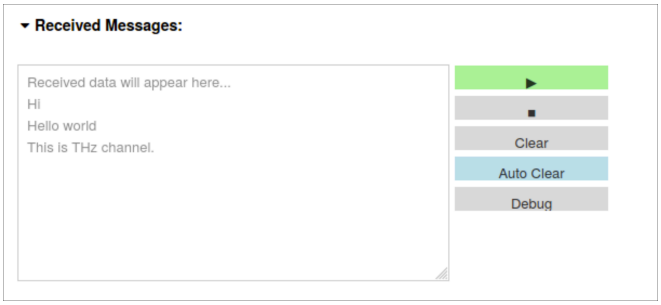

Fig. 6. The receiver interface: a user-friendly interface for managing the receiving process and debugging, ensuring efficient signal control and analysis.

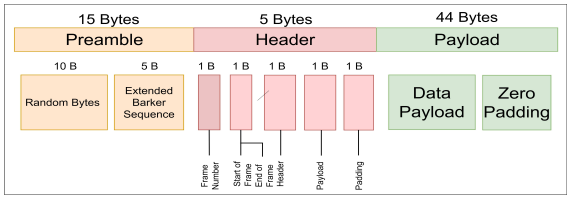

Fig. 7. The data frame structure: the data frame is created by software at the transmitting end in order to synchronize with the start of the payload.

configuration bypasses the coarse mixer stage and directly connects to the fine digital mixer. The "event source" is set to trigger the mixer immediately, allowing the fine mixer to act on the signal as soon as it is generated. The mixer output is scaled by factor 0.7; and it is set to up-convert the signal by 500 MHz which is our chosen IF value, converting a complex input signal to a real valued IF output from the DAC of the RF-SoC. No phase offset is applied. The bandwidth of the IF waveform is 64 MHz; IF outputs are DBPSK modulated signal having 64 Mbps data rate. At the receiver, the mixer is triggered by the RF-SoC tile as specified by the event source. The output of the receive side digital mixer is not scaled, maintaining the original signal amplitude. The fine mixer is set to down-convert the input signal by 500 MHz, converting a real input signal to a complex output. The configuration uses the fine mixer for more accurate frequency adjustments, with no additional phase offset applied. This setup ensures precise frequency down-conversion, crucial for accurately processing RF signals within the ADC block.

2) DATA Frame: To allow the receiver to synchronize with the start of the payload, the data frame is created by PYNQ software at the transmitting end. A data frame typically consists of three major parts: the preamble, header, and payload. Normally, the transmitter sends a known sequence of bits, which the receiver detects using correlation techniques. In this case, a barker sequence is used as the known sequence of bits for frame synchronization. Beyond the barker sequence, important information is embedded within the bit stream or data frame, including:

- Random data to exercise for synchronizing.
- The extended barker sequence or known sequence of bits.
- The frame number.
- A start flag indicating the first frame in the sequence.
- An end flag indicating the last frame in the sequence.
- The data frame length.
- The payload.
- Zero padding.

In this real-time D-band SDR demonstration, a custom data frame is built, as illustrated in Fig. 7, keeping the design simple. Each data frame is 64 bytes long.

IV. 147 GHz Real-Time SDR Experiment

The research is structured into three key stages, each contributing to the overall development and evaluation of the system:

A. Transmitting 500 MHz IF Sine Wave Without Modulation

The first stage involved transmitting an unmodulated 500 MHz sine wave through a D-band system. The signal was evaluated using an oscilloscope to ensure accurate transmission and signal integrity across the system.

B. Transmitting a 500 MHz IF DBPSK signal with 64 Mbps Datarate

In the second stage, a 500 MHz intermediate frequency (IF) differential binary phase shift keying (DBPSK) signal was transmitted through the D-band system, developed using an 8-polyphase implementation in the RFSoC. Phase shifts were introduced after 2, 8, 16, and 32 cycles to assess the impact on data rates. The transmitted signal was evaluated on an oscilloscope to verify performance and accuracy. The IF signal has a bandwidth of 64 MHz centered at 500 MHz and delivers a data rate of 64 Mbps via DBPSK modulation.

C. Digital SDR System with PYNQ RF-SoC Platform

The final stage involved setting up a complete digital transmitting and receiving system, with a focus on ease of integration and use with the python programming platform, facilitated by the Xilinx PYNQ platform. This stage ensures that the system is fully operational, with user-friendly control interfaces for both transmission and reception, making it accessible and functional for further research and application development.

D. Link Budget Design

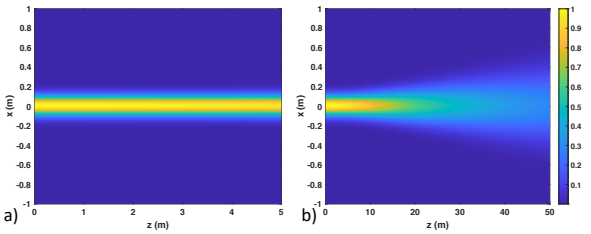

Fig. 8. Beam generated by a 10 cm antenna at 147 GHz carrier: a) The beam is a wide beam of 10 cm thickness with almost no spreading loss for small propagation distance; b) the beam eventually spreads out and can be predicted per Friis path loss over longer distances. Color bar provides normalized intensity pattern.

We employed 40 dBi antennas with an aperture size of 10 cm at transmit and receive ends. The near-field distance is more than 10 m. Thus, when evaluating the link budget, we need to evaluate the link budget not based on the far-field Friis path loss, but on a more generalized power density equation. The Friis path loss comes from far-field assumptions. A fundamental assumption there is that the gain is directly related to the antenna size. This fails in very close distance since otherwise, the gain would continue to increase with an increasing aperture, leading to infinite gain of the antennas, which would result in us deriving more received power than

transmitted – a natural contradiction. Thus, in the near-field, a more generalized link budget is formulated, given as [16]:

$$\frac{P_{Rx}}{P_{Tx}} = \frac{\iint |E_2(x_2, y_2, z)|^2 dS_{Rx}}{\iint |E_1(x_1, y_1, 0)|^2 dS_{Tx}}, \quad (1)$$

where E_1 is the field at the emitter plane (at $z = 0$), E_2 is the field at the receiver plane, and where the integrals are performed over the receiver and transmitter apertures, S_{Rx} and S_{Tx} respectively. We can thus predict the received power more accurately at the receiver. An example of how the generated beam does not have much divergence until we reach longer distances of propagation (greater than 20 m) is shown in Fig. 8. Specifically, we see in Fig. 8a) that the generated beam starts with a beam of size 10 cm thickness, and from both Fig. 8a) and b), we can see that the beam needs to traverse a considerable distance before the beam can be evaluated by the far-field principles. Thus, to evaluate the link budget through (1), we remember that the Anteral horn-lens antennas are producing a Gaussian beam with a beam waist of 5 cm [17], and then we evaluate the expected power accordingly. The other constants, such as cable losses, mixer conversion loss, remain the same. Utilizing the evaluated noise floor with -77 dBW noise power, we derive the link budget, with a 10 dB mixer loss accounted for [18]. The derived link budget is shown in Fig. 9. It is seen that with the present setup, we measured a 55 dB SNR at a 1 m link distance. Interestingly, the measured SNR in the near-field region (more than 10m for a 40 dBi lens loaded horn) is *much smaller* than the signal level predicted by Friis formula which is meant for far-field region [19].

Moreover, since DBPSK can be successfully decoded as long as more than 13 dB SNR is maintained (for BER better than 10^{-3}), we see that multi-km links can be maintained at low latency with current setup if transmit power can be increased to allow receiver SNR of around 13 dB. For 20 dBm transmit power, the distance where far-field SNR is 13 dB falls at $\approx$ 600 m. We see that in the presence of outer space links (vacuum), where absorption losses due to water vapor absorption are completely removed, we should be able to achieve a further smaller improvement of link distance. Further, we have currently considered a noise floor of -77 dBW which reveals an $N_0 = 3.1e-16W/Hz$, where N_0 is the noise power spectral density. However, we can also utilize a much lower N_0 as in our testbed at SUNY Poly and Northeastern University [8]. Thus, we also show in Fig. 9 that we can get up to 2 km link budget if we have the lower N_0 of $10^{-19}W/Hz$. All this indicates that we can potentially further sustain even longer links at the D-band, perhaps several kilometre for the current PanTera setup.

V. Results

In the first experiment, we transmitted a 500 MHz pure sine wave (no modulation) yielded a clear sine wave at the receiver with a signal-to-noise ratio (SNR) of approximately 55 dB at IF. However, the amplitude of the received signal exhibited rapid variations, indicating fluctuations in the received power.

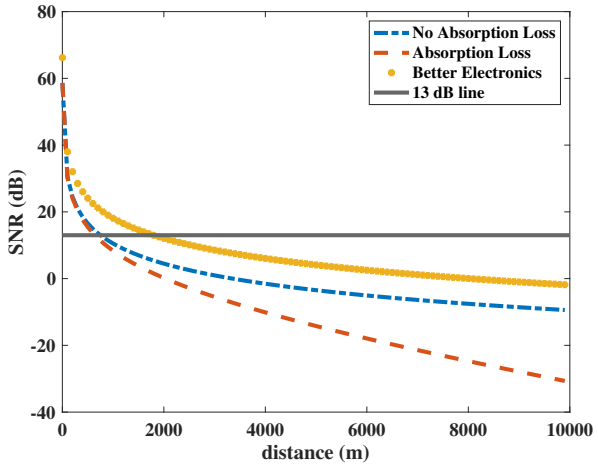

Fig. 9. Calculated SNR with near-field considerations accounted for. We consider three cases: i) all spreading and absorption taken into account; ii) no spreading losses (in space); iii) lower noise floor as in our other testbeds (better technology). More than a few km link can be maintained with DBPSK.

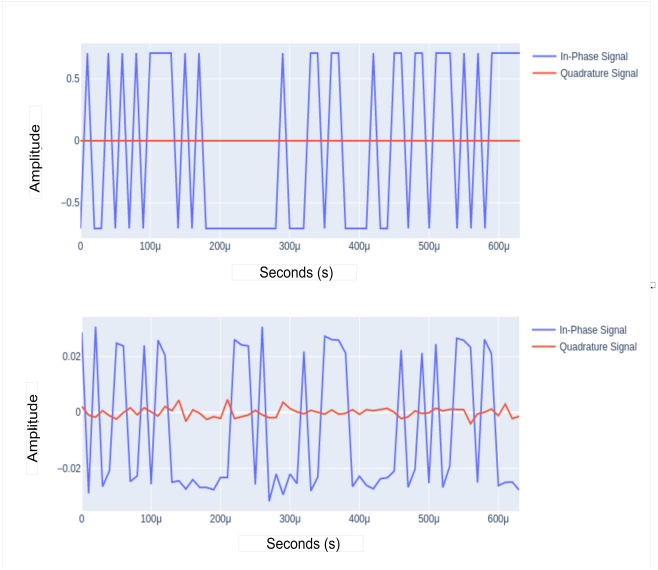

Fig. 10. The time-domain DBPSK modulated signals (64 MHz bandwidth, 64 Mbps data rate, IF at 500 MHz) at the transmitting end and receiving end (55 dB SNR at 1m range).

In the second experiment, a 500 MHz DBPSK signal, generated using an 8-polyphase implementation in the RF-SoC, was transmitted through the D-band system. The DBPSK signal has 64 MHz baseband bandwidth and contains a data stream at 64 Mbps (1 bit/Hz spectral efficiency, PAPR=0 dB i.e., a constant envelope waveform). The experiment lead to observations of different and seemingly random phase shifts occurring after 2, 8, 16, and 32 FPGA clock sample cycles. The sudden phase shifts, such as those occurring after just two FPGA cycles, made it challenging to capture the signal accurately at the receiver.

The third experiment involved integrating digital trans-

mission and reception with the PYNQ platform and the D-band front ends. This setup successfully transmitted text messages like "Hello world" as displayed in Figs. 6 at 64 Mbps rate. Figs. 10 illustrate the time-domain signals at the transmitter and receiver in our experiment. The PYNQ platform is able to lock in and achieve real time data transport. Despite our success, we hasten to note that synchronization issues were observed, leading to occasional errors in character reception, especially when transmitting lengthy data stream. A full bit error rate study has not been performed at the time of writing. These issues underscores the importance of precise synchronization, particularly in the D-band front end, to ensure reliable data transmission and reception. Importantly, the current test bed realization evaluates the 147 GHz using ideal LO matching (i.e., no frequency offset) due to the use of a single RF-SoC board for both transmit and receive functions. We are well aware that this is not the case in real-world communication systems. When the link distance is long, we will need to use two RF-SoC systems at transmit and receive ends and these RF-SoCs do need LO frequency offset cancellation; the challenges associated with LO matching is reserved as future work. Nevertheless, the use of DBPSK modulation simplifies LO matching and synchronization issues.

VI. Conclusion

The digital hardware for the transmit and receive ends was designed to function as a software defined radio (SDR) based on the Xilinx PYNQ platform. The D-band front end utilizes VDI's 110-170 GHz system with a lens horn antenna (LHA-HG-WR06) having 40 dBi gains while the digital back end is built using the RF-SoC ZCU-111. Additionally, working with the D-band wireless channel presents unique challenges due to its high sensitivity to environmental factors, making time/phase, and frame synchronization crucial for maintaining reliable communication. Current version of PanTera achieved a real time data rate of 64 Mbps using 64 MHz of bandwidth at 147.0 GHz carrier, using a DBPSK waveform at 0 dB PAPR. The aim is to push the bandwidth further to 4 GHz per channel, enabling even higher data rates and enhancing overall system capacity. Such innovations at the DSP hardware architecture level are being actively explored. Moreover, we will focus on extending modulation techniques to include M-array phase shift keying (M-PSK) while maintaining 0 dB of PAPR, frequency shift keying (FSK), and differential quadrature phase shift keying (DQPSK) in order to improve the spectral efficiency without sacrificing PAPR or the synchronization advantages of differential modulation. The primary issue is the lack of support for faster data rates from the PYNQ platform which motivates greenfield designs of the SDR components that support high bandwidths, up to 2.5 GHz per RF channel in the RF-SoC platform using multirate DSP methods. Such innovations at the DSP hardware architecture level are being explored as ongoing work.

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