Gate Switching Lifetime of P-Gate GaN HEMT: Circuit Characterization and Generalized Model

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***Abstract*— In converter operations, a major reliability concern of the GaN HEMT with a p-GaN gate (i.e., p-gate GaN HEMT) is the very small gate overvoltage margin. Despite many reliability studies using DC bias and pulse I-V test, the gate reliability under the application-use condition has been seldom reported for p-gate GaN HEMTs. Meanwhile, due to the unique electrostatics of the p-GaN gate, the applicability of the conventional DC lifetime model to p-gate GaN HEMTs is questionable. To address these gaps, this work develops a new circuit method to produce the application-like gate voltage (V_G) stress that consists of a resonant ringing added to an operational DC bias. Using this circuit method, the gate lifetime of commercial p-gate GaN HEMTs is characterized under multiple variables, including the DC bias, peak ringing V_G ($V_{G(PK)}$), ringing pulse width (PW), switching frequency (f_{SW}), and temperature (T). The lifetime is found to show complex relations with the $V_{G(PK)}$, PW and f_{SW}, as well as a positive temperature dependence. Based on the statistical data, a *gate switching lifetime model* is constructed for the first time for p-gate GaN HEMTs. This model comprises the V_G-, f_{SW}-, T-related *Acceleration Functions* and allows one to determine overvoltage stress from an arbitrary V_G waveform and further calculate the gate lifetime. The gate reliability is revealed to be an increasingly significant concern under high f_{SW}, low T, and increased parasitics in the driver loop. The new characterization circuit and switching lifetime model underscore the importance of application-based reliability methodology. The characterization results suggest the need for performing gate qualification for p-gate GaN HEMTs under high-f_{SW}, low-T switching conditions.**[1]

***Index Terms*—GaN, HEMT, gate, spike, overvoltage, switching, reliability, lifetime, model**

I. Introduction

GaN Schottky-type p-gate GaN HEMT (SP-HEMT) has become a popular power device of choice in many device vendors and foundries, and it has been widely used in high-frequency power electronics. However, a major concern in their applications is the small gate voltage (V_G) headroom between the typical driving voltage and the suggested maximum allowable voltage (as low as 1 V [1], [2]). In power converters, the gate-loop inductance can easily induce V_G overshoots during the device turn-on transient due to its resonance with the device gate capacitance. Such overshoot could be increasingly serious at a high switching frequency (f_{SW}). As a result, gate reliability can be the determining factor of the lifetime of GaN SP-HEMTs in practical applications [1]. Thus, a gate lifetime model building on practical switching waveforms is highly desirable for driver design and fault protection of GaN HEMTs in numerous applications.

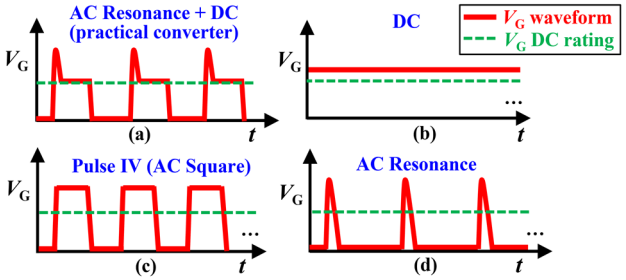

Fig. 1. V_G profiles in (a) practical converters and various reliability tests based on (b) DC bias, (c) pulse I-V, and (d) resonance circuit test.

In practical converters, the device V_G profile usually consists of a resonance-like ringing added to an operational DC bias (Fig. 1(a)). For GaN HEMTs, the operational DC bias is usually 5~6 V, and the peak ringing voltage can be a few volts higher, particularly for those with high current rating and without the monolithically integrated drivers. Also, the ringing is usually fast with an average slew rate (dV_G/dt) of 1~2 V/ns [3].

Unfortunately, the current gate reliability test of GaN HEMTs is primarily based on the DC bias [4], [5], [6], [7], [8], [9],[10] (Fig. 1(b)), which is distinct from the application-use condition. This DC method is inherited from the reliability qualification of Si power transistors with a metal-oxide-semiconductor (MOS) gate, which differs from the p-GaN gate in both composition material and operation physics. Recently, the pulse current-voltage (I-V) test, which generates square-wave AC signals (Fig. 1(c)), has been used to test the gate lifetime [11], [12], [13]. The gate lifetime under pulse I-V tests has been found to depend on f_{SW} and duty cycle [14], suggesting a strong sensitivity of the gate lifetime about the switching parameters. To further mimic the V_G overshoot profile in applications, we recently developed a circuit method to produce the resonant V_G pulses (Fig. 1(d)) [3], [15] and used it to characterize the gate breakdown [15] and lifetime [3], [16] under soft- and hard-switching conditions. Despite a better representation of the resonant overshoot, this circuit method, as well as the pulse I-V test, do not contain the DC operational bias in practical V_G stress [see Fig. 1(a)].

In addition to the test method, another key knowledge gap of the p-GaN gate is the switching lifetime model. In general, a switching lifetime model should be able to determine switching stress and calculate lifetime from the switching waveform [1],

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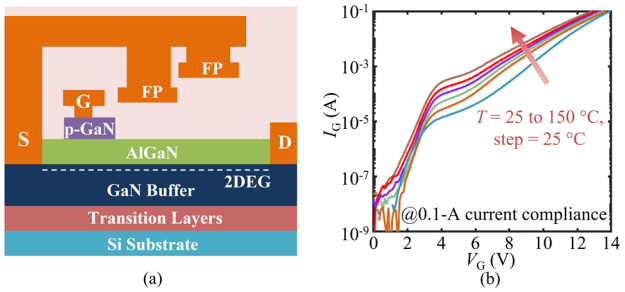
TABLE I
COMPARISON OF MAJOR REPORTS ON THE GATE LIFETIME OF GAN P-GATE HEMTS AND THE PROPOSED MODEL IN THIS WORK.

Ref.	Characterization Method	Voltage Profile	Voltage or Current Acceleration Function	Temperature (°C)	Temperature Acceleration Function	Frequency (Hz)	Frequency Acceleration Function	Combined Switching Lifetime Model
[5]	Constant-volt. stress (CVS)	DC	E Model[1], ${I_G}^{b_{PL}}$ Model[2]	25 ~ 125	Arrhenius Model[3]	N/A	N/A	N/A
[6]	CVS	DC	E Model	25	N/A	N/A	N/A	N/A
[7]	CVS	DC	E Model, $\mathrm{Exp}(\gamma/I_G)$ Model[4]	25 ~ 150	N/A	N/A	N/A	N/A
[8]	CVS	DC	E Model, ${I_G}^{b_{PL}}$ Model[5], $\mathrm{Exp}(1/{I_G}^{1/4})$ Model[6]	25 ~ 150	N/A	N/A	N/A	N/A
[10]	CVS	DC	E Model, Power-law Model[7]	25	N/A	N/A	N/A	N/A
[22]	CVS	DC	$\mathrm{Exp}(1/V_G^{\delta})$ Model[8] $\mathrm{Exp}(\lambda/E_F)$ Model[9] $\mathrm{Exp}(\xi E_F^{1/2})$ Model[10]	-125 ~ 50	Arrhenius Model[11]	N/A	N/A	N/A
[24], [33]	CVS	DC	E Model, $\mathrm{Exp}(\gamma/I_G)$ Model	25 ~ 150	Arrhenius Model	N/A	N/A	N/A
[11]	Pulse-IV	Square AC	Power-law Model	25 ~ 150	N/A[12]	10k ~ 100k	N/A[13]	N/A
[12]	Pulse-IV	Square AC	$\mathrm{Exp}(\gamma/I_G)$ Model[14]	150	N/A	100k ~ 1M	N/A[15]	N/A
[14]	Pulse-IV	Square AC	N/A	150	N/A	100k ~ 3.3M	N/A[15]	N/A
[13]	Pulse-IV	Square AC	N/A	25	N/A	100 ~ 100k	N/A[16]	N/A
[3]	Overvoltage Circuit	Resonance AC	Power-law Model on $V_{G(PK)}$	25 ~ 150	N/A[12]	10k ~ 100k	N/A[13]	N/A
This Work	Overvoltage Circuit	Resonance AC + DC bias	Power-law Model on arbitrary V_G waveform	25 ~ 125	Arrhenius Model	10k ~ 10M	Power-law Model	Quantitative V_G, T, and f_{SW} acceleration functions

[1] Exponential law, i.e., time to failure (TTF) $\propto \exp(\alpha \times V_G)$, where α (<0) is the electric-field acceleration factor.
[2] $TTF \propto {I_G}^{b_{PL}}$, where I_G is the initial gate leakage under stress, and b_{PL} (<0) is the power law exponent.
[3] $TTF \propto \exp[-E_A/(kT)]$, where E_A (>0) is the activation energy of failure, k is the Boltzmann constant.
[4] $TTF \propto \exp(\gamma/I_G)$, where γ (>0) is the gate current acceleration factor.
[5] In this paper, $b_{PL} = -1$.
[6] $TTF \propto \exp(1/{I_G}^{1/4})$.
[7] $TTF \propto {V_G}^{b_{PL}}$, where b_{PL} (<0) is the power law exponent.
[8] $TTF \propto \exp(1/V_G^{\delta})$, where δ (>0) is the power law exponent.
[9] $TTF \propto \exp(\lambda/E_F)$, where E_F is the electric field at the interface of the metal/p-GaN Schottky junction in the gate stack, and λ (>0) is the electric-field acceleration factor.
[10] $TTF \propto \exp(\xi \times E_F^{1/2})$, where ξ (<0) is the electric-field acceleration factor.
[11] In this paper, the E_A varies across different temperatures (e.g., above or below -25 °C), implying corresponding variations in the voltage acceleration functions.
[12] No acceleration function, but qualitatively shows an increasing trend of TTF at higher temperature.
[13] No acceleration function, but qualitatively shows a weak TTF in switching relevance with the frequency ranging from 10 kHz to 100 kHz.
[14] In this paper, $\gamma = 1$.
[15] No acceleration function, but qualitatively shows a decreasing trend of TTF in switching with shorter OFF-state time below 10 µs.
[16] No acceleration function, but qualitatively shows an increasing trend of TTF in switching at higher frequency ranging from 100 Hz to 100 kHz, under switching with a high OFF-state drain bias.

[17]. Recently, switching lifetime models of GaN HEMTs have been reported by the industry and academia for a variety of mission profiles, such as the double-pulse test [18], buck converter [17], [19], AC power cycling [20], and resonant switching [21]. However, these models only capture the voltage and current stressors in the drain-source loop. An application-oriented gate switching lifetime model is still lacking in GaN HEMTs.

Table I summarizes the major gate lifetime models reported for GaN SP-HEMTs in the literature, including the underlying characterization methods and the captured stressors [3], [5], [6], [7], [8], [11], [13], [14], [22]. For the voltage stress, most of these existing models are built on fitting the relation between gate lifetime and the V_G in DC or square-AC tests. Such fitting usually employs one of a few mathematical functions inherited from the Si MOS reliability, such as the power law, E-model, 1/E-model, etc. [6] However, these models have two common limitations when applied to switching lifetime. First, they cannot capture the trajectory of V_G stress in practical waveforms, thereby not taking into account the impacts of the ringing slew rate, pulse width, and duty cycle. The DC lifetime model cannot even capture the lifetime's possible f_{SW} dependence. Second, the lifetime projection is sensitive to the selection of fitting function. For example, based on the same experimental data, the extrapolated maximum V_G for 10-year lifetime can vary considerably using different fitting functions [8], [23].



(a) (b)

Fig. 2. (a) DUT schematics. (b) Static I_G-V_G characteristics at 25 to 150 ºC.

Compared to the Si MOS gate, the p-GaN gate possesses a different degradation physics, making it more difficult to select the appropriate fitting function. The degradation mechanism of the p-GaN gate is reported as the time-dependent Schottky breakdown (TDSB) [3], [11], which is distinct from the time-dependent dielectric breakdown (TDDB) of the MOS gate. A key distinction of TDSB from TDDB is the sensitivity about not only the electric field but also the gate leakage current (I_G) [5], [8], [24]. Utilizing the I_G measured under the DC bias, several I_G-related lifetime models have been proposed, e.g., the $1/I_G$ model and its variants [8]. However, as I_G is usually in the nanoampere to microampere level, it is difficult to measure precisely at the board level in practical converter applications.

In addition to the V_G model, as shown in Table I, there is no report of quantitative models to describe the acceleration effects of the f_{SW} and temperature (T) on the gate lifetime. It is also unclear if the V_G-, f_{SW}-, and T-accelerations are interdependent or can be decoupled mathematically. As a result, there is no combined switching lifetime model reported for the gate reliability in GaN HEMTs.

To address the above gaps and challenges, this work develops a new circuit method that can produce the application-like V_G stress profile and derives, for the first time, a switching lifetime model for p-gate GaN HEMTs based on the circuit test results. The produced V_G profile consists of a resonance ringing added to an operational DC bias ($V_{G(DC)}$), in which the resonance has a controllable peak V_G ($V_{G(PK)}$) and an adjustable pulse width (PW) that can produce a high dV_G/dt comparable to practical applications. This test-vehicle circuit is used to apply accelerated V_G stress with various profiles of the $V_{G(DC)}$, $V_{G(PK)}$ and PW. The derived switching lifetime model can capture the overvoltage stress accumulation along an arbitrary V_G waveform as well as the acceleration effects of the f_{SW} and T. Therefore, such a model can be directly applied to practical switching waveform for lifetime calculation, obviating the need for extrapolation based on a specific function and minimizing the possible errors associated with the fitting function selection.

Note that, while some frequencies and temperatures used in the characterizations of this work are similar to those in [3], all data presented here are characterized using the new circuit method, which produces distinct V_G profiles compared to those in [3]. The remainder of this paper is organized as follows. Section II introduces the new circuit test circuit. Section III presents the test results and the switching lifetime model. Section IV discusses the physics behind the key dependences unveiled in this work. Section V concludes this work.

II. New Circuit Test Vehicle

The device under test (DUT) is a 650V/30A GaN SP-HEMT from a mainstream vendor. Over 300 devices from different batches have been tested under multiple variables including the $V_{G(DC)}$, $V_{G(PK)}$, PW, T, and f_{SW}. To validate the statistical significance, at least 10 devices are tested under each condition for Weibull distribution fitting. Fig. 2(a) shows the schematic of the DUT. Fig. 2(b) shows the DUT's I_G-V_G characteristics at temperatures from 25 to 150 ºC, measured using the Keysight B1505 Power Device Analyzer with a 0.1-A I_G compliance.

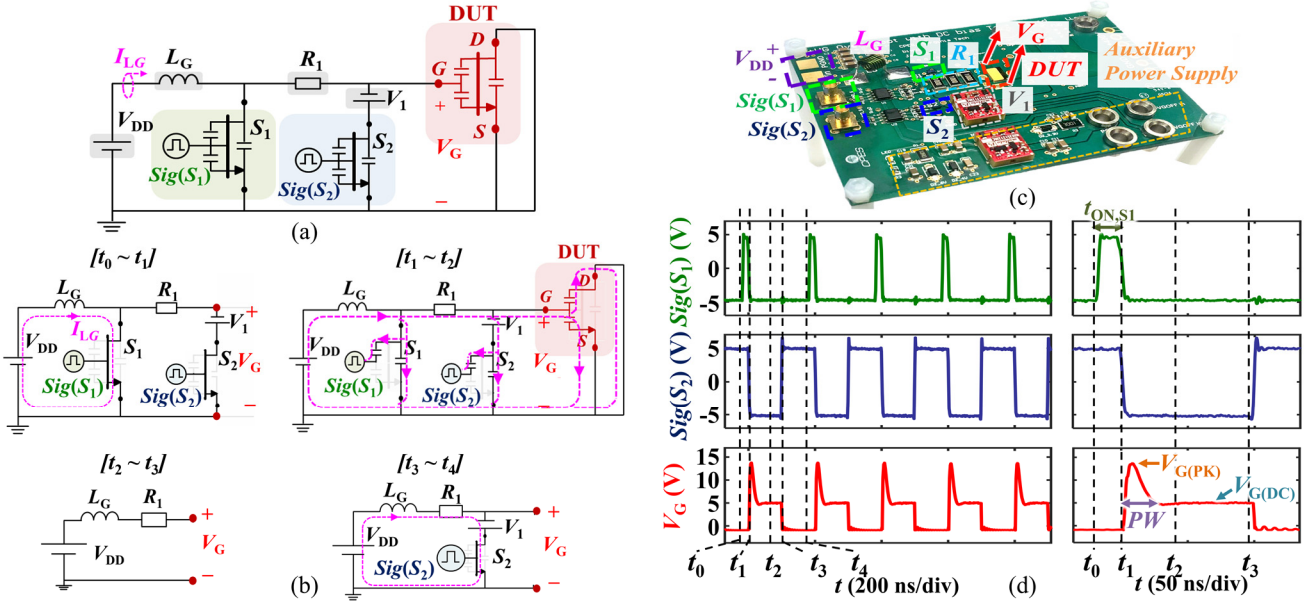


Fig. 3. (a) Schematics of the prototyped gate overvoltage test circuit. (b) Four working stages of the circuit. The current shown in $[t_0 \sim t_1]$ and $[t_3 \sim t_4]$ is conductive current. The current shown in $[t_1 \sim t_2]$ is capacitive current. (c) Photo of the prototyped circuit. (d) Exemplary test waveforms at $V_{G(PK)}$ = 13.5 V and f_{SW} = 5 MHz for (left) repetitive switching cycles and (right) Zoom-in view of the $t_0 \sim t_3$ period in a cycle.

TABLE II
COMPONENTS OF THE PROTOTYPED CIRCUIT

Specification	Symbol	Value or Part #
Gate-loop inductor range	L_G	50 nH ~ 120 nH
Input DC voltage	V_{DD}	5 V
Fast switch 1	S_1	EPC8010
Fast switch 2	S_2	EPC8002
On time of S_1	$t_{ON,S1}$	20 ns ~ 100 ns
On time of S_2	$t_{ON,S2}$	50 ns ~ 50 µs
Isolated DC voltage	V_1	1 V, NXJ2S1212MC
Power resistor	R_1	33 Ω
Pulse width of gate overvoltage	PW	17 ns ~ 40 ns
Peak value of gate overvoltage	$V_{GS(PK)}$	11.5 V ~ 17.5 V
Switching frequency in lifetime test	f_{SW}	10 kHz ~ 10 MHz
Voltage probe	N/A	TPP1000
Current probe	N/A	TCP0030A

Fig. 3(a) and (b) show the schematic and working principles of the proposed circuit, respectively. Similar to the circuit in [3], the V_G overshoot is generated in the DUT's gate-source loop using an inductor L_G to mimic the gate-loop parasitic inductance, a DC voltage source V_{DD} to mimic the source of the surge energy, and a fast switch S_1 to tune the V_G overshoot duration. The principle of this V_G-overvoltage generation is similar to implementing an unclamped inductive switching (UIS) [25], [26] in the gate loop.

Different from [3], the circuit in this work uses the V_{DD} and another isolated DC voltage source V_1 to tune the ON-state and OFF-state operational $V_{G(DC)}$, respectively. Another fast switch S_2 is used to switch ON/OFF the DUT gate, which modulates the duty cycle. A resistor R_1 is used to mimic the gate-loop resistance that damps the ringing.

Table II lists the major components in the prototyped circuit. Fig. 3(c) shows the photo of the prototyped board. As shown in Fig. 3(b), in each cycle, the circuit operation can be divided to four stages:

1) *Stage 1 [t_0 ~ t_1]:* S_1 and S_2 are ON. L_G is charged by V_{DD}. The peak L_G current (I_{LG}) can be tuned by the ON time of S_1 ($t_{ON,S1}$). The DUT's V_G (−0.9 V) is set by $-V_1$ (−1 V) added on the forward voltage drop of S_2 (~0.1 V). The DUT remains OFF.
2) *Stage 2 [t_1 ~ t_2]:* S_1 and S_2 turn OFF at the same time. The energy stored in L_G creates a V_G overshoot on the DUT via a third-order *RLC* resonance (R is R_1, L is L_G, and C can be approximated as the S_1's output capacitance as well as the S_2's output capacitance in parallel with the DUT's input capacitance). This overshoot is quickly damped by R_1 and the DUT's V_G gradually settles to V_{DD}.
3) *Stage 3 [t_2 ~ t_3]:* S_1 and S_2 are both OFF. $V_G = V_{DD}$.
4) *Stage 4 [t_3 ~ t_4]:* S_2 turns ON, and S_1 remains OFF. The DUT's V_G is −0.9 V and the DUT remains OFF.

The PW of V_G overshoot, defined as the period when V_G exceeds V_{DD}, is adjusted by L_G to range from 17 to 40 ns, with the dV_G/dt ranging from 0.7 to 2 V/ns. The $V_{G(PK)}$ is adjusted by $t_{ON,S1}$ ranging from 11.5 to 17.5 V in various tests. The f_{SW} ranges from 100 kHz to 10 MHz, and the duty cycle is kept as 0.5 by adjusting the ON time of S_2 ($t_{ON,S2}$).

The gate switching lifetime is tested under the continuous circuit operation. Similar to [3], we develop a program to detect the waveform deformation, which signifies the DUT failure, and counts the number of switching cycles before the DUT failure. After each circuit test, the DUT is also measured on the curve tracer to validate the failure. Fig. 3(d) shows the exemplar experimental waveforms of the DUT's V_G and the driver signals of S_1 and S_2, under $V_{G(PK)}$ = 13.5 V, $V_{G(DC)} = V_{DD}$ = 5 V, f_{SW} = 5 MHz, and PW = 20 ns. The DUT's case temperature (T_C) is adjusted by a power resistor attached to the case and calibrated by a thermocouple and a thermal camera.

Similar to [3], the circuit in Fig. 3(a) can be also integrated with a inductive load in the power loop to test the gate reliability under hard switching. In this work, all tests are performed under the drain-source grounded (DSG) condition, as the DSG condition has been proved to pose a more severe stress on the gate compared to the hard switching [3], [15]. In this DSG condition, very little self-heating is produced. Hence, the DUT junction temperature is nearly the same as T_C. In this work, we use the measured T_C to represent the DUT temperature in the switching lifetime model.

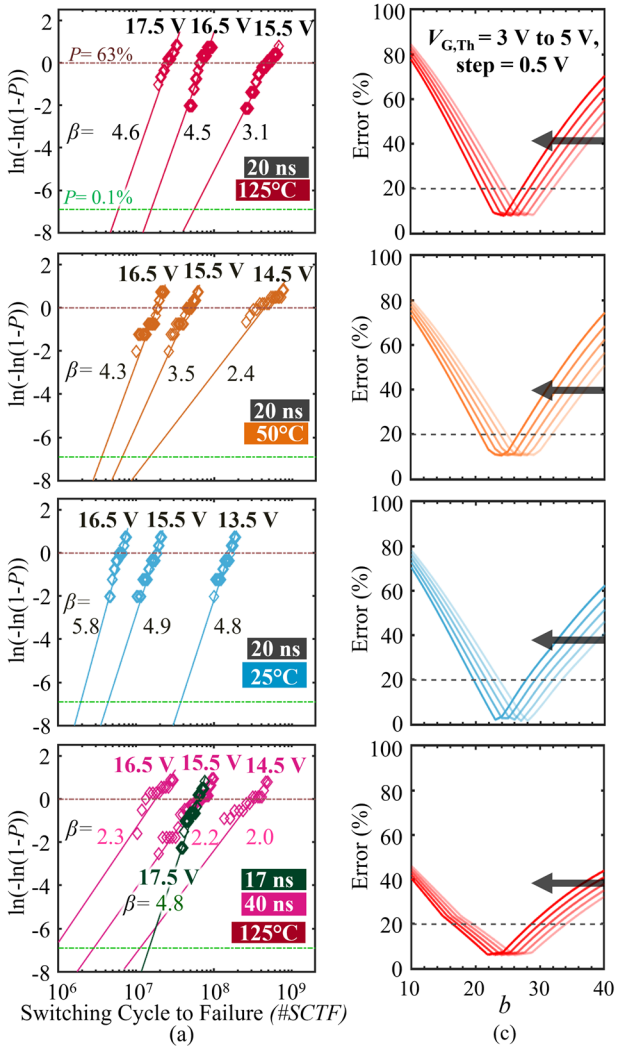
III. SWITCHING LIFETIME MODEL

Recently, Bahl *et al.* [17] demonstrated a generalized approach to construct the switching lifetime model directly utilizing the switching waveform, which can simplify the stressor parametrization. Here we employ the same method, as the switching V_G waveform captures the complexity of the switching transition and directly contains the voltage and slew rate information. In addition to the V_G, the f_{SW} and T are explored as the other two stressors considering the prior findings from DC and pulse I-V tests. From the physics standpoint, the I_G could also be an accelerator, but it is difficult to measure in circuit tests. Due to the strong correlation between the I_G and V_G, the impact of I_G could be lumped into the V_G stress. This assumption is further supported by the I_G-V_G characteristics as shown in Fig. 2(b). In the overvoltage range of interest (V_G >5 V), the I_G-V_G curve exhibits a relatively consistent function at various temperatures, suggesting a consistency of the dominant leakage mechanism.

We then derive the switching lifetime model based on three main assumptions: 1) the gate failure is the wear-out mode, where the wear-out from switching stress accumulates till device failure [18]; 2) when failure is reached under different switching conditions, the cumulative stress ($\Sigma stress$) is a constant for a certain device technology [17]; 3) the acceleration effects by three stressors can be decoupled similar to the drain-loop switching lifetime model of GaN HEMTs developed in [17], [18]. The viability of decoupling three stressors will be checked in the following process of model development. Based on these three assumptions, the cumulative stress to failure ($\Sigma stress$) can be written as

$$\Sigma stress = \Sigma stress^V \times AF^{fsw} \times AF^T = Const \quad (1)$$

where $\Sigma stress^V$ is the stress to failure from V_G acceleration; AF^{fsw} and AF^T are the acceleration functions of the f_{SW} and T.



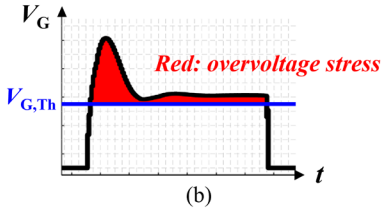


Fig. 4. (a) *#SCTF* data and Weibull distribution of DUTs measured at various $V_{G(PK)}$ at T = 25, 50, and 125 °C (top three), all with PW = 20 ns, as well as at PW = 17 and 40 ns (bottom). (b) Schematics illustration of the gate overvoltage stress in a switching cycle. (c) The mean absolute percentage error (MAPE) of three or four $\Sigma stress^V$ as a function of b and $V_{G,Th}$; the $\Sigma stress^V$ are calculated using experimental data in (a) using equation (2).

The next step is to identify the *Acceleration Function* of each stressor. The chosen model functions should best describe the statistics of experimental data, at the same time reflect the relevant semiconductor physics. The usual functions reported for various stressors such as voltage, current, and temperature include power-law function, exponential function, Arrhenius function, etc. [17].

A. Voltage acceleration

To model the V_G acceleration, a reasonable assumption is the gate lifetimes tested under various $V_{G(PK)}$ should correspond to a similar $\Sigma stress^V$. Fig. 4(a) show the switching-cycle-to-failure (*#SCTF*) data of DUTs measured under overshoots with various $V_{G(PK)}$, T, and PW. For each test condition, the *#SCTF* of 10 DUTs are fitted by Weibull distribution, followed by the extraction of the *#SCTF* with a failure probability (P) at 63% ($\#SCTF_{63\%}$) and with a P at 0.1% ($\#SCTF_{0.1\%}$). The shape parameter β of all Weibull distributions are higher than unity, confirming the wear-out degradation. Note that the specific β range is dependent on sample size and variation. The β range in the current data is consistent with many prior literature on GaN HEMT gate reliability studies [3], [11].

Based on the power-law model widely used for the Si MOS gate [27], we speculate that the $\Sigma stress^V$ function can be written in the form

$$\sum stress^V = \int_0^{T_{SW}} [V_G(t) - V_{G,Th}]^b dt \times \#SCTF \qquad (2)$$

where T_{SW} is a switching cycle period, $V_{G,Th}$ is the V_G threshold above which the gate stress becomes significant, and b is a power law coefficient. The schematic illustration of the gate overvoltage stress in a switching cycle is shown in Fig. 4(b). As $\sum stress^V$ is calculated through an integral traversing the entire V_G waveform, the overvoltage stress produced by every datapoint in the V_G waveform instead of merely the peak value is captured. This ensures the inclusion of overvoltage stresses in both the ringing part and DC part.

To fit the $V_{G,Th}$ and b, the corresponding mean absolute percentage error (MAPE) of the $\sum stress^V$ at various $V_{G(PK)}$ are plotted in Fig. 4(c) for a b range of 10~40 and $V_{G,Th}$ of 3~5 V, for all four groups of experimental data shown in Fig. 4(a). These four groups of experimental data involve the device switching lifetime under three $V_{G(PK)}$ at temperatures of 25 °C, 50 °C, 125 °C and the PW of 17 ns, 20 ns, and 40 ns. For each condition, the corresponding $\sum stress^V$ is calculated based on Eqn. (2), using the $\#SCTF_{63\%}$ and the integral of V_G acceleration per cycle based on the experimental V_G waveform. Such integral covers both the ringing part and the DC part.

As shown in Fig. 4(c), the MAPEs of the four groups of data show a valley in a similar $V_{G,Th}$ and b window for all the T and PW conditions. This further verifies the applicability of the model in (2) to different conditions. A wide window of the b and $V_{G,Th}$ selection is found to satisfy MAPE < 20% in all conditions. Here we select a b of 26 and $V_{G,Th}$ of 4 V. Note that this $V_{G,Th}$ is also physically meaningful, as it is roughly the V_G above which the p-GaN Schottky contact becomes reversely-biased and sees the electric field stress [3], [11].

The relatively large b suggests that the overvoltage stress quickly grows with the V_G and the stress produced in the DC operational bias is minimal in our acceleration tests. To verify this, we test the switching lifetime for a $V_{G(DC)}$ range from 0.5 V to 5 V, under various $V_{G(PK)}$ (in the range of 13.5-17.5 V), f_{SW}, and T. The tested $V_{G(DC)}$ in this range shows minimal impacts on the switching lifetime under all these conditions. As a proof, Fig. 5 plots the Weibull distributions for the gate switching lifetime under two $V_{G(DC)}$: 0.5 V and 5 V, for three groups of conditions, i.e., various $V_{G(PK)}$, T, and f_{SW}. The Weibull

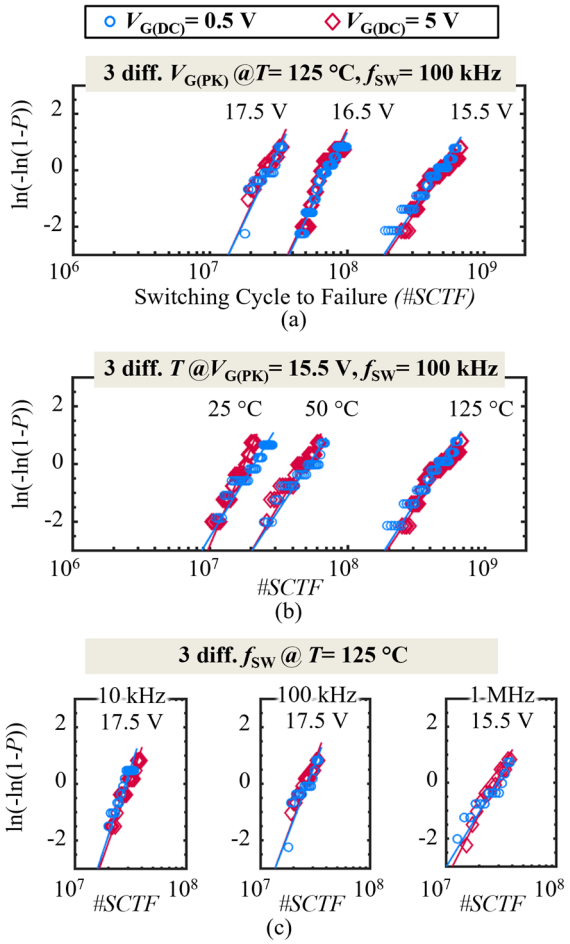


Fig. 5. The Weibull distributions for the gate switching lifetime under $V_{G(DC)}$ of 0.5 V and 5 V for different test conditions including the various (a) $V_{G(PK)}$, (b) T, and (c) f_{SW}. The data under $V_{G(DC)}$ of 0.5 V and 5 V nearly overlap in all switching conditions with various $V_{G(PK)}$, T and f_{SW}.

distributions nearly overlap for the two $V_{G(DC)}$ in all these conditions.

Despite the insignificant $V_{G(DC)}$ stress under test conditions in this work, in theory, as $V_{G(DC)}$ increases and $V_{G(PK)}$ reduces, the $V_{G(DC)}$-induced stress can become comparable to the ringing-induced stress. For example, using the calibrated model in (2) and assuming its applicability to the $V_{G(DC)}$-induced stress, it is projected that under $V_{G(PK)}$ = 10 V ringing stress with a 20-ns PW, the $V_{G(DC)}$-induced stress at $V_{G(DC)}$ > 7.7 V becomes comparable to the ringing-induced stress, for f_{SW} = 1 kHz and 50% duty cycle. Note that the relative magnitude of the $V_{G(DC)}$-induced stress and the ringing-induced stress also depends on the f_{SW} and duty cycle, as they determine the duration of the $V_{G(DC)}$-induced stress. Theoretically speaking, when the $V_{G(DC)}$-induced stress dominates, the circuit-test results may converge to the pulse I-V test results. Further research in this direction will be performed in our future work.

B. Frequency and temperature accelerations

Fig. 6(a) and (b) show the Weibull distributions of the gate lifetime measured at different f_{SW} from 10 kHz up to 5~10 MHz for T of 25 °C and 125 °C, respectively. At both T, the f_{SW} acceleration is found to occur only above a threshold f_{SW} (f_{Th}) at

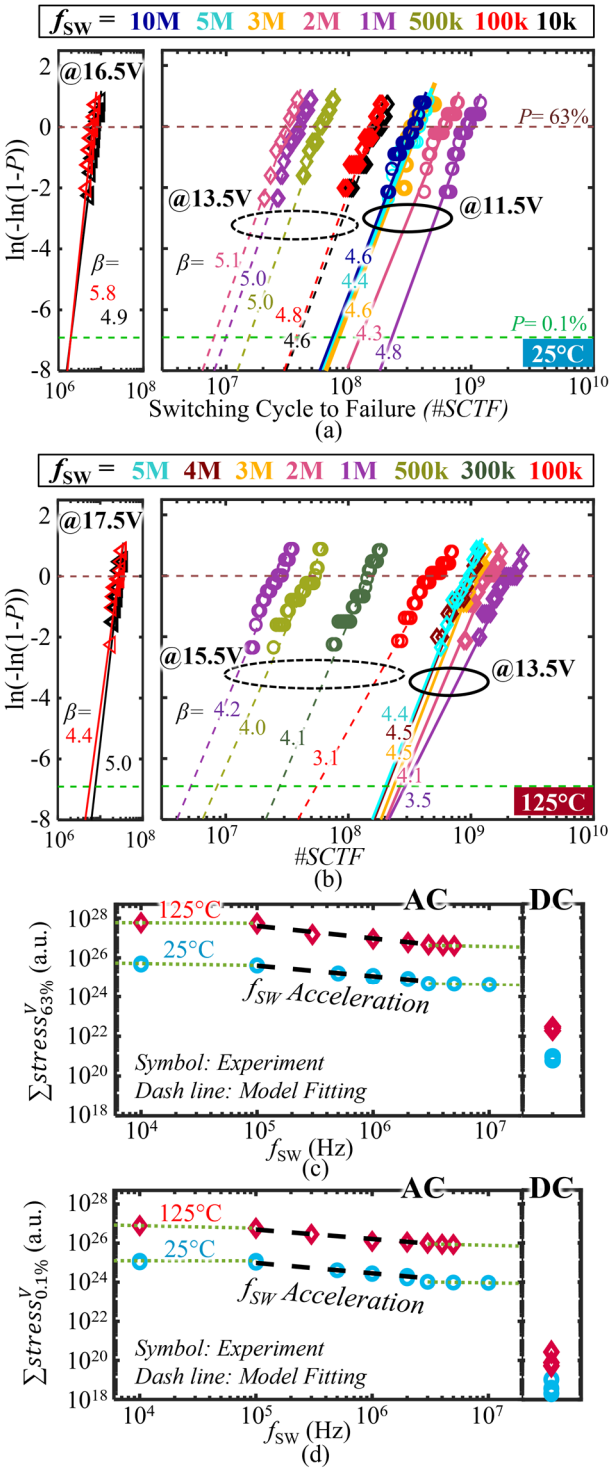


Fig. 6. #*SCTF* data for DUTs measured at various f_{SW}, along with their Weibull distributions at (a) 25 °C and (b) 125 °C. The data for f_{SW} < f_{Th} (~100 kHz) are shown under $V_{G(PK)}$=13.5 V in the right section of (a), as well as under $V_{G(PK)}$=16.5 V and $V_{G(PK)}$=17.5 V in the left sections of (a) and (b), respectively. The data for f_{SW} > f_{Th} are presented in the right section of each figure. The failure boundary $\sum stress^{V}$ versus f_{SW} under the above switching conditions with failure probabilities (P) of (c) 63% and (d) 0.1%. Between f_{Th} and f_{Sat} (~3 MHz), the failure boundary lowers at higher f_{SW} due to f_{SW} acceleration. The $\sum stress^{V}$ with P of 63% and 0.1% derived from the DC test data measured at 9 V, 9.5 V, and 10 V are also included in the plots.

~100 kHz and below a saturation f_{SW} (f_{Sat}) of ~3 MHz. Below the f_{Th}, the #*SCTF* shows nearly no dependence on f_{SW}, which

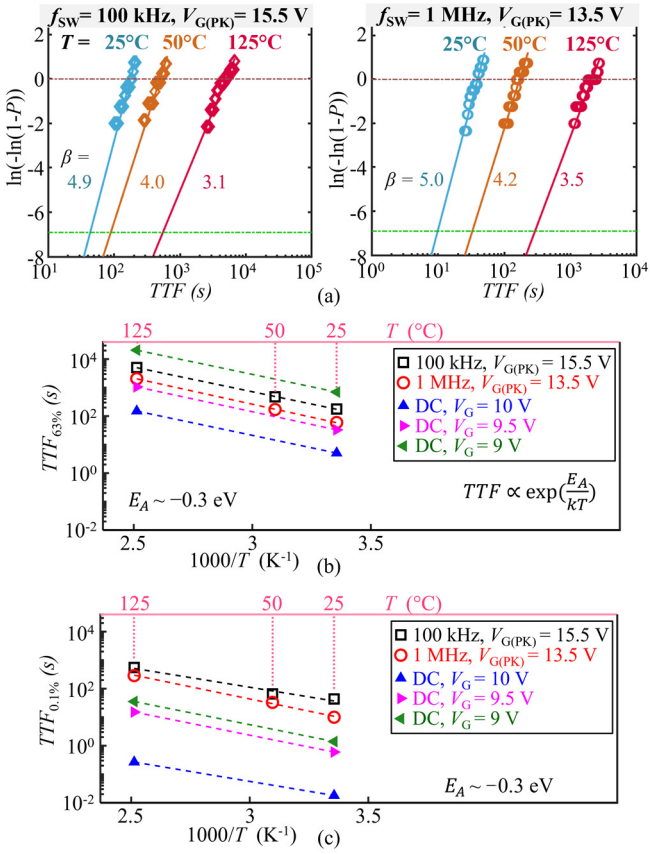


Fig. 7. (a) Time to failure (*TTF*) data and Weibull distributions of DUTs measured at three *T* for f_{SW} at (left) 100 kHz and (right) 1 MHz. Arrhenius fitting of *TTF* versus *T* under the above switching conditions as well as DC stresses from 9 to 10 V (exemplary test waveforms and *TTF* data shown in Fig. 8) with *P* of (b) 63% and (c) 0.1%.

has been validated at three different $V_{G(PK)}$ conditions, i.e., 13.5 V, 16.5 V and 17.5 V, and two different *T*. Above f_{Th}, the *#SCTF* decreases quickly with f_{SW}. This general trend on the f_{SW} acceleration is consistent with a prior report using pulse I-V for reliability test [12]. When f_{SW} reaches above f_{Sat}, the *#SCTF* is found to saturate with the increased f_{SW}, which is reported for the first time for the p-GaN gate.

To present the f_{SW} acceleration in the range between f_{Th} and f_{Sat}, the V_G-related stress-to-failure boundary $\Sigma stress^V$ versus f_{SW} are calculated using equation (2) under both *T*. A lowered $\Sigma stress^V$ at high f_{SW} is a straightforward illustration of the lowered failure boundary due to the f_{SW} acceleration. Based on experimental data, Fig. 6(c) and (d) show the calculated $\Sigma stress^V$ at the *P* of 63% and 0.1% ($\Sigma stress^V_{63\%}$ and $\Sigma stress^V_{0.1\%}$), respectively, as a function of f_{SW} above f_{Th}. The $\Sigma stress^V_{63\%}$ versus f_{SW} relation and $\Sigma stress^V_{0.1\%}$ versus f_{SW} relation can be fitted by a power-law model, giving AF^{fsw}

$$AF^{fsw} = \begin{cases} 1 & (f_{SW} \le f_{Th}) \\ d \cdot {f_{SW}}^{e} & (f_{Th} < f_{SW} < f_{Sat}) \\ d \cdot {f_{Sat}}^{e} & (f_{SW} > f_{Sat}) \end{cases} \quad (3)$$

where *e* is a power-law coefficient fitted to be ~0.6 for $\Sigma stress^V_{63\%}$ and ~0.5 for $\Sigma stress^V_{0.1\%}$, and *d* is a normalization parameter to ensure the continuity of AF^{fsw}. For both

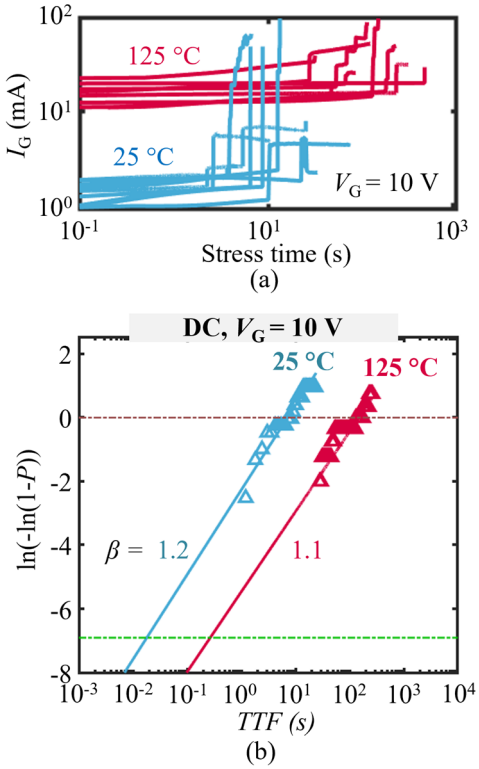


Fig. 8. (a) Gate lifetime characteristics in 10-V DC-bias tests under two different *T*. (a) Test waveforms of I_G evolution. (b) *TTF* data and Weibull distributions under the above test conditions.

$\Sigma stress^V_{63\%}$ and $\Sigma stress^V_{0.1\%}$, the fitted *e* from the 125 °C data and the 25 °C data is nearly identical. This confirms the viability of decoupling the AF^{fsw} and AF^T in (1).

The *T* acceleration of the gate switching lifetime occurs at decreasing *T*. Fig. 7(a) shows the gate lifetime data at three *T* of 25 °C, 50 °C and 125 °C under f_{SW} of 100 kHz and 1 MHz. Here we plot the lifetime data in time-to-failure (*TTF*) instead of the *#SCTF* for a later comparison with the DC test data. Fig. 7(b) shows the Arrhenius plot for these two sets of data, showing a good fit between the *TTF* with the *P* = 63% ($TTF_{63\%}$) versus *T*. As shown in Fig. 7(c), a good Arrhenius fit is also confirmed between the *TTF* with the *P* = 0.1% ($TTF_{0.1\%}$) versus *T*. A consistent activation energy (E_A) of –0.3±0.03 eV is extracted for these two f_{SW} conditions (100 kHz and 1 MHz), further confirming that the AF^{fsw} and AF^T can be decoupled in (1). The AF^T function can be given by

$$AF^T = \exp\left(\frac{-E_A}{kT}\right) \quad (4)$$

where *k* is the Boltzmann constant. It is worth mentioning that the *T* acceleration can be also manifested by the lowered failure boundary $\Sigma stress^V$ at lower *T*, as shown in Fig. 6(c)-(d). Note here the negative E_A is a representation of one or multiple physical processes that result in a positive *T*-dependence of gate lifetime, which will be discussed in more detail in Section IV; it may not correspond to the physical activation of a specific process.

To further confirm the viability to decouple the *T* acceleration from f_{SW}, one can investigate an extreme case with zero f_{SW}. To this end, we test the DC gate lifetime under a constant V_G of 9, 9.5 and 10 V using the B1505 Power Device Analyzer. The evolution of static I_G under a constant V_G of 10

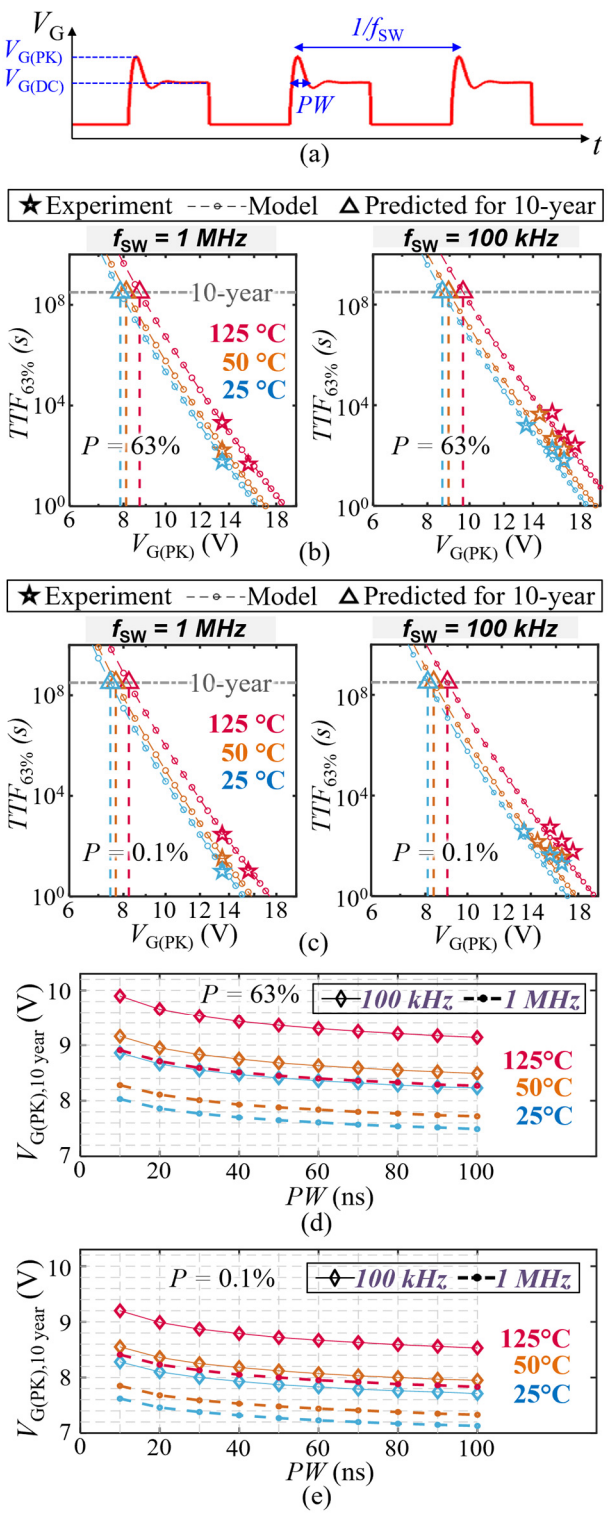


Fig. 9. (a) V_G schematic waveform used to predict the maximum $V_{G(PK)}$ for 10-year lifetime [$V_{G(PK),10year}$] in various switching conditions. The V_G ringing is assumed to be approximately sinusoidal. Projected $V_{G(PK),10year}$ under switching at f_{SW} of (left) 1 MHz and (right) 100 kHz at 20-ns-PW and three T, with P of (b) 63% and (c) 0.1%, respectively. The projected $V_{G(PK),10year}$ as a function of PW, at the above three T and two f_{SW} conditions, with P of (d) 63% and (e) 0.1%, respectively.

V and two T (25 and 125 °C) are plotted in Fig. 8(a). 10 DUTs are tested under each temperature. The $TTF_{63\%}$ and $TTF_{0.1\%}$ data are extracted from the Weibull distributions, as shown in Fig. 8(b). Subsequently, these DC $TTF_{63\%}$ and $TTF_{0.1\%}$ data under three V_G stresses are added to the Arrhenius plots in Fig. 7(b) and (c), respectively. The extracted E_A for the DC lifetime data is consistent with the one for the switching lifetime data at two f_{SW}. This suggests a unified T acceleration under both DC and switching conditions.

In addition, with the TTF data obtained in the DC test (Fig. 8), $\Sigma stress^V_{63\%}$ and $\Sigma stress^V_{0.1\%}$ under the DC condition can be calculated by

$$\Sigma stress^V_{63\%} = (V_G - V_{G,Th})^b \times \#TTF_{63\%} \quad (5)$$

$$\Sigma stress^V_{0.1\%} = (V_G - V_{G,Th})^b \times \#TTF_{0.1\%} \quad (6)$$

The calculated $\Sigma stress^V$ under the DC tests are plotted in Fig. 6(c)-(d) for comparison with that from the switching test. The $\Sigma stress^V_{63\%}$ derived from the data under three V_G are very similar, confirming the applicability of our model to DC stress, i.e., (5) and (6). The $\Sigma stress^V_{0.1\%}$ under three V_G shows some variations mainly due to the possibly larger errors when extrapolating the lifetime at 0.1% failure rate. Nevertheless, it is evident that the DC test cannot capture the acceleration effects from f_{SW}.

Another interesting observation is that the switching-to-failure boundary $\Sigma stress^V$ is in general lower than the DC $\Sigma stress^V$, suggesting an overall longer lifetime under the switching condition than the DC condition. This AC lifetime gain has also been reported for the Si MOS gate very recently, and it was explained by the recombination and suppression of defect generation and the resulted delaying formation of the percolation path [28].

C. *Switching lifetime projection*

From (1)-(4), the DUT's TTF under switching operations can be written as

$$TTF = \frac{\#SCTF}{f_{sw}} = \frac{\Sigma stress}{\int_0^{T_{SW}} [V_G(t) - 4V]^{26} dt \times f_{sw} \times AF^{f_{sw} \times \exp\left(\frac{0.3eV}{kT}\right)}} \quad (7)$$

With the total $\Sigma stress$ measured by one or two accelerated conditions for calibration of fitting parameters, (7) can be used to project the DUT's switching lifetime for an arbitrary V_G waveform at a specific T and f_{SW}. To manifest this capability, we model the TTF versus $V_{G(PK)}$ and further extract the maximum $V_{G(PK)}$ for a 10-year lifetime [$V_{G(PK),10year}$] in various switching conditions. The V_G ringing is assumed to approximately follow a sinusoidal function, as shown in Fig. 9(a). Note that, in this lifetime extraction, there is no need to fit between TTF and $V_{G(PK)}$; all TTF can be directly calculated from the lifetime model.

As shown in Fig. 9(b), the $V_{G(PK),10year}$ is projected to be 7.8 V under a 20-ns-PW and 1-MHz-f_{SW} switching at 25 °C with a P = 63%, and it increases by ~1 V under either a higher T of 125 °C or a lower f_{SW} of 100 kHz. As shown in Fig. 9(c), at the P = 0.1%, the $V_{G(PK),10year}$ decreases to 7.4 V under a 20-ns-PW and 1-MHz-f_{SW} switching at 25 °C.

To manifest the model's superiority in capturing the trajectory of V_G waveform, the $V_{G(PK),10year}$ is modeled at various PW, which represents the varying slew rates and the parasitic

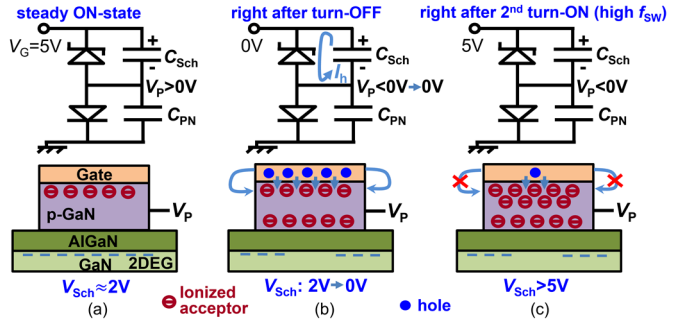


Fig. 10. (Top) equivalent circuit model and (bottom) schematic of charges in the Schottky-type p-GaN gate structure under three working conditions: (a) steady ON-state, (b) right after the turn-OFF, and (c) right after the 2nd turn-ON when V_P has not recovered to zero in the stage (b) (i.e., high-f_{SW} scenario). The arrows in (b) show the hole injection to facilitate the V_p recovery, and such hole injection is blocked at positive V_G in (c) due to the reverse-biased Schottky junction. The voltage across the Schottky junction (V_{Sch}), which is directly proportional to the electric field stress at the Schottky contact, is also marked for three conditions, highlighting the high V_{Sch} and electric field stress in (c).

inductance in the gate loop. As shown in Fig. 9(d)-(e), at the tested T and f_{SW} conditions, when the PW increases from 17 ns to 100 ns, the $V_{G(PK),10year}$ shows a general drop by 0.5 ~ 0.8 V for both P of 63% and 0.1%. When the PW increases to 100 ns, the $V_{G(PK),10year}$ decreases to 7 V at 1-MHz-f_{SW} and 25 °C for a P = 0.1%.

The PW dependence suggests that, in practical applications, the gate lifetime will drop for a higher parasitic inductance in the gate driver loop even under the same $V_{G(PK)}$. Apparently, such an effect cannot be captured in prior gate lifetime models which only comprises a peak V_G value under the DC or AC condition.

The results in this section illustrate that, compared to the conventional models based on DC test and pulse I-V test, our switching lifetime model captures the operational V_G profiles and considers multiple acceleration factors in switching. Moreover, this switching model obviates the need for selecting the fitting functions (e.g., power-law, E-model, 1/E model), which avoids the errors associated with the model selection. Overall, it allows a more accurate projection for a wider variety of application-use conditions.

Finally, it is worth noting that the shape parameter (β) of Weibull distribution shows a variability across the lifetime data collected under different conditions, though all β are higher than unity, which confirms the wear-out degradation. Beyond the inevitable variability introduced in statistical fitting, which could potentially be reduced by increasing the size of dataset for each test condition, we believe the β variability also provides implications on the stress intensity. In general, faster degradation results in a higher β value, as the failures occur more rapidly and are clustered within a specific period. From our test data, a higher β is generally exhibited under low temperature (25 °C), high $V_{G(PK)}$, and high f_{SW}. This trend of β is consistent with the overvoltage, temperature and frequency accelerations of gate failure revealed in this work.

Another interesting observation regarding β is the low value for the DC data (see Fig. 8). This may be explained by an additional degradation mechanism related to the trap/defect assisted leakage current at the gate-edge isolation region as reported by some prior works [8]. Compared to the TDSB in the active gate region, this mechanism features a more stochastic, multiplicative process for defect formation and propagation, as proven by the strong dependence of the gate lifetime on the initial gate leakage current rather than gate voltage [8]. When this process is fitted by the Weibull function, the increased stochasticity can result in a low β, which drags the overall β closer to unity. This lowering effect is similar to the impact of the additional extrinsic degradation factors reported in high-k dielectrics in Si CMOS [29]. The reason why this additional mechanism (and low β) is more pronounced under the DC stress instead of AC stress can be explained by the possible de-trapping in each cycle and the delayed defect/trap generation under the AC switching stress [28]. Future work is needed to uncover the full physical causes for the β difference under DC and AC stress tests.

IV. Physical Mechanism

In this section, we discuss the physical mechanism for the observed V_G, f_{SW} and T acceleration of gate degradation under overvoltage conditions.

The Schottky p-gate can be represented by an anti-series connection of the p-GaN Schottky junction and the GaN PIN junction (Fig. 10). Prior papers have revealed its failure under V_G overshoot to be dominated by the time-dependent Schottky breakdown [3], [11], [15]. Under high V_G, the p-GaN Schottky junction and GaN PIN junction are reverse-biased and forward-biased, respectively. The PIN junction extracts electrons from the two-dimensional electron gas (2DEG) channel into p-GaN, which diffuse to the depleted p-GaN region and get accelerated by the high electric field in the depleted region. These accelerated electrons can bombard the Schottky interface and result in gate failure.

As V_G rises, this TDSB-based gate degradation can be accelerated by two factors. First, more electrons are able to diffuse to the depleted p-GaN region due to the reduced width of the non-depleted region in the p-GaN as the depleted region expands [11]. Fundamentally, this diffusion is viable considering that the electron diffusion length in p-GaN is ~200 nm [30], while the p-GaN layer thickness is usually below ~100 nm [31]. Second, as the electric field in the depleted p-GaN region increases with V_G, the kinetic energy of the electrons bombard the Schottky interface also increases.

In the prior circuit test [3], the gate switching lifetime was measured at f_{SW} < 100 kHz, which does not show the f_{SW} acceleration. The newly found f_{SW} acceleration at higher f_{SW} in this circuit work can be explained by a theory similar to [14]. In the steady ON state, the potential of the non-depleted p-GaN (V_P) is positive, as shown in Fig. 10(a). Right after turn-OFF, due to the depletion charge stored in the Schottky junction, the V_P drops to negative. It then gradually returns to zero via hole injection, as shown in Fig. 10(b). Under high f_{SW}, the OFF-state time is insufficient to complete this process, leaving a negative V_P when the next turn-ON occurs. This further leads to a high bias across the Schottky junction ($V_{Sch} = V_G - V_P$) during the next turn-ON, inducing a higher electric field at the Schottky

junction compared to the low-f_{SW} scenario, as illustrated in Fig. 10(c).

In addition, after the device turn-ON, as the Schottky junction is reverse biased at $V_G > 0$ V, the hole injection and V_P rise are significantly blocked. This effect prolongs the high field stress on the Schottky contact. Such higher and prolonged field stress explains the degraded switching lifetime at high f_{SW}. At very high f_{SW} (e.g., >3 MHz), the very limited charging and discharging of the p-GaN Schottky junction make V_P remain negative in both ON state and OFF state, continuously stressing the p-GaN Schottky contact under a high electric field. In contrast, when the f_{SW} is below a certain threshold (e.g., f_{Th}), there is sufficient time for the V_P to rise to 0 V in the OFF state and reach ~3 V in the ON state, which eliminates the extra field stress on the Schottky contact during the next turn-ON originated from the negative V_P. Overall, the incapability of the V_P to follow the switching V_G at a high f_{SW} can explain the f_{SW} acceleration on the gate lifetime when $f_{SW} > f_{Th}$ and the ultimate saturation at very high f_{SW}.

For the T acceleration of gate lifetime, a new finding of this work is the consistent activation energy under switching and DC stresses. This suggests that the T acceleration of gate lifetime originates from the intrinsic electrostatics of the p-GaN gate and is insensitive to the device operation condition. Hence, the theories developed in prior papers based on DC test [22], [32], [33], [34], [35], pulse I-V [11], and circuit tests [3], [15] can be well leveraged to explain the T acceleration of gate lifetime observed in this circuit work. Throughout the literature, three main mechanisms have been proposed to explain the prolonged gate lifetime at high T in SP-HEMT: (a) the higher I_G [34] and the resulted larger voltage drop in the PIN junction and non-depleted p-GaN, which reduces the voltage drop and electric field in the p-GaN Schottky junction [3], (b) the impact ionization in the p-GaN depletion region, which is known to possess a positive T coefficient and allow the junction region to withstand a higher overvoltage [11], as well as the accompanied thermally-enhanced hole injection [35], which annihilates the hot electrons, and (c) the reduction of electron mean free path in p-GaN at high T [36], which could reduce the number of hot electrons diffuse across the non-depleted p-GaN and reach the depleted p-GaN region. Overall, at high T, all these mechanisms predict either a lower energy or a smaller number of hot electrons that can ultimately bombard the Schottky junction, which is used to explain the prolonged gate lifetime.

The above physical analyses manifest that our switching lifetime model captures the key physics regarding the TDSB degradation. This suggests the applicability of this model to most SP-HEMTs in which TDSB is the dominant degradation mechanism. When applying the model to a different SP-HEMT, although all key relations in the model are expected to retain, some fitting parameters may need to be adjusted due to the design variations of SP-HEMTs (e.g., p-GaN thickness and doping concentration) among different vendors. These fitting parameters could be settled down in relatively few switching tests, allowing device users to quickly tailor the lifetime model for specific devices.

V. Summary

In summary, this work demonstrates a new circuit method for characterizing the gate reliability of p-gate GaN HEMTs in application-use conditions. The produced V_G stress consists of a resonant ringing added to an operational DC bias. A switching lifetime model is established that can derive the accumulated overvoltage stress from an arbitrary V_G waveform in practical converter operations. Such a model can comprehensively capture the complete stress-related information in the V_G waveform including the PW, slew rate, $V_{G(PK)}$ and $V_{G(DC)}$.

The model also quantifies the acceleration effects of f_{SW} and T. The f_{SW} acceleration is found to occur beyond f_{Th} of ~100 kHz and saturates above ~3 MHz; in this range, its impact on gate lifetime can be fitted by a power-law relation. The T acceleration has a negative activation energy (i.e., positive T dependence) and can be fitted by the Arrhenius fitting. In the conditions traversed in this work, the f_{SW} and T accelerations could be largely decoupled, and the T-related activation energy is found to be consistent under switching and DC conditions.

Finally, the switching lifetime model is used to predict the $V_{G(PK),10year}$ under various conditions. This projection can eliminate the possible error produced when selecting a fitting function for TTF~$V_{G(PK)}$ relation in conventional projection methods. Meanwhile, it can capture the impacts of the PW and slew rate, which is inviable using the conventional DC or pulse I-V (square AC) tests. The lower bound of $V_{G(PK),10year}$ is found to generally occur at a higher f_{SW}, lower T, and larger PW. The projected $V_{G(PK),10year}$ at f_{SW} = 1 MHz, PW = 20 ns, and T = 25 °C is ~7.4 V for a P of 0.1%.

These results suggest the conventional DC test is insufficient to project the gate lifetime and underscore the significance of switching reliability method for GaN HEMT gate qualification. In converter applications, particular attention should be placed on device operations at low T and high f_{SW}, and the parasitic inductance in the gate loop should be minimized to reduce the ringing period. Otherwise, gate reliability could become a critical limiter of the switching lifetime of p-gate GaN HEMTs, particularly in low T and high f_{SW} (e.g., MHz) applications. Such risk cannot be addressed by the current gate reliability qualification method such as high-temperature gate breakdown (HTGB) tests.

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