A Low-Power Phase Frequency Detector Using SRAM Cells in 22nm FD-SOI

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***Abstract*—This paper presents the design and performance evaluation of a class of Phase-Frequency Detectors (PFDs) implemented utilizing only logic gates. It is a suitable candidate for applications like All-Digital Phase-Locked Loops (ADPLLs) and Delay-Locked Loops (DLLs). The proposed design is laid out in $65\,\mathrm{nm}$ CMOS and $22\,\mathrm{nm}$ FD-SOI technology and it is validated using post-extracted simulations. According to the results the proposed PFD is blind zone free and exhibits a small dead zone of $\approx 7\,\mathrm{ps}$ and $\approx 9\,\mathrm{ps}$ with a detection range of $\pm 2\pi$ at a frequency of $10\,\mathrm{GHz}$ and $8\,\mathrm{GHz}$ in $22\,\mathrm{nm}$ and $65\,\mathrm{nm}$, respectively. The proposed design has jitter $\approx 448\,\mathrm{fs}$ in $22\,\mathrm{nm}$ and $\approx 1.2\,\mathrm{ps}$ in $65\,\mathrm{nm}$. The proposed PFD occupies a layout area of $115.625\,\mu m^2$ and consumes $7.2\,\mu\mathrm{W}$ in 22nm and the area of the design is $225.7\,\mu m^2$ and consumes $11.03\,\mu\mathrm{W}$ in 65nm.**

***Index Terms*—Phase/Frequency Detector (PFD), Phase-Locked Loop (PLL), Delay-Locked Loop (DLL), Dead-Zone, Blind-Zone.**

I. Introduction

Phase-locked loops (PLLs) are nearly ubiquitous in both computational and communications systems as a means to synthesize accurate clock or local oscillator (LO) frequencies by synchronizing to precise reference frequencies. However, using PLLs as clock generators comes with several challenges. Primarily, process,voltage and temperature (PVT) variations can result in PLL instability due to variations in the loop response. This can be compensated for in the design, and or calibratedat the expense of extra power consumption, complexity and circuit area. Over the past 20 years, there has been a steady push towards more use of all-digital PLLs (ADPLLs), due to their programmability, stability and ease of porting to new process technologies [1, 2]. These circuits rely heavily on digital synthesis and automatic placement and routing for their design and result in a relatively compact system. In systems where a clock does not need to be synthesized (e.g., clock-and-data recovery circuits, multi-phase clock generation, etc.) a delay-locked-loop (DLL) can also be practical [3]. Unlike PLLs which typically require at least a second-order system for practical operation, DLLs can operate as first-order systems, which means they can be made inherently stable.

A critical block that is common to both DLLs and PLLs is the phase-frequency detector (PFD). The PFD outputs a pulse that is proportional to phase differences between the reference signal and a locally generated clock signal. Many different architectures have been proposed for PFDs (e.g., tri-state (TSPD) [4], Alexander (APD) [5], subsampling (SSPD) [6], Bang-Bang (BBPD) [7], multi-bit [8], etc.). APDs and BBPDs have considerably higher power consumption compared to the tri-state PFD. Additionally, the BBPD has limited operating range and also has the possibility of false locking. Although the SSPD offers benefits including low complexity and higher operating speed, high SSPD/CP gain makes full integration difficult [9]. Operation at high frequency also dissipates significant power. An architectural comparison of the choices for PFDs is shown in Table. I.

TABLE I: Architectural comparison of PFDs

Specification	SSPD	BBPD	APD	TSPD	SRPD
Linearity	✓	✓	✓✓	✓✓	✓✓
Speed/Frequency Range	✗✗	✓✓	✗✓	✗✓	✓
Jitter Sensitivity	✓✓	✗	✗✗	✓✓	✓✓
Noise Tolerance	✓	✓	✗✓	✓	✓
Complexity	✓✓	✗✓	✗	✗✗	✓✓
Calibration	✓	✓	✗	✗	✓

✓: Good , ✗✓: Moderate, ✗ : Bad

Latch-based PFDs such as the TSPD [4] are common due to their simplicity, but are subject to a tradeoff in their output responsivity between "blind-" and "dead-" zones. A choice must typically be made to have either a small blind-zone, or a small dead-zone. There is a desire for PFDs that simultaneously achieve small blind- and dead-zones. In this paper, an SRAM cell, which is fundamentally a latch is proposed as the core element in an SRAM-PFD (SRPD) that allows simultaneously achieves blind-zone free and small dead-zone, concurrently. It also enables concurrent low-power and -area design.

This paper is organized as follows. In Section II, a brief background discussion on blind- and dead-zones in the latch-based TSPD is provided. This is followed by details of the proposed SRPD and its mechanism in Section III. Simulation results are provided in Section IV. Finally, conclusions are outlined in Section V.

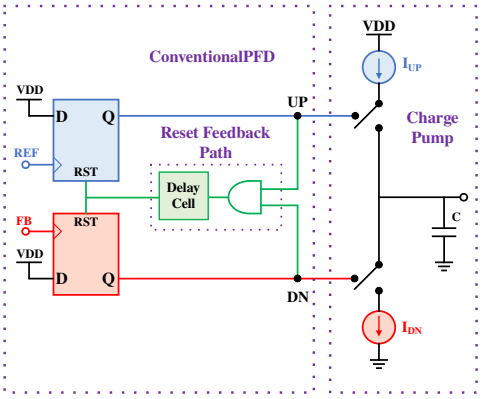


Fig. 1: Schematic of a conventional, tri-state PFD with a charge pump.

II. Background

Fig. 1 illustrates a conventional tri-state PFD [10]. It consists of two D-flip-flops (DFFs) and a reset mechanism. A rising edge on the REF or FB input results in a pulse at UP or DN, respectively. To prevent both current sources from being enabled simultaneously, a reset mechanism detects a scenario where both UP and DN are caused to be high simultaneously and resets the DFFs to impede this state. A primary bottleneck in this type of PFD is the finite delay in the reset path that can briefly allow the UP and DN lines to be high simultaneously due to the delay in the logic gates that comprise the reset path. This introduces the concept of two primary challenges in PFD design: the "dead zone" and "blind zone".

The effects of the blind zone on the detection range of any latch-based PFD are depicted in Fig. 2(a). Φ is the phase difference between the REF and FB signals. Ideally, the PFD would have a constant, linear slope through the full range ($\Phi = 4\pi$) representing the FB signal leading the REF by ($\Phi = -2\pi$) to the FB signal lagging the REF ($\Phi = 2\pi$). However, due to the delay in the reset mechanism, the detection range of the PFD is limited to $4\pi - 2\Delta$ where Δ is the blind zone duration and is given by:

$$\Delta = 2\pi \times \frac{T_{reset}}{T_{REF}} \tag{1}$$

T_{REF} and T_{reset} are the period of REF period and the reset pulse length, respectively. Not only does the blind zone limit the phase comparison range, but it also slows down the locking process [11]. One way to mitigate this, subject to PVT variation is employing a programmable delay cell at the input of the PFD [12].

In contrast to the blind zone, a dead zone occurs when the phase difference between REF and FB is ≈ 0, shown in Fig. 2(b). In this state, the parasitic capacitances of the internal nodes of the PFD result in delays that cause the PFD to not be able to output signals correctly (e.g., pulses are delayed too much or are swallowed); hence, both UP and DN are simultaneously driven to logical highs. In an ideal case, this means that I_{UP} and I_{DN} are turned on simultaneously and no

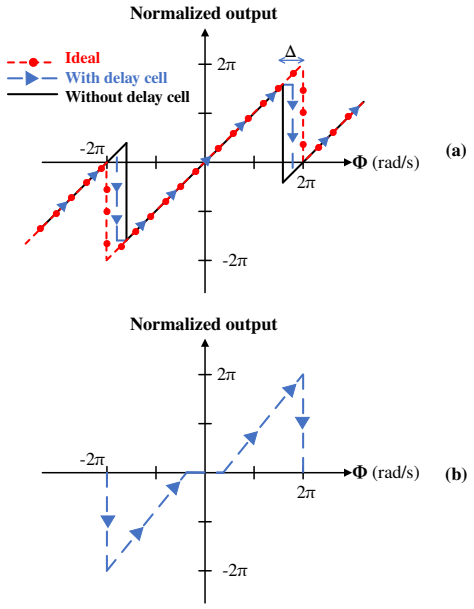


Fig. 2: Non-ideal characteristic of latch-based PFDs: (top) blind Zone (bottom) dead zone

charge contribution can be made to the loop filter capacitor, C. This results in a region where the PFD has no gain and hence during this interval, the loop may become briefly unlocked, resulting in glitches that induce spurious signals and noise.

It should be noted that most PFDs have either a blind-zone, or a dead-zone, or both. In the following section, a proposed PFD, consisting only of logic gates and an SRAM cell, that is inherently blind-zone free and has a short dead-zone is described.

III. Proposed Circuit

The schematic of the proposed SRAM-based PFD (SRAM-PFD) is shown in Fig. 3. The SRAM-PFD has a symmetric structure and it is implemented based on complementary logic circuits. It consists of a 6T-SRAM which acts as the core of PFD, a detection phase difference window (DPDW), which is formed by two rising edge detectors, and UP and DN generator blocks. The UP/DN generators consist of a pull-up network, M5-M6, an auxiliary pull-up network, M7-M8, and a pull-down network, M3 and M4. The phase difference between the reference signal (REF) and the feedback signal (FB) is detected and results in a time window corresponding to their phase difference. During this window, the polarity of the latch in the SRAM cell changes and the UP or DN signal is generated depending on whether REF is leading or lagging FB. The UP/DN signals are then input to a charge-pump circuit, similar to the one shown in Fig. 1.

Representative waveforms, for a case where FB is leading REF, detail the operation of the SRAM-PFD as shown in Fig.4. In this case, the DPDW outputs an active-low FB_rise pulse to the gate of M1, connecting node Q to VDD. The latching

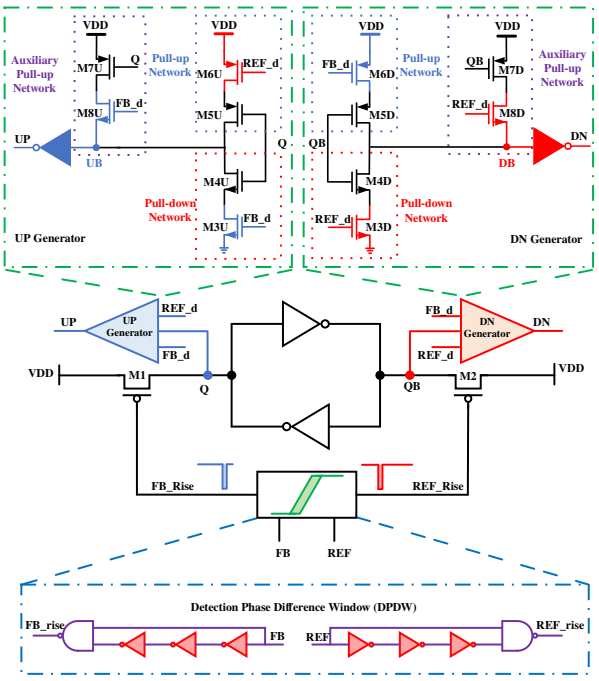


Fig. 3: Schematic of proposed SRAM-based PFD.

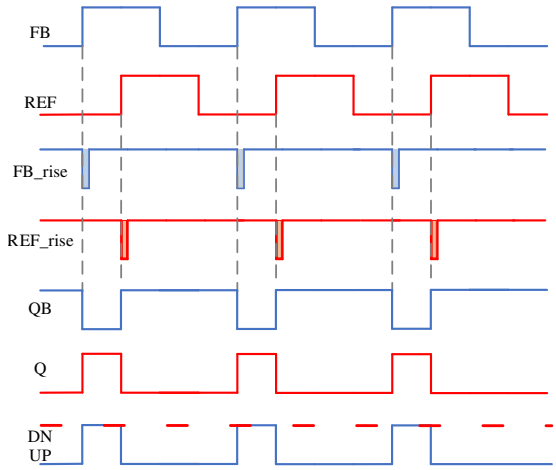


Fig. 4: Waveform of the proposed SRAM-based PFD.

action of the SRAM cell pulls QB down to the ground. When the rising edge of the REF signal occurs, a similar action happens where QB is connected to VDD and Q is latched to GND by the SRAM. During the window where Q has switched to VDD, the pull-down network consisting of M3U and M4U is enabled, and is inverted to cause UP to output a logic high that is gated when the REF_rise signal is activated. Once Q is switched to logic low, and neither of the pull-up nor pull-down networks are active, to maintain the state, the auxiliary pull-up network latches the outputs correctly. A similar process occurs when REF is leading FB. The FB and REF signals are delayed by 2 minimum inverters, $\mathrm{Ref_d}$ and $\mathrm{FB_d}$, in the UP and DN generator block to remove the blind-zone.

The output pulse width of the proposed PFD is estimated as:

$$T_{UP/DN} = T_{delay} + T_{\phi} \tag{2}$$

Where T_{delay} and T_{ϕ} represent the pulse width of the pulse generated by DPDW and the phase difference of the FB and REF signal, respectively.

To estimate the jitter performance if used in a system, the output jitter impact in a DLL can be estimated. The output jitter at the $\mathrm{X^{th}}$ delay cell, $\sigma^2(\Delta t_X)$, due only to the PFD jitter, Δt^2_{PFD}, is given by the following [13]:

$$\sigma^2(\Delta t_X) = \left| \frac{(\frac{X}{N})^2(\frac{I_{CP} \times K_{VCDL}}{C_{LF}})}{-2 + (\frac{I_{CP} \times K_{VCDL}}{C_{LF}})} \times \sigma^2(\Delta t^2_{PFD}) \right|, \tag{3}$$

where X is the $\mathrm{X^{th}}$ cell, N is the total number of delay cells in the DLL, and I_{CP} is the charge pump current. $\mathrm{K_{VCDL}}$ presents the gain of the Voltage Controlled Delay Line(VCDL) and $\mathrm{C_{LF}}$ is the capacitance in the loop filter. From (3), this can be interpreted that lower $\mathrm{I_{CP}}$ results in lower jitter. It can be seen that the jitter of the DLL is linearly dependent on the PFD jitter. As the jitter performance of the proposed SRAM-PFD is similar to other latch-based PFDs, the jitter performance in larger systems is expected to be similar to those results.

The post-extraction simulation results of the proposed PFD are highlighted in detail in IV.

IV. Post-Extracted Simulation Results

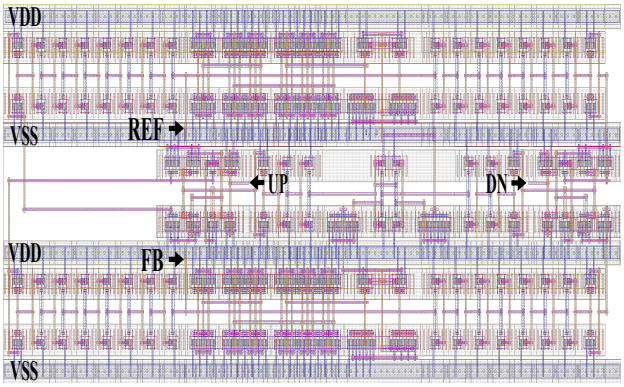


Fig. 5: Layout of the SRAM-PFD in 22nm FD-SOI.

The SRAM-PFD (Fig. 5) is laid out in a 22nm FD-SOI process and it occupies $115.625\mu m^2$. It is extracted using foundry provided rules with Mentor Graphics Calibre software. The extracted layout is then simulated over process corners to validate its performance. When operating from a 0.9V supply, the power consumption of the SRAM-PFD, $7.2\mu W$ while operating at 125MHz. The dead zone, which corresponds with the minimum detectable range, T_{ϕ} for the SRAM-PFD is plotted across temperature and supply voltage in Fig. 6 and 7, respectively, for several process corners. As can be seen, the maximum dead-zone in the nominal corner is

TABLE II: Performance Comparison to the State-of-The-Art

Specification	This Work	This Work	[14]:PFD 1	[14]:PFD 2	[15]	[16]	[17]
Technology (nm)	**22 FDSOI**	**65 CMOS**	65 CMOS	65 CMOS	130 CMOS	130 BiCMOS	90 CMOS
Power supply (V)	**0.9**	**1.2**	1.2	1.2	1.2	1.2	1.8
Dead zone (ps)	**7**	**9**	Free	2.5	25	-	15
Blind zone (ps)	**Free**	**Free**	29	9	-	0.75	Free
Detection range	$\pm 2\pi$	$\pm 2\pi$	$\pm 2\pi$	$\pm 2\pi$	$\pm 2\pi$	$\pm 2\pi$	$\pm 2\pi$
Max Frequency (GHz)	**10**	**8**	7	16.6	4.1	2.5	1
DC Power (μW)	**7.2@125MHz**	**11.03@125MHZ**	29.5@125MHz	26.3@125MHz	76	-	6.6@1MHz
Area (μm^2)	**115.625**	**225.7**	233.5	360	250	-	-
Structure	**Open**	**Open**	Close	Open	Close	Close	Open

8ps, which corresponds to 0.36° at 125MHz. The worst case over PVT variations occurs at 80% of V_{DD}, $> 70°$C in the SS corner is 14.5 ps (0.65° at 125MHz).

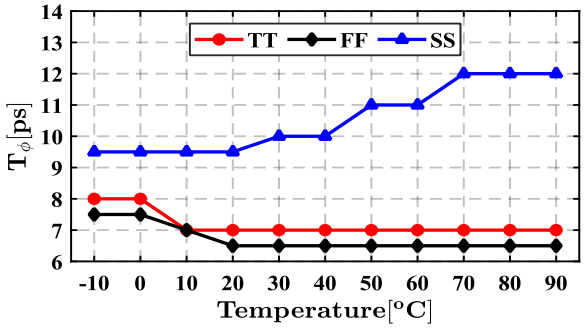


Fig. 6: Minimum detectable range of the proposed SRAM-based PFD in different corners for the temperature range of -10 to 90 degrees based on Post-Layout Simulation.

Transient waveforms are shown for the extracted simulation of design in 22nm FD-SOI technology for operation at 125 MHz for the output of the SRAM-based PFD for the case in which REF leads the FB with 7ps and 4ns is shown in Fig. 8. These cases correspond to the edges of the dead- and blind-zones. As can be seen, the SRAM-PFD is blind-zone free.

Comparison of the proposed SRAM-PFD to the state-of-the-art is shown in Table II. For a fair comparison, the proposed design simulated in 65nm CMOS technology as well. Table II shows the advantages of the proposed PFD which is smaller and can be more power-efficient than other topologies. The measured $\text{Jitter}_{\text{RMS}}$ for the proposed design is 448fs and 1.2ps in 22nm-FDSOI and 65nm CMOS technology, respectively.

V. Conclusion

This paper presented an SRAM-based PFD in two different technologies, 65nm CMOS and 22nm FDSOI, with a power consumption of 11.03μW and 7.2 μW when the power supply is 1.2V and 900mV. A proposed PFD in 22nm technology has a dead zone of 7ps up to 10GHz, and in 65nm it has a dead zone of 9ps and 8GHz, yet it is blind zone free, and it has a detection range of $\pm 2\pi$. Besides, the SRAM-based PFD occupies 115.625 μm^2 ($18.5\mu m \times 6.25\mu m$), in 22nmFDSOI,

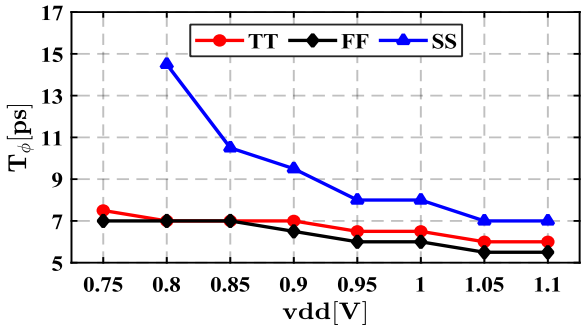
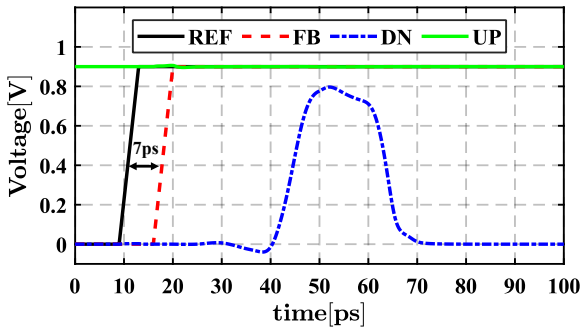
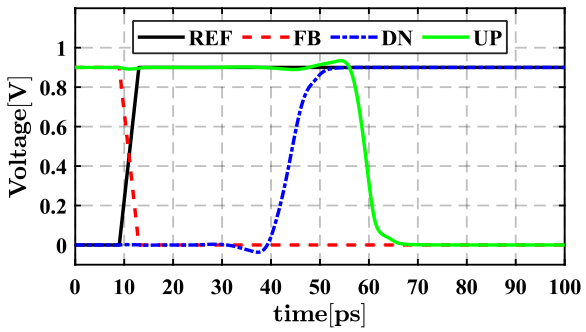


Fig. 7: Minimum detectable range of the proposed SRAM-based PFD in different corners for the supply range of 0.75V to 1.1V based on Post-Layout Simulation.



(a)



(b)

Fig. 8: The outputs of Post-Layout Simulation at 125MHz with respect to different time delay (a) 7ps (b) 4ns.

and 225.7 μm^2 ($15.57\mu m \times 14.5\mu m$), in 65nm . Therefore, not only was the proposed PFD a good candidate for the DLL and PLL, but it also can result in better integrity of the chip in applications such as Computing-in-Memory (CiM) and ADPLL whose integrity is one of the most important factors.

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