NeuroFlare: An mm^3-Scale Wireless Neural Interface Device With Simultaneous Neural Recording and Optical Stimulation

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***Abstract*— This article presents the creation of a wireless, miniature implantable opto-electro neural interface device called NeuroFlare, capable of simultaneous neural recording and optical stimulation. NeuroFlare features a low-power, dual-modal application-specific integrated circuit (ASIC) fabricated using the 180-nm CMOS process. To support the power-intensive optical stimulation in NeuroFlare, the ASIC employs a novel linear-charging switched-capacitor stimulation (LC-SCS) structure. The LC-SCS, operating under only a 1.2-V supply voltage, can illuminate the LED with a driving voltage three times the supply voltage and large current pulses of up to 12 mA while maintaining a high charging efficiency of 86.4%. In addition, LC -SCS requires only one off-chip capacitor, greatly facilitating device miniaturization. To accurately record neural signals in the presence of stimulation artifacts, the ASIC employs a delta-sigma modulator ($\Delta\Sigma$M)-based recording front end with a wide dynamic range (DR) to directly digitize the neural signals. The $\Delta\Sigma$M features a 2nd-order loop architecture implemented using a linearized transconductance-capacitor (Gm-C) integrator followed by an active noise-shaping (NS) successive approximation register (SAR) quantizer. The $\Delta\Sigma$M with a power consumption of 9.8 μW provides a peak DR of 83.7 dB, corresponding to a 400-mV$_{PP}$ linear input range. The $\Delta\Sigma$M's 173.8-dB figure of merit (FoM$_{DR}$) indicates its superior energy efficiency. The ASIC is assembled into a prototype of NeuroFlare measuring 2.8 × 3.5 × 0.7 mm^3. The recorded light-evoked local field potential (LFP) verified the functionality of NeuroFlare in vivo.**

***Index Terms*— Implantable miniature neural interface, neural recording, optical stimulation, wireless data transmission, wireless power transmission.**

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I. Introduction

IMPLANTABLE neural interface devices show great potential in exploring fundamental neural mechanisms, developing new therapies for neurological disorders, and enhancing human capabilities [1], [2], [3], [4], [5]. To drive the advancement of these applications, implantable neural interface devices are expected to have multiple features. First, they require the capability of neuromodulation and neural recording, as neural recording can provide immediate feedback for neuromodulation [6], [7]. In such dual-modal scenarios, simultaneous neural recording and stimulation are highly desired to fully capture neural signals during and after stimulation. This feature avoids missing useful signals during the recovery time of the recording front end, a common issue in conventional dual-modal neural interface devices where recording is OFF when stimulation is ON [8] and [9]. Second, the size of the implantable neural interface devices should be minimized to reduce their invasiveness and tissue damage during the implantation [10], [11]. Although leveraging integrated circuit (IC) technology that allows for the integration of all necessary circuits in a millimeter-scale silicon area can significantly reduce device size, the number and size of the required off-chip components remain a bottleneck for further miniaturization. Last but not least, these devices should be equipped with wireless power and data transmission techniques to eliminate the need for wire connections penetrating through tissue and batteries that hinder device miniaturization [12], [13].

In recent literature, researchers have demonstrated several miniature neural interface devices [14], [15], [16], [17], [18], [19], [19], [20], [21], [22]. All these devices achieve mm^3-scale and feature wireless power and data transmission. However, these devices can only support a single neural interface modality, either neural recording or stimulation. This limitation necessitates extra implantations to achieve simultaneous neural recording and stimulation. In addition, these additional implantations unavoidably separate the recording and stimulation sites. Moreover, the distance between these sites is limited by the size of each device.

Integrating both stimulation and recording functionalities in a single miniature device presents significant challenges.

First, the reduction in size of the power receiver (Rx), such as the inductive coil, limits the amount of power available to the miniature device. The limited power budget necessitates high energy-efficient circuit design, especially for operating the power-intensive optical stimulation. Optical stimulation requires a sufficiently high LED driving voltage to exceed the LED's forward voltage (V_F) and milliampere-level current pulses to ensure that the light intensity exceeds the threshold for effective stimulation, all within a total power budget of less than 1 mW. Second, neural stimulation may induce large artifacts that can saturate the neural recording front end if it remains ON during stimulation. Moreover, this artifact effect is exacerbated as the recording and stimulation sites get closer, as required in certain applications [23]. Therefore, a wide dynamic range (DR) is necessary for the neural recording front end to prevent it from saturation. Third, integrating additional neural interface functions may require extra off-chip components. However, the size and number of these components must be minimized to maintain the device's miniature form factor. Due to these challenges, miniature implants that support simultaneous neural recording and optical stimulation are currently unavailable.

To bridge this gap, our efforts focus on innovating application-specific IC (ASIC) designs for our NeuroFlare. To the best of our knowledge, NeuoFlare is the first mm^3-scale neural interface device capable of simultaneous neural recording and optical stimulation. Key innovations include a highly energy-efficient optical stimulator and a wide DR delta-sigma modulator ($\Delta\Sigma$M)-based direct digitizing recording front end. More specifically, the optical stimulator introduces a novel linear-charging switched-capacitor stimulation (LC-SCS) structure that presents multiple advantages: 1) providing a 3.6-V LED driving voltage and LED current pulses up to 12 mA with a supply voltage of only 1.2 V; 2) reducing loading on the inductive link thanks to its high charging efficiency of up to 86.4%; and 3) minimizing the required off-chip components to only one capacitor. The $\Delta\Sigma$M-based front end features a novel $\Delta\Sigma$M architecture consisting of a linearized transconductance-capacitor (Gm-C) integrator and a noise-shaping (NS) successive approximation register (SAR) quantizer. It offers 83.7-dB DR with a power consumption of 9.8 μW, indicating a superior figure of merit (FoM_{DR}) of 173.8 dB.

Fig. 1 demonstrates the conceptual view of the prototype NeuroFlare device, showing its use in optically stimulating target neurons while recording neural signals. The NeuroFlare device is wirelessly powered through an inductive link operating at 144 MHz, which also serves as the wireless data link. The use of a relatively high carrier frequency helps decrease the size of the Rx coil. NeuroFlare decodes stimulation parameters from the ON–OFF keying (OOK) modulated power carrier and then generates current pulses based on these parameters to drive the LED. Meanwhile, NeuroFlare records and digitizes the neural signal and wirelessly transmits the data back to the end user. A commercial software-defined radio (SDR)-based data Rx picks up the transmitted signal to decode the data. NeuroFlare is designed with all components assembled on a flexible substrate, including the ASIC wire-bonded on the top, a capacitor and an LED soldered on the bottom, and the Rx coil and electrode pads printed on the substrate. The entire device is coated with polyimide glue to enhance biocompatibility, resulting in a size of 2.8 × 3.5 × 0.7 mm and a weight of 12 mg.

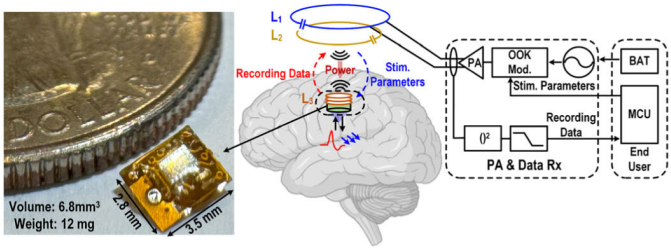


Fig. 1. Conceptual view of using the NeuroFlare device to simultaneously stimulate target neurons and record neural signals.

This article builds on our prior report [24] by providing a more comprehensive circuit analysis, detailed circuit implementation, and additional measurement results. Section II provides an overview of the ASIC architecture. Section III illustrates the operation of the LC-SCS and its advantages over previous designs, as well as the implementation of the charge pump (CP) in LC-SCS. Detailed design considerations and implementation of the $\Delta\Sigma$M are given in Section IV. Section V presents the ASIC's electrical performance measured in the benchtop setup. Section VI focuses on the in vivo evaluation of NeuroFlare. Section VII compares the performance metrics of NeuroFlare with other state-of-the-art designs, highlighting its distinct innovations and advantages.

II. ASIC Architecture

The architecture of the ASIC is presented in Fig. 2. In the power management block, the rectifier converts the received ac power carrier (V_{COIL}) to a dc voltage (V_{SUP}), while the low-dropout regulator (LDO) regulating V_{SUP} to a supply voltage (V_{DD}). Two on-chip capacitors are also integrated into the power management block to decouple the variation and noise on the two dc supply voltages, V_{SUP} and V_{DD}. The power carrier is also used as the data carrier for bidirectional wireless data transmission. The forward data telemetry, serving as the data Rx on the ASIC, decodes the user commands from the OOK-modulated V_{COIL} to configure the stimulation and recording settings. The LC-SCS provides milliampere-level LED current pulses with high energy efficiency. The $\Delta\Sigma$M-based recording front end directly quantizes the recorded neural signal with high resolution and wide DR. The backscatter-based data transmitter (Tx) transmits the digitized recording data through load-shift keying (LSK) modulation of the power carrier.

III. Linear-Charging Switched-Capacitor Stimulation

A. LC-SCS Architecture

In recent stimulation circuit designs, switched-capacitor stimulation (SCS), as shown in Fig. 3, is the most popular structure due to its higher efficiency compared to constant

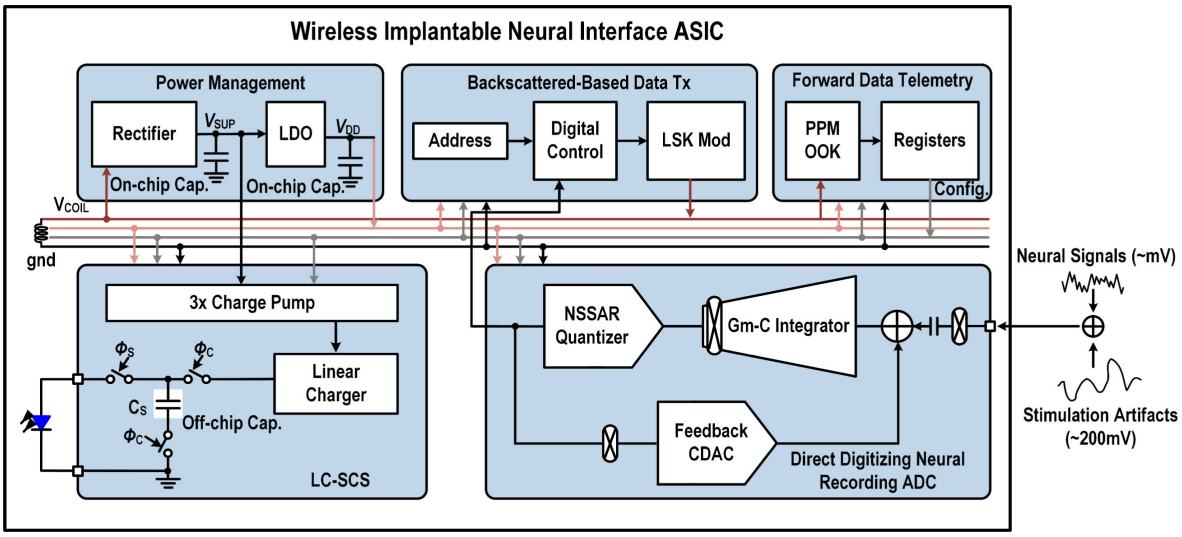


Fig. 2. Overview of the ASIC and its supporting off-chip components assembled in NeuroFlare.

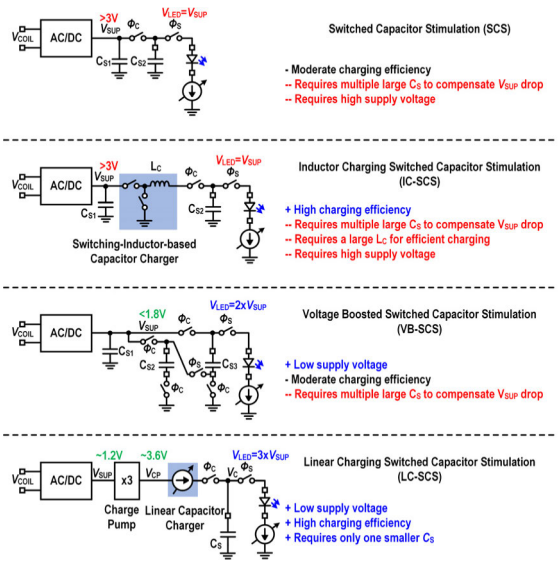


Fig. 3. Comparison between SCS, IC-SCS, and VB-SCS structures, and the proposed LC-SCS structure, highlights the LC-SCS's distinct advantages.

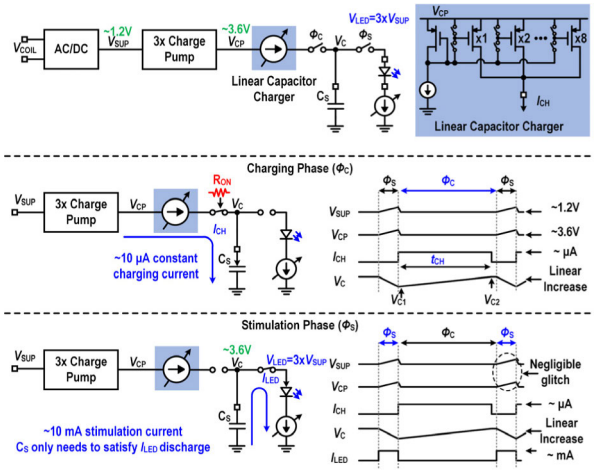


Fig. 4. Detailed circuit diagram and operation of the LC-SCS circuit.

current stimulation (CCS) [14], [25], [26], [27]. In SCS, the inductive link charges the storage capacitor (C_{S2}) during the charging phase (Φ_C). Then, the storage capacitor dumps its charge in the stimulation phase (Φ_S), resulting in milliampere-level LED current pulses. This method has three major limitations: limited charging efficiency, a high supply voltage requirement, and the need for an additional off-chip decoupling capacitor (C_{S1}). An inductor charging SCS (IC-SCS) design in [28] improves the charging efficiency by leveraging a switching inductor circuit. However, it requires a large off-chip inductor and the decoupling capacitor and still needs a high supply voltage. In [29], a voltage-boosted SCS (VB-SCS) structure leverages the capacitor stacking technique to reduce the required supply voltage by half, but it necessitates multiple off-chip capacitors. To address these disadvantages, we propose the LC-SCS structure.

Fig. 4 shows the detailed circuit diagram and operation scheme of LC-SCS. Compared with the traditional SCS structure, it introduces a self-gate-driven CP and a linear capacitor charger. The CP boosts the supply voltage, generating an output voltage, V_{CP}, which is equal to $3V_{SUP}$. In Φ_C, the linear capacitor charger, implemented with a 4-bit current digital-to-analog converter (IDAC), provides a microampere-level constant current to charge the storage capacitor (C_S) to V_{CP}. In Φ_S, C_S is disconnected from the charger and dumps its charge to the LED with a high driving voltage of $3V_{SUP}$ over a short period, resulting in a milliampere-level LED current (I_{LED}). The peak value of I_{LED} is set by a current limiter. Thanks to the linear-charging scheme, the supply glitch due to load variation between Φ_C and Φ_S is negligible. Thus, the decoupling capacitor on the V_{SUP} node can be reduced and implemented using an on-chip capacitor. As a result, the ASIC requires only one off-chip capacitor (e.g., 10 μF) for charge storage in the LC-SCS, greatly promoting device miniaturization.

The traditional SCS structure prevents the heavy load on the inductive link from milliampere-level LED current during Φ_S by using C_S to solely drive the LED. However, during Φ_C, the inductive link replenishes the charge in C_S in a short time, resulting in a large charging current that still loads the inductive link heavily. In addition, this large capacitor charging current degrades the charging efficiency due to the I^2R loss on the charging switch. The proposed LC-SCS features a low and constant charging current. This significantly reduces the loading on the inductive link during Φ_C, further improving charging efficiency. The total charging efficiency ($\eta_{\text{LC-SCS}}$) of the LC-SCS is determined by the power conversion efficiency (PCE) of the CP (η_{CP}) and the charging efficiency of the rest circuits, including the linear capacitor charger and the charging switch ($\eta_{\text{LC,S}}$). $\eta_{\text{LC,S}}$ is defined as

$$\eta_{\text{LC,S}} \approx \frac{E_C}{E_C + E_{\text{LOSS}}} \tag{1}$$

where E_C is the total energy transferred to C_s during Φ_C and E_{LOSS} represents the energy loss on the linear capacitor charger and the charging switch. E_{LOSS} includes both switching loss and conduction loss. Since the charging frequency of the LC-SCS, which is the same as the stimulation frequency (e.g., 1 Hz), is slow, the switching loss is negligible. Thus, E_{LOSS} contains the conduction loss on the capacitor charger and the charging switch. E_C depends on C_S's voltage (V_C) at the beginning and the end of each Φ_C. During Φ_S, V_C drops as C_S dumps its charge to drive the LED. When the stimulation pulse ends or V_C drops below the LED's V_F, C_S stops dumping charges, resulting in a residual voltage (V_{CRES}) on C_S. In each Φ_C, C_S is linearly charged from $V_{\text{C,RES}}$ to V_{CP} within a certain charging time (t_{CH}), using a constant charging current (I_{CH}). Thus, E_C can be expressed as follows:

$$E_C = \frac{1}{2} C_S \left(V_{CP}^2 - V_{\text{C,RES}}^2\right). \tag{2}$$

Because of linear charging, we can assume that the voltage across the capacitor charger linearly drops from $V_{CP} - V_{\text{C,RES}}$ to 0 V. Hence, E_{LOSS} can be written as follows:

$$\begin{aligned} E_{\text{LOSS}} &\approx \frac{1}{2}\left(V_{CP} - V_{\text{C,RES}}\right) I_{CH} t_{CH} + I_{CH}^2 R_{ON} t_{CH} \\ &= \frac{1}{2} C_S \left(V_{CP} - V_{\text{C,RES}}\right)^2 + I_{CH}^2 R_{ON} t_{CH} \end{aligned} \tag{3}$$

where R_{ON} is the turn-on resistance of the charging switch. Given (1)–(3), we can rewrite $\eta_{\text{LC,S}}$ as follows:

$$\begin{aligned} \eta_{\text{LC,S}} &\approx \frac{\frac{1}{2} C_S \left(V_{CP}^2 - V_{\text{C,RES}}^2\right)}{\frac{1}{2} C_S (V_{CP} - V_{\text{C,RES}})^2 + I_{CH}^2 R_{on} t_{CH} + \frac{1}{2} C_S \left(V_{CP}^2 - V_{\text{C,RES}}^2\right)} \\ &= \frac{\frac{1}{2} C_S \left(V_{CP}^2 - V_{\text{C,RES}}^2\right)}{C_S V_{CP} (V_{CP} - V_{\text{C,RES}}) + I_{CH}^2 R_{on} t_{CH}}. \end{aligned} \tag{4}$$

Taking η_{CP} into account, we can calculate $\eta_{\text{LC-SCS}}$ using the following equation:

$$\eta_{\text{LC-SCS}} = \eta_{\text{LC,S}} \times \eta_{CP}. \tag{5}$$

According to (4), a larger I_{CH} results in a lower $\eta_{\text{LC,S}}$ due to increased conduction loss in the charging switch. To prevent significant efficiency drops, we limit I_{CH} to below 20 μA in this design. Furthermore, I_{CH} is typically set at its minimal value that allows C_S to be fully charged to V_{CP} by the end of the charging time at each stimulation frequency setting. The use of the minimal I_{CH} also mitigates the CP's efficiency degradation by reducing CP's idle time when C_S is fully charged, thereby improving the overall efficiency. In addition, we sized the charging switch to reduce its conduction loss.

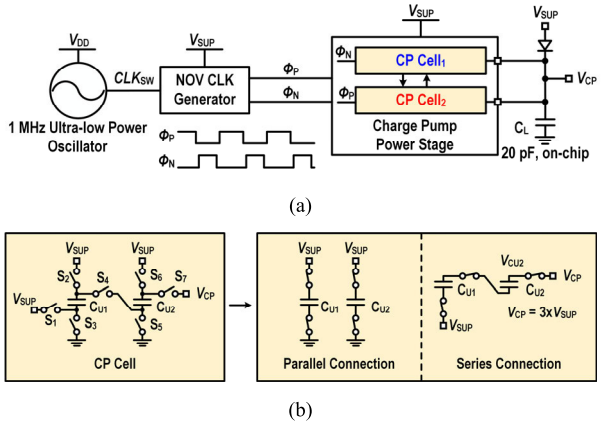


Fig. 5. Circuit diagram of (a) CP in LC-SCS and (b) CP cell's configuration in two phases (Φ_P and Φ_N) of each switching cycle.

B. Energy-Efficient CP With Self-Gate-Driven Mechanism

Fig. 5(a) shows the circuit diagram of the CP. The 1-MHz ultra-low-power relaxation oscillator generates the switching clock (CLK_{SW}), which is converted by the non-overlapping signal generator into two-phase gate driving signals, Φ_P and Φ_N. These signals drive the CP power stage to boost the supply voltage by a ratio of three. A diode-connected PMOS is placed between V_{SUP} and V_{CP} to provide an initial voltage at V_{CP}, facilitating the CP's start-up. In the CP power stage, there are two identical CP cells, Cell_1 and Cell_2. Each CP cell includes two flying capacitors, C_{U1} and C_{U2}, and seven switches, S_1–S_7, as shown in Fig. 5(b). Both C_{U1} and C_{U2} are implemented as a metal–oxide–semiconductor (MOS) capacitor in parallel with a metal–insulator–metal (MIM) capacitor. In layout, the MIM capacitor is vertically stacked on the MOS capacitor to save area. The CP cell utilizes serial-to-parallel topology due to its high efficiency. In each phase, each CP cell is configured in either the parallel or the series connection. In parallel connection, C_{U1} and C_{U2} are charged to V_{SUP} by closing S_2, S_3, S_5, and S_6. In serial connection, C_{U1} and C_{U2} are stacked by closing S_1, S_4, and S_7. Meanwhile, V_{SUP} is connected to the bottom plate of C_{U1}, resulting in an output voltage (V_{CP}), equal to $3V_{SUP}$, to charge the on-chip load capacitor, C_L.

Properly switching S_1–S_7 in Φ_P and Φ_N of every switching cycle is crucial to reduce the energy loss. In this work, we design a self-gate-driven mechanism that provides switches with a sufficiently high driving voltage. This mechanism offers several following advantages. First, it reduces the conduction loss and prevents charge leakage, significantly improving the CP's efficiency. Second, its implementation is simple, with nearly zero power and area overhead. Finally, it eliminates

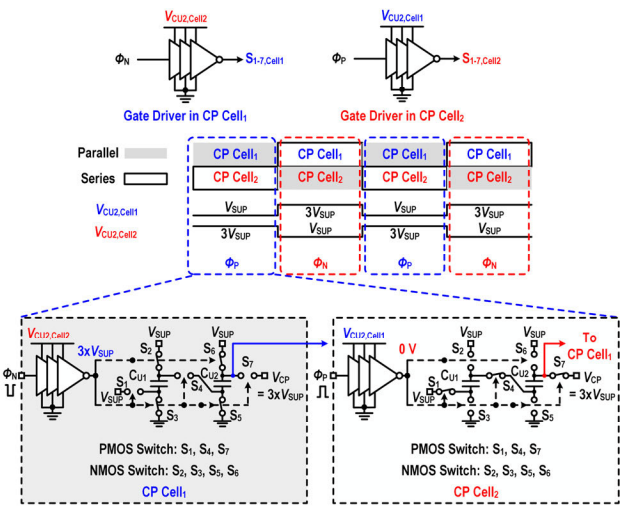


Fig. 6. Time-interleaved operation scheme of the two CP cells and the circuit configuration in Φ_P, demonstrating the self-gate-driven mechanism.

the need for a dedicated bootstrap gate driver or auxiliary CP, saving both power and area. As shown in Fig. 6, the bootstrapped gate driver in one CP cell is implemented using simple cascaded inverters to drive switches in that cell. The two CP cells are operated in a time-interleaved manner. The supply for the gate driver in one CP cell is provided by the voltage on the top plate of C_{U2} (V_{CU2}) in the other CP cell.

In Φ_P, Cell$_1$ operates in parallel connection, resulting in its $V_{CU2,Cell1}$ being equal to V_{SUP}, while Cell$_2$ operates in serial connection, resulting in its $V_{CU2,Cell2}$ being equal to $3V_{SUP}$. In this case, Cell$_2$ provides $3V_{SUP}$ as the supply voltage for the gate driver in Cell$_1$. In Cell$_1$, with such a high gate driving voltage, NMOS switches S_2, S_3, S_5, and S_6 are fully closed to allow C_{U1} and C_{U2} to be charged to V_{SUP}, while PMOS switches S_1, S_4, and S_7 are fully open to avoid charge leakage. Meanwhile, Cell$_1$ provides V_{SUP} to power Cell$_2$'s gate driver. The gate driver in Cell$_2$ does not need the high supply voltage of $3V_{SUP}$ in Φ_P since its zero output voltage is sufficient to fully close S_1, S_4, and S_7 while fully opening S_2, S_3, S_5, and S_6 in Cell$_2$. In Φ_N, the configurations of the two CP cells and the supply voltages for their gate drivers are reversed.

IV. ΔΣM-Based Neural Recording Front End

A. ΔΣM Architecture

The recording front end in this ASIC, which directly digitizes neural signals, requires high resolution to accurately quantize the signal, a wide DR to tolerate stimulation artifacts, and low power consumption to meet the stringent power budget of wireless miniature devices. To meet these requirements, we choose the continuous-time (CT) ΔΣM as the recording front-end architecture, with the detailed circuit diagram shown in Fig. 7. ΔΣM quantizes the input signal with 2nd-order NS, achieved using a Gm-C integrator followed by a 4-bit noise-shaping successive register approximation (NSSAR) quantizer. The capacitive digital-to-analog converter (CDAC) feeds back the reconstructed input signal to the input summing node, closing the loop. Chopping is employed to move the offset and flicker noise of the Gm-C filter out of signal band. This

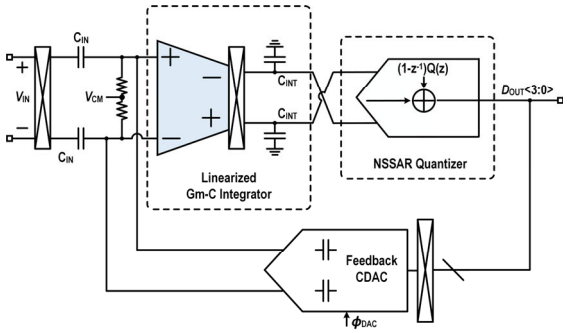


Fig. 7. Architecture of the ΔΣM-based direct digitizing recording front end.

ΔΣM is designed with a sampling frequency of 1.28 MHz and an oversampling ratio (OSR) of 64, resulting in a signal bandwidth of 10 kHz. This bandwidth allows the ΔΣM to capture both local field potential (LFP) and action potential (AP). The CT ΔΣM features inherent anti-aliasing and is easy to drive, making it suitable for directly digitizing neural signals. The low power consumption of the proposed CT ΔΣM can be attributed to the use of the Gm-C integrator. The open-loop nature of the Gm-C integrator relaxes the bandwidth requirement on its operational transconductance amplifier (OTA), thereby reducing power consumption. The use of the NSSAR contributes to improving both energy efficiency and area efficiency. The NSSAR increases the order of quantization NS using its internal ΔΣ loop. This feature allows the ΔΣM to use a smaller number of quantization levels to achieve the target resolution, which decreases both the power consumption and area consumption of the quantizer and feedback digital-to-analog converter (DAC). In addition, the use of NSSAR improves the tolerance of the CT ΔΣM to excess loop delay (ELD), further relaxing the bandwidth requirement on the OTA in the Gm-C integrator and eliminating the extra power and area overhead needed for implementing ELD compensation circuits [30].

To further demonstrate the energy and area efficiency improvements brought by the use of the 4-bit NSSAR, we compare our CT ΔΣM to other CT ΔΣM designs with different quantizer designs. To ensure a fair comparison, we design other CT ΔΣM configurations using the minimal quantization bits required to achieve the same signal-to-quantization noise ratio (SQNR) at a 64 OSR as our CT ΔΣM design. As shown in Fig. 8, our CT ΔΣM with a 4-bit NSSAR, which results in a noise transfer function (NTF) of $1 - z^{-1}$, achieves 100-dB SQNR with 64 OSR. Using this as a reference, there are two other designs that almost reach 100-dB SQNR with 64 OSRs. They are CT ΔΣM with a 6-bit passive NSSAR, which results in an NTF of $1 - 0.8z^{-1}$ [29], [31] and CT ΔΣM with an 8-bit SAR quantizer.

For the CT ΔΣM with 6-bit passive NSSAR, the passive integrator in the NSSAR can achieve near zero power overhead on its internal ΔΣ loop. However, using a passive integrator sacrifices the NS performance, as reflected in its NTF, necessitating higher required quantization bits. For the CT ΔΣM with an 8-bit SAR, the lack of an NS feature in the SAR quantizer requires even higher quantization bits to achieve the same SQNR level. Among these designs, our CT ΔΣM

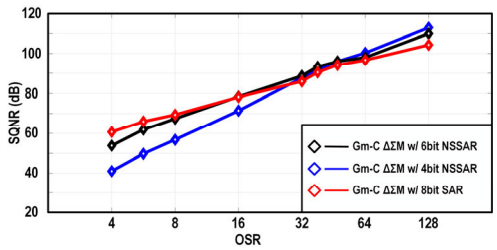


Fig. 8. Simulated SQNR of three CT ΔΣM designs with different quantizers.

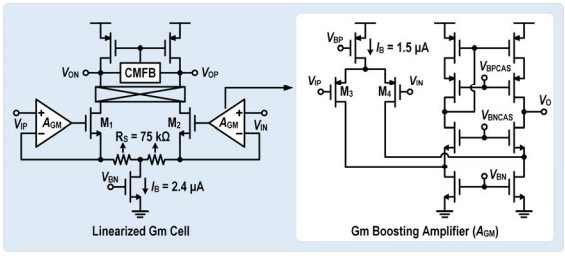


Fig. 9. Circuit diagram of the linearized Gm cell and its Gm-boosting amplifier.

with 4-bit NSSAR requires only a 4-bit quantizer and a 4-bit feedback DAC, offering the highest energy efficiency and area efficiency. Hence, this structure was selected for the CT ΔΣM in our ASIC.

B. Circuit Implementation of the Linearized Gm-C Integrator and 4-bit NSSAR Quantizer

The Gm-C integrator features low power consumption but suffers from poor linearity. To improve its linearity, we adopt two methods. First, the Gm-C is placed after the input summing node, reducing the signal swing at the Gm's input [32], [33]. Second, we leverage the gain-boosting technique described in [20], to suppress the nonlinearity of transistors, M_1 and M_2, in the Gm cell. Fig. 9 shows the detailed circuit diagram of the linearized Gm cell. The gain-boosting technique that includes auxiliary amplifiers, A_{GM}, and source degeneration resistors, R_S, regulates the Gm to

$$G_m = \frac{g_{m1,2}A(s)}{1 + g_{m1,2}A(s)R_s} \tag{6}$$

where $A(s)$ is the transfer function of A_{GM} and $g_{m1,2}$ is the transconductance of M_1 and M_2. The Gm is approximately equal to the $1/R_S$ when A_{GM} has a sufficiently high gain. This greatly decreases the Gm's variation due to the residual voltage at the input summing node, improving the Gm-C's linearity. To achieve a high gain for A_{GM}, we design a folded-cascode OTA. The PMOS input pair is biased with a relatively large tail current of 1.5 μA to reduce the thermal noise of Gm-boosting amplifier. In addition, the input pair is properly sized to achieve a high gm/id ratio, further enhancing its transconductance.

The 4-bit NSSAR quantizer includes bootstrap switches, a CDAC ($CDAC_{SAR}$), a multi-input comparator, SAR logic, and an integrator that consists of residual sampling capacitors (C_{RS}), integration capacitors ($C_{INT,SAR}$), and an OTA, as shown

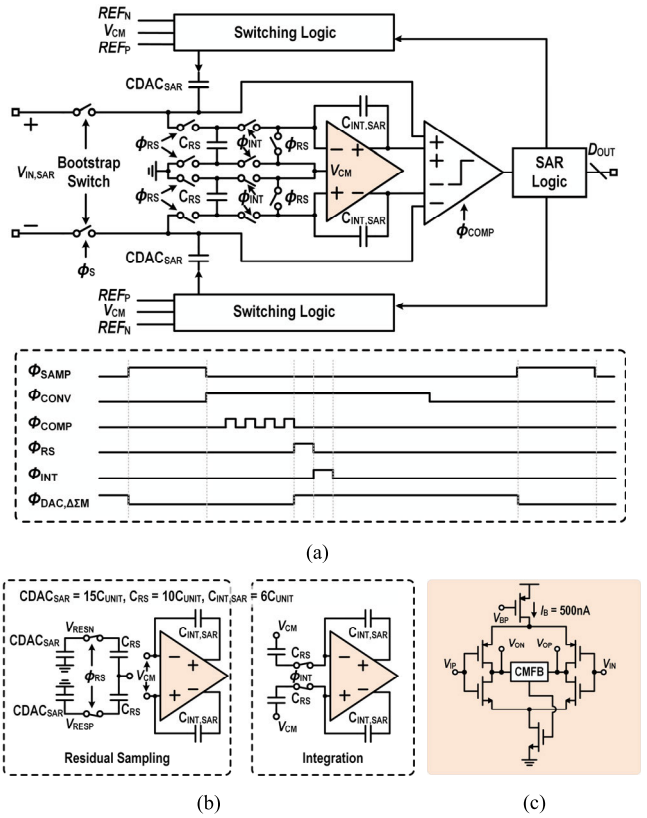


Fig. 10. Circuit diagram of (a) NSSAR, (b) integrator in the NSSAR under different operation phases, and (c) OTA in the integrator.

in Fig. 10. According to the timing diagram of the NSSAR operation, the NSSAR samples the Gm-C's output voltage onto its $CDAC_{SAR}$ during the sampling phase (Φ_{SAMP}). Afterward, the NSSAR quantizes the summation of the sampled voltage on $CDAC_{SAR}$ and the integration voltage on $C_{INT,SAR}$ during the conversion phase (Φ_{CONV}), achieving a cascaded integrator feed-forward (CIFF) structure for the internal ΔΣ loop in the NSSAR. The summation is realized by feeding both the sampled voltage and the integration voltage into the multi-input comparator. After the LSB is generated, the feedback CDAC in the ΔΣM samples the 4-bit output data of the NSSAR and refreshes its output voltage during $\Phi_{DAC,\Delta\Sigma M}$. After Φ_{CONV}, a residual voltage remains on $CDAC_{SAR}$. This residual is then sampled onto C_{RS}, during the residual sampling phase (Φ_{RS}), by connecting the top plate of C_{RS} to $CDAC_{SAR}$. Subsequently, in the integration phase (Φ_{INT}), the bottom plate of C_{RS} connects to the input node of the OTA in the NSSAR integrator, and the top plate connects to the common mode voltage (V_{CM}), transferring the charge in C_{RS} to $C_{INT,SAR}$. Since the voltage across $C_{INT,SAR}$ will not be reset, this residual sampling and integration process integrates the residual voltage after each Φ_{CONV}. The ratio between $CDAC_{SAR}$, C_{RS}, and $C_{INT,SAR}$ is set to 15:10:6 to achieve the NTF of $1 - z^{-1}$. Since the NSSAR integrator's nonlinearity and noise will be suppressed by the first Gm-C integrator in the CT ΔΣM, its design requirement is greatly relaxed. Specifically, we employ an inverter-based OTA with a small power overhead of 500 nW.

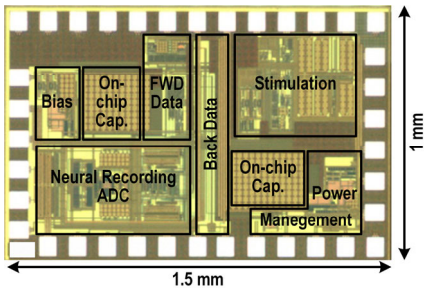
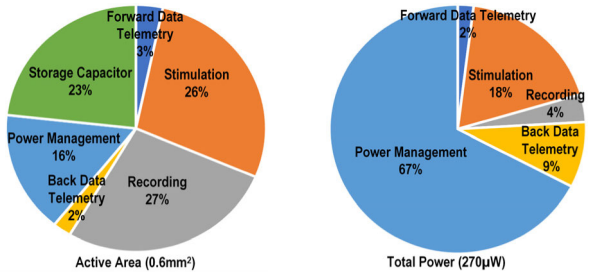


Fig. 11. Micrograph of the miniature neural interface ASIC.



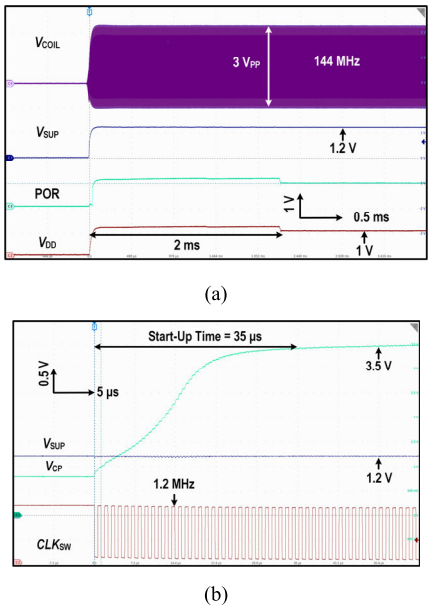
(a) (b)

Fig. 12. Pie charts demonstrate the breakdown of (a) active silicon area and (b) average power consumption of the ASIC.

V. Measurement Results

The neural interface ASIC was fabricated using the TSMC 180-nm CMOS process. The micrograph of the ASIC in Fig. 11 shows the silicon area is 1.5 × 1 mm, including testing pads. The total active area is 0.6 mm^2, as shown in Fig. 12(a). The ΔΣM-based direct digitizing recording front end and the LC-SCS circuit are the top two contributors to the chip area, primarily due to the capacitor array in the ΔΣM and the flying capacitor in the CP of the LC-SCS. The ASIC consumes an average power of 270 μW. Fig. 12(b) details the power consumption of each circuit block. The power management block consumes most of the power due to the limitation in its rectifier's PCE at the high carrier frequency of 144 MHz. The remaining circuit blocks consume only 33% of the total power consumption, thanks to their low-power designs.

We measured the start-up transient of the ASIC, as shown in Fig. 13(a). Upon receiving the 144-MHz ac power with an amplitude of $3V_{PP}$ at the Rx coil, the rectifier converts the ac power to a 1.2-V dc voltage, V_{SUP}. Subsequently, the LDO begins to regulate the 1.2-V V_{SUP} to a supply voltage, V_{DD}, which stabilizes at 1 V after 2 ms. The power-on-reset (POR) circuit is triggered when V_{DD} reaches 600 mV, generating a flag to prepare the forward data telemetry for receiving user commands. Once the stimulation function is enabled, the CP begins boosting V_{SUP}, with a conversion ratio of 3, resulting in $V_{CP} = 3V_{SUP}$. Fig. 13(b) demonstrates the measured start-up transient of the CP. When the CP wakes up, its ultra-low power oscillator starts to generate a 1.2-MHz switching clock, CLK_{SW}. Then, CLK_{SW} drives the CP power stage to gradually charge the load capacitor. After approximately 35 μs, V_{CP} reaches 3.5 V and begins to charge the storage capacitor in preparation for optical stimulation.



(a) (b)

Fig. 13. Measured transient waveforms of (a) power management circuits during start-up and (b) CP start-up.

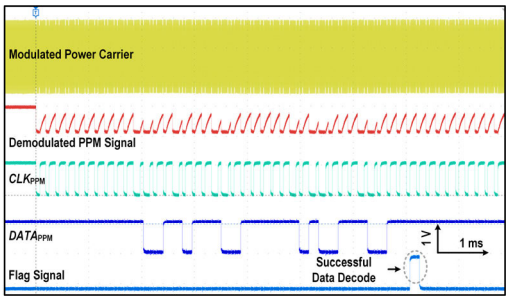


Fig. 14. Transient waveform of the key nodes in forward data telemetry.

As shown in Fig. 14, user commands are encoded in the OOK-modulated power carrier of the inductive link at a data rate of 6 kb/s. We choose pulse-position-modulated OOK (PPM-OOK) as the modulation scheme due to its simplicity and robustness [25]. In the PPM-OOK scheme, each data "0" and data "1" is encoded using a pair of pulses with different intervals. In the ASIC, the forward data telemetry demodulates the power carrier and then converts the extracted PPM pulses to a saw-wave-like demodulated PPM signal. In this signal, a higher peak indicates a data "1" and a lower peak indicates a data "0." By comparing this demodulated PPM signal with a reference voltage, the forward data telemetry extracts the clock signal (CLK_{PPM}) and the synchronized data signal ($DATA_{PPM}$). After receiving a 48-bit complete user command data packet, the forward data telemetry compares the packet's header bits with the pre-defined header bits in the ASIC. Upon a successful match, a flag signal is raised to indicate successful data transmission.

Fig. 15 demonstrates the transient operation of the LC-SCS delivering LED current pulses at 0.6 Hz with a pulsewidth of 2 ms. With V_{SUP} at 1.25 V, the CP in the LC-SCS generates a V_{CP} of 3.6 V. After each stimulation pulse, the LC-SCS recharges a 22-μF C_S with a 12-μA charging current (I_{CH}).

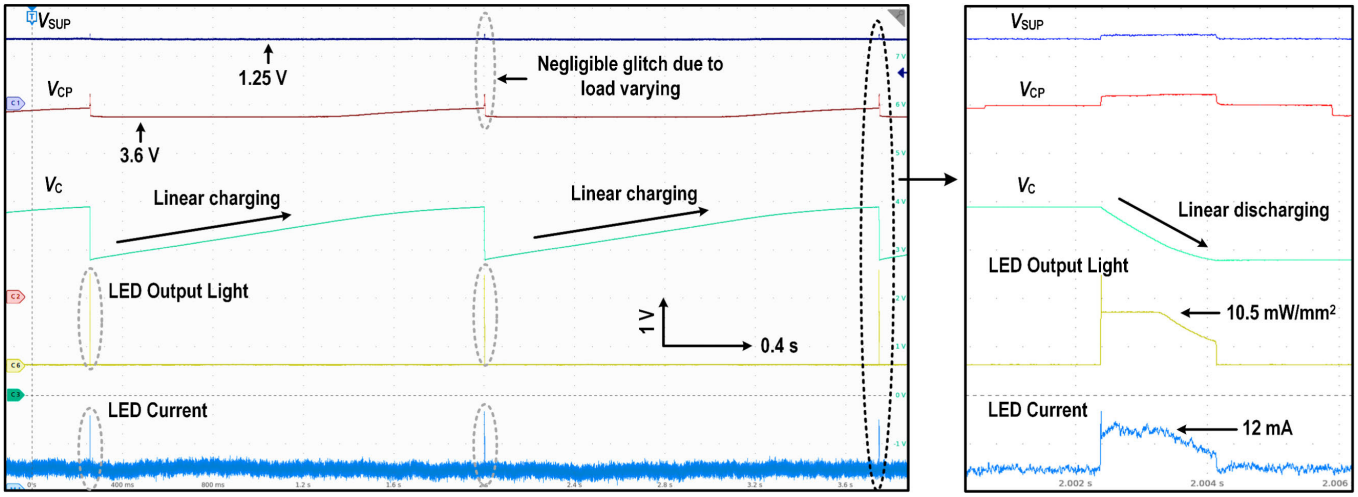


Fig. 15. Transient LC-SCS operation that linearly charges the storage capacitor and drives LED with high instantaneous current pulses.

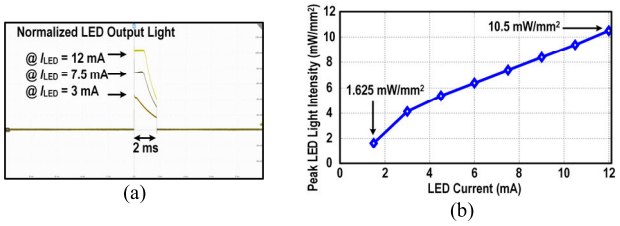


Fig. 16. Measured (a) LED output light transient waveform and (b) LED light intensity at different LED current levels.

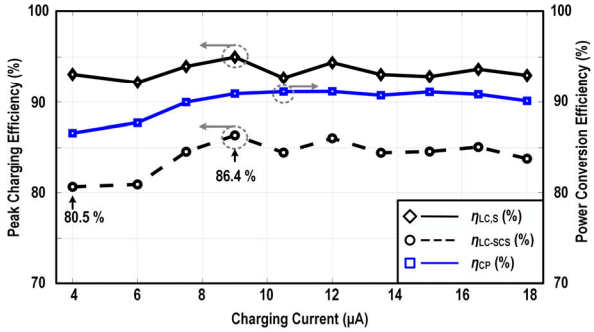


Fig. 17. Measured $\eta_{LC,S}$, η_{CP}, and $\eta_{LC\text{-}SCS}$ with different charging currents.

Consequently, V_C linearly increases during the charging phase (Φ_C). As V_C approaches V_{CP}, the voltage headroom of the linear capacitor charger decreases, causing I_{CH} to decrease gradually. Once the stimulation pulse arrives, C_S drives the LED with an approximately 3.6-V driving voltage, while the supply voltage for the LC-SCS is only 1.25 V. The current limiter sets the peak I_{LED} to 12 mA, resulting in a 10.5-mW/mm^2 light intensity. In the stimulation phase (Φ_S), both V_{SUP} and V_{CP} have voltage glitches due to load variation. However, the glitch on V_{SUP} is less than 20 mV, which does not influence the LDO's output, eliminating the need for a large off-chip decoupling capacitor at the V_{SUP} node. The LC-SCS can deliver current pulses with frequencies from 0.125 to 1 Hz, pulsewidths from 1 to 4 ms, and current levels from 1.5 to 12 mA. Fig. 16(a) shows the LED output light transient at I_{LED} of 3, 7.5, and 12 mA, measured using the optical meter (Newport 2936-R). The blue LED (Cree TR2227TM) is soldered on the bottom of the board and coated with polyimide. The optical power detector (Newport 818 SL/DB) is placed directly over the LED, completely covering it during measurement to capture all emitted light. The measured LED output light intensity at different I_{LED} ranges from 1.625 to 10.5 mW/mm^2, exceeding the 1-mW/mm^2 threshold for effective optical stimulation [34].

To comprehensively evaluate the charging efficiency of the LC-SCS, we measured the total charging efficiency ($\eta_{LS\text{-}SCS}$), the charging efficiency of the linear capacitor charger and the charging switch ($\eta_{LC,S}$), as well as the CP's PCE (η_{CP}) at different I_{CH}'s. During the measurement, we set I_{LED} to 12 mA and stimulation pulsewidth to 1 ms. In Fig. 17, the peak $\eta_{LC,S}$ was measured at different I_{CH} values ranging from 4 to 18 μA. These are the minimum I_{CH} values needed for V_C to reach V_{CP} by the end of charging time at different stimulation frequencies ranging from 0.125 to 1 Hz. The peak $\eta_{LC,S}$ ranges from 92.1% to 95%, while $\eta_{LS\text{-}SCS}$ ranges from 80.5% to 86.4%. This difference is attributed to η_{CP}, which ranges from 86% to 91.1%. The LC-SCS maintains a charging efficiency of at least 80% when the charging current is larger than 4 μA. These results indicate the high energy efficiency of the LC-SCS, which can be attributed to the following factors: the slow charging frequency minimizes the charging switch's switching loss, the small I_{CH} reduces the charging switch's conduction loss, and the constant I_{CH} mitigates the CP's load variation and subsequent efficiency degradation.

The energy efficiency of the optical stimulation is heavily influenced by the LED's energy conversion efficiency, which depends on factors such as temperature, LED materials, and packaging [35], [36]. Specifically, the LED (Cree TR2227TM) used in our in vivo experiment typically generates a radiant flux of 27 mW with a forward current of 20 mA and a forward voltage of 3.3 V [37]. This corresponds to an energy conversion efficiency of approximately 41%, significantly limiting the total energy efficiency of the optical stimulation below 40%. To address this limitation and provide a more

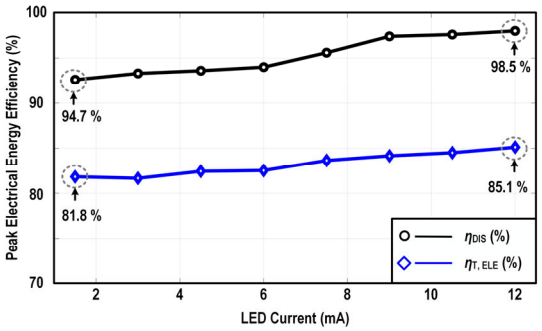


Fig. 18. Measured $\eta_{T,ELE}$ and η_{DIS} with different LED currents.

accurate evaluation of the LC-SCS performance, we introduce a new metric: the total energy transfer efficiency ($\eta_{T,ELE}$). This metric is defined as the ratio of the total electrical energy delivered to the LED to the total energy supplied to the circuit. By excluding the impact of the LED's energy conversion efficiency, this new metric provides a more accurate evaluation of the circuit's performance. In the LC-SCS scheme, the process of delivering energy to the LED involves two phases: charging the capacitor and discharging the stored charge to the LED. Thus, $\eta_{T,ELE}$ can be expressed as follows:

$$\eta_{T,ELE} = \eta_{LC\text{-}SCS} \times \eta_{DIS} \tag{7}$$

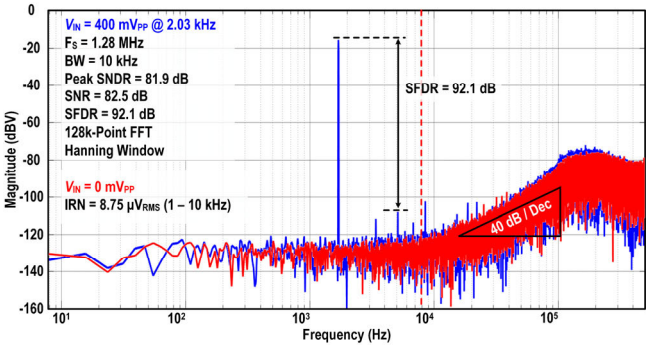
where η_{DIS} represents the discharging efficiency, defined as the ratio of the electrical energy delivered to the LED to the energy transferred out of the capacitor in the discharging phase. To comprehensively evaluate $\eta_{T,ELE}$, we have measured the peak $\eta_{T,ELE}$ and η_{DIS} at different LED currents, as shown in Fig. 18. At each LED current level, the charging current is optimized to ensure the highest charging efficiency. η_{DIS} and $\eta_{T,ELE}$ range from 94.7% to 98.5% and from 81.8% to 85.1%, respectively, across LED currents from 1.5 to 12 mA. These results indicate that the proposed LC-SCS not only provides high charging efficiency but also achieves good overall energy efficiency.

Table I compares the proposed linear-charging scheme with other capacitor charging schemes. The proposed scheme improves charging efficiency by 19% compared to the design in [27], which uses an ac-to-cap charging scheme. Although the switching-inductor-based charging schemes in [28] and [38] offer higher efficiency, they require large off-chip inductors ($\sim\mu$H), challenging the device miniaturization. Furthermore, the charging efficiency of this work could be enhanced by improving the CP's efficiency.

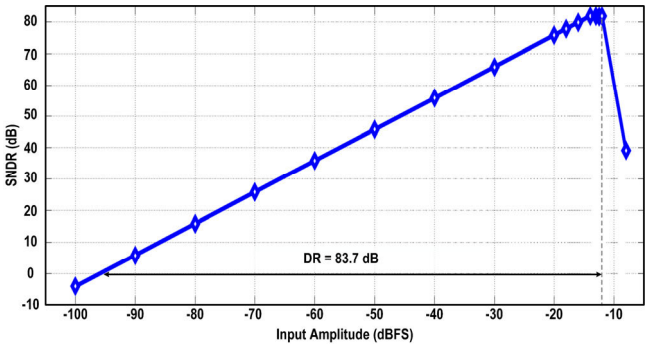
Fig. 19(a) demonstrates the output power spectrum density (PSD) of the $\Delta\Sigma$M-based recording front end. A 400-mV$_{PP}$ sinusoidal signal at 2.03 kHz is generated using the audio analyzer (Stanford Research System, SR1) and fed to the input of the $\Delta\Sigma$M. The $\Delta\Sigma$M quantizes the input sinusoid with a 1.28-MHz sampling rate. Subsequently, 128 000 points of output data are collected using a logic analyzer. We conducted an offline calibration to address the mismatch error in the $\Delta\Sigma$M's feedback CDAC by applying correction coefficients to the ADC's output. The Nelder–Mead algorithm was used to determine the optimal coefficients, effectively compensating for the mismatch. We analyzed the output data using the fast Fourier transform (FFT) with a Hanning window. The PSD shows a 2nd-order NS. Within a 10-kHz signal bandwidth, the $\Delta\Sigma$M achieves a signal-to-noise-and-distortion ratio (SNDR) of 81.9 dB, a signal-to-noise ratio (SNR) of 82.5 dB, and a spurious-free DR (SFDR) of 92.1 dB. The resultant effective number of bits (ENOB) is 13.3 bits. Fig. 19(a) also presents the $\Delta\Sigma$M's output PSD with shorted input, demonstrating its input-referred noise (IRN) PSD. The $\Delta\Sigma$M achieves an integrated IRN voltage of 8.75 μV$_{RMS}$ over a bandwidth of 1 Hz–10 kHz. We also measured the SNDR at different input amplitudes, as shown in Fig. 19(b). The DR is 83.7 dB, corresponding to a linear input range of 400 mV$_{PP}$.

TABLE I
COMPARISON BETWEEN DIFFERENT CAPACITOR CHARGING SCHEMES

Reference	This Work	TIA' 16 Lee [35]	JSSC' 24 Park [27]	JSSC' 24 Eom [28]
Charging Scheme	Linear Charging	Inductor Charging	AC-to-Cap	Inductor Charging
V_C (V)	3.6	4.2	0-4	0-3
Supply Voltage (V)	1.2	4.2	4.5	3.3
C_S (μF)	1 - 22	10	N/A	10
Max Char. Current (mA)	0.018	N/A	N/A	110
Peak η_{CHAR} (%)	86.4	93	72.6	90
Off-chip Components	None	1 Inductor (10 μH)	1 Coil, 1 Cap (~ nH/ ~μF)	1 Inductor (10 μH)



(a)



(b)

Fig. 19. (a) Measured output PSD of the $\Delta\Sigma$M with a 400-mV$_{PP}$ input and shorted input and (b) peak SNDR measured at different input amplitude.

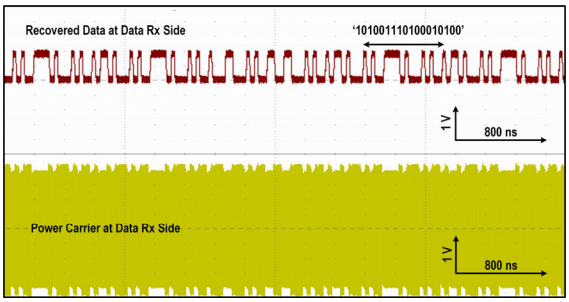
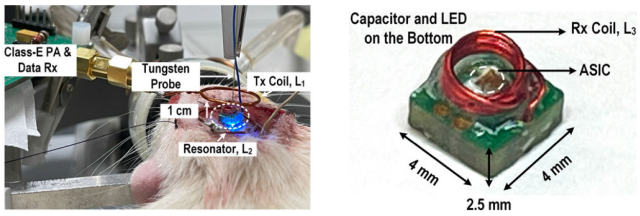


Fig. 20. Transient measurements of the recovered data stream and the modulated power carrier at the data Rx side.



(a) (b)

Fig. 21. (a) In vivo experiment setup. (b) Implementation of the NeuroFlare device used during the in vivo experiment.

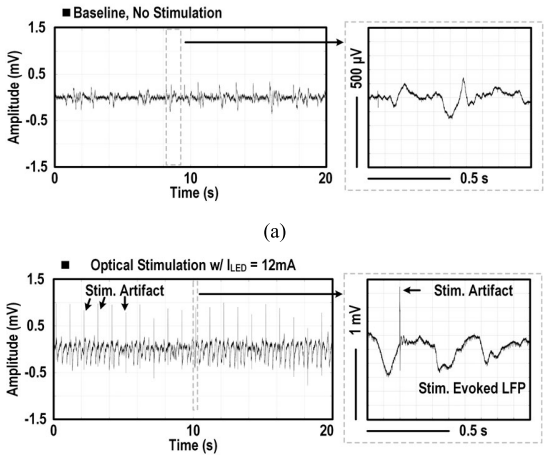


Fig. 22. Examples of 20-s transient LFP signals recorded from the left V1 lobe: (a) without stimulation and (b) with stimulation applied.

Every 4-bit $\Delta\Sigma$M output data, 1-bit stimulation flag, and 9-bit header are packetized together, resulting in a serial data stream with a data rate of 17.92 Mb/s. The packetized data stream then LSK modulates the power carrier to transmit the data back to the end user. Fig. 20 presents the modulated power carrier and the data stream recovered at the data Rx side. The consistency between the recovered data stream and the modulation waveform on the power carrier indicates successful data transmission and decoding.

VI. In Vivo Verification

The functionality and performance of our NeuroFlare were verified through in vivo experiments. Fig. 21(a) illustrates the experimental setup. The animal subject is an adult male Sprague Dawley rat with a weight of 770 g. All animal procedures were conducted with approval from the Institutional Animal Care and Use Committee (IACUC) of Michigan State University. The rat received an injection of the virus (AAV-hSyn-hChR2 (H134R)-mCherry) into its primary visual cortex (V1) to induce the expression of neurons with the light-sensitive protein channelrhodopsin-2 (ChR2). After the virus injection, a four-week incubation period was conducted for optimal ChR2 opsin expression. When the experiment started, the rat was under isoflurane anesthesia.

As shown in Fig. 21(b), the NeuroFlare device was built with the ASIC, along with the Rx coil, capacitor, and LED all assembled on a rigid PCB, resulting in a device size of 4 $\times$ 4 $\times$ 2.5 mm and a weight of 18 mg. The Rx coil is wire-wound around the ASIC, resulting in a diameter of 3 mm, while the capacitor and LED are soldered on the bottom. The NeuroFlare device was placed on the skull above the left V1 lobe, with the LED positioned to make contact with the surface tissue in the left V1 lobe. A tungsten electrode, connected to a pad on the bottom of the rigid PCB, penetrated the tissue at the left V1 to a depth of 800 μm to record the neural signals. In addition, the ground wire was placed underneath the subject's skin to bias the animal body. Since the input impedance of the recording front end is limited to 7.8 MΩ due to chopping, we processed the tungsten electrode to reduce its impedance below 0.2 MΩ, mitigating signal attenuation. We implemented a three-coil inductive link with a carrier frequency of 144 MHz, which served as both the power and data link for wireless power and data transmission with the NeuroFlare device. This inductive link achieves a power transfer efficiency (PTE) of 11.3%, measured with a thin tissue layer (e.g., beef) placed between the Tx and Rx coils to simulate tissue effect. Furthermore, the link configuration is robust against horizontal misalignment, as demonstrated in [13]. To ensure the safety of wireless power transmission, the specific absorption rate (SAR) is simulated with the input power set to 2.5 mW, providing sufficient power to the device. The simulated maximum local SAR is 0.081 W/kg, which is below the safety limit of 1.6 W/kg. The Class-E power amplifier (PA) drove the Tx coil to deliver power, while the SDR-based data Rx picked up the reflected wave at the Tx coil to decode the backscattered data from the ASIC. The Tx coil is positioned approximately 1 cm above the Rx coil to improve PTE and reduce the bit error rate (BER) of the back data link. Upon receiving user commands via the OOK-modulated power carrier, the ASIC delivered LED current pulses at 1 Hz with a pulsewidth of 1 ms and an amplitude of 12 mA to stimulate the genetically modified neurons in the left V1 lobe. Meanwhile, the ASIC digitized the neural signal recorded through the tungsten electrode and sent the digital data back via the inductive link to the SDR-based data Rx.

LFP provides stable and reliable results of population-level neural activity. We chose to use the LFP as the primary benchmark to validate the system's functionality and performance. The LFP was extracted from the recorded neural signal using a 1–300-Hz bandpass filter, as shown in Fig. 22. Fig. 22(a) shows the baseline LFP when the optical stimulation is OFF. Compared with the baseline, the recorded LFP when

TABLE II
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART ASICS FOR MINIATURE NEURAL INTERFACE DEVICE

	Reference	This Work	TBioCAS' 18 Jia [14]	JSSC' 19 Ghanbari [15]	Nat. Electron.' 20 Lee [16]	JSSC' 23 Lee [20]	CICC' 23 Zhao [29]
System	Technology	180 nm	350 nm	65 nm	65 nm	110 nm	180 nm
	Chip Area (mm^2)	1.5	1	0.25	0.25	4	2
	Supply Voltage (V)	1 / 1.25	5	1	1	1 / 2.3	1.2 / 1.8
	Wireless Link	RF, 144 MHz	RF, 60 MHz	US, 1.78 MHz	RF, 915 MHz	Body Link, 32MHz	RF, 60 MHz
	Total Power (mW)	0.27[b]	1[b]	0.028[c]	0.030[b]	0.644[c]	0.24[b]
	Implants Vol. & Weight	6.8 mm^3, 12 mg	9.375 mm^3, 15 mg	2.4 mm^3, -	0.11 mm^3, -	32 mm^3, -	0.45 cm^3, -
	Required Off-Chip Components / Channel[a]	1 Coil, 1 Capacitor	1 Coil, 3 Capacitors	1 US Transducer	None	2 Electrodes for Power & Data	1 Coil, 3 Capacitors
	System Modality	Opt. Stim. + Rec.	Opt. Stim.	Rec.	Elec. Sti. / Rec.	Rec.	Opt. Stim. + Rec.
Stimulation	Stim. Topology	LC-SCS	SCS	-	CCS	-	VB-SCS
	Stim. Supply (V) / LED Drive Volt. (V)	1.2 V / 3.6V	5 V / 5 V	-	1 V / -	-	1.8 V / 3.6
	Max Stim. Current (mA)	12	10	-	0.025	-	8
	Max η_{CHAR} (%)	95[d] / 86.4	37	-	-	-	-
Recording	Topology	CT-ΔΣM	-	LNA	CT-ΔΣM	CT-ΔΣM	CT-ΔΣM
	Power (μW) / Channel	9.8	-	4	3.2	8.6	10.8
	Area (mm^2) / Channel	0.15	-	-	0.01	0.04	0.47
	Supply (V)	1	-	1	1	1	1.2
	IRN (μV_{RMS})	8.75	-	5.3	2.2	6.6	14.6
	Signal BW (kHz)	10	-	5	0.5	10	10
	SNDR/DR (dB)	81.9 / 83.7	-	- / -	51 / -	82.3 / 83.3	70.1 / 71.6
	Peak Input (mV_{PP})	400	-	20	2	300	300
	FoM_{SNDR} / FoM_{DR}	172.2 / 173.8	-	- / -	133 / -	173 / 174	159.8 / 161.3

[a]Exclude the commonly required off-chip components for neural recording and stimulation. (e.g. electrodes, LEDs) [b]Measured at maximum stimulation current. [c]No stimulation function.
[d]Measured charging efficiency only includes linear capacitor charger and the charging switch.

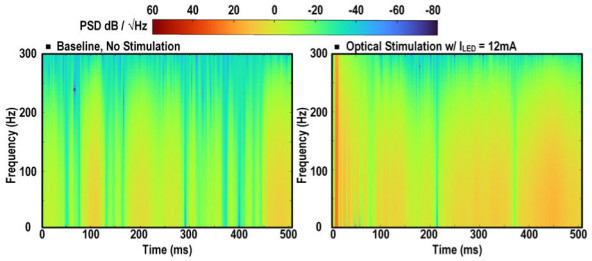


Fig. 23. Spectrogram of the LFP signals within the 500-ms time window without and with stimulation applied.

optical stimulation is ON has a significantly higher amplitude, as shown in Fig. 22(b). In addition, the stimulation-induced artifact is also visible alongside the desired LFP signal. Thanks to its 400-mV_{PP} linear input range, the ΔΣM-based recording front end is able to accurately capture neural signals even in the presence of artifacts.

Fig. 23 shows the spectrogram of the baseline LFP and the stimulation-evoked LFP over a 500-ms time window. To obtain the LFP spectrogram, for the baseline LFP, we sliced the 33-s-long LFP transient data into 33 segments. Each data segment is 1 s long. For the stimulation-evoked LFP, we used the rising edge of the stimulation pulse as the starting point to segment LFP transient data and align each segment. Then, we averaged the 33 segments and plotted the spectrogram of the averaged segment within the first 500 ms using short-time Fourier transform (STFT) [39]. The color bar in Fig. 23 visualizes the LFP energy strength. After each stimulation, the recorded LFP exhibits significantly higher energy, particularly within the first 100-ms time window following the stimulation pulse. In contrast, neural activity is less activated when the stimulation is OFF, as observed from the lower energy in the baseline LFP.

VII. COMPARISON AND CONCLUSION

In Table II, we summarized the performance metrics of the NeuroFlare device and its ASIC and compared them with the state-of-the-art designs. To the best of my knowledge, NeuroFlare is the first miniature neural interface device that supports simultaneous neural recording and power-intensive optical stimulation. With innovative circuit designs, such as the LC-SCS and the ΔΣM-based direct digitizing recording front end in the ASIC, the NeuroFlare device requires only one off-chip storage capacitor, one LED, and one Rx coil, greatly enhancing its miniature form factor. Consequently, the latest NeuroFlare prototype (see Fig. 1) measures 6.8 mm^3 in size and weighs 12 mg. Compared to other stimulation structures, our proposed LC-SCS can drive the LED with high driving voltage and high current pulses using lower and more constant input power, reflected in a much lower required supply voltage and smaller charging current. This lower and more constant input power lightens the loading on the inductive link, facilitating wireless power transmission to NeuroFlare. In addition, the LC-SCS reduces the variation in transient loading on the supply nodes. This decreases the required decoupling capacitor values, enabling their on-chip implementation and thereby reducing the off-chip capacitors required by the ASIC to only one.

In our ΔΣM design for the direct digitizing recording front end, we introduce an alternative low-power ΔΣM architecture consisting of a linearized Gm-C integrator followed by

a 4-bit NS SAR quantizer, achieving state-of-the-art performance. Within its 10-kHz bandwidth, the $\Delta\Sigma$M-based front end can capture both LFP and AP with a peak SNDR of 81.9 dB and a DR of 83.7 dB. Achieving this performance, the $\Delta\Sigma$M-based front end consumes only 9.8 μW of power. Its high energy efficiency is reflected in a promising FoM_{DR} of 173.8 dB. Moreover, we comprehensively evaluated our NeuroFlare device with incorporation of wireless power and data transmission through both bench testing and in vivo testing using rat models. All tests successfully verified the functionality of our NeuroFlare device with its wireless system.

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