Integrated 75–100 GHz In-Band Full-Duplex Quasi-Circulator-Based Front-End GaN MMIC

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***Abstract*— This article presents a fully integrated 75–100 GHz element-level in-band full-duplex (IBFD) front-end MMIC. The MMIC is implemented in a 40-nm HEMT GaN-on-SiC process and consists of a tunable passive quasi-circulator (PQC), power amplifier (PA), and low noise amplifier (LNA). The tunable passive circulator, consisting of three Lange couplers, uses self-interference cancellation (SIC) for circulator-like performance. With tunable loads at the isolated ports in two of the couplers, this PQC demonstrates an isolation of 30 dB from transmit to receive dependent on tunable load biasing, in addition to a return loss better than 10 dB across the band for all bias levels. The passive circulator is then integrated on a chip with a three-stage PA and a three-stage LNA, with a measured system transmit gain of 13.6 dB and a receive gain of 17 dB. The fully integrated front-end demonstrates a transmit output power of 22 dBm and a receive noise figure (NF) of 5 dB.**

***Index Terms*— GaN, in-band full-duplex (IBFD), integrated front-end, low-noise amplifier, millimeter wave, MMIC, passive quasi-circulator (PQC), power amplifier (PA), self-interference cancellation (SIC).**

I. Introduction

IN-BAND full-duplex (IBFD) phased arrays have improved spectral efficiency [1], and can perform sensing and communications with the same aperture [2], [3]. However, simultaneous transmission and reception lead to high self-interference that desensitizes the receiver. In order to recover the sensitivity, self-interference cancellation (SIC) needs to be implemented. This can be done in the propagation, analog, and/or digital domains as discussed in [4]. In addition, for element-level IBFD systems, an element with circulator functionality is required to separate the transmit (Tx) and receive (Rx) signals at the antenna. The desired SIC level is determined by the transmitter output power, coupling between Tx and Rx, and the receiver noise floor. Typically, a combination of different SIC techniques is required for sufficient cancellation. For example, in [5], propagation, analog, and digital cancellation are employed for an IBFD Wi-Fi network, achieving an SIC level of 68–70 dB at 2.45 GHz. For a two-antenna element MIMO system at 3.7 GHz, [6] demonstrates an SIC level of 55–60 dB. This is done using multiple propagation domain cancellation techniques in addition to three-tap analog cancellers for each Tx and Rx path.

As frequency increases, the size of a unit element of an active antenna array decreases faster than the circuit size, and interconnects become increasingly lossy. Using a single chip integrated front-end as shown in [7] and [8] at 6 and 34 GHz, and [9], [10], [11], and [12] above 70 GHz, instead of multiple chips, helps with overall array integration. This is especially the case for monostatic IBFD systems, in which the power amplifier (PA) and low noise amplifier (LNA) share a single antenna. Integrating a passive quasi-circulator (PQC) in the front-end, as shown in Fig. 1(a), further improves functionality without adding substantial volume to the unit element. A photo of the integrated front-end MMIC can be seen in Fig. 1(b). In this approach, the output of the PA is transmitted through the PQC, with some associated loss, but isolated from the receive path LNA. The isolation is accomplished by appropriate phasing in the Tx and Rx paths.

Other approaches for IBFD front-end modules with a shared antenna element requiring Tx–Rx isolation include commonly used ferrite circulators [13], [14], [15], [16], which require bulky external magnets and are not monolithically integrated. Alternatively, active circulators [17], [18], [19] and quasi-circulators [20], [21] can be implemented on the chip, using nonreciprocity of transistors to enable circulation and isolation with gain, e.g., 2.4 dB in [19]. Integrated switch-based circulators, using switched gyrator networks, have been demonstrated in [22] and [23]. These networks can be integrated on-chip, using time-controlled transistor switch devices in the signal path, enabling circulator-like performance limited by switch insertion loss, isolation, and response time. Another approach for IBFD isolation is balanced duplexers demonstrated in [24], [25], and [26], which incorporate a single coupler with one tunable load. For more precise impedance tuning, [26] incorporates an electromechanical impedance tuner for measurements on the balanced duplexer, demonstrating an isolation greater than 40 dB at 1.9 GHz. The approach from Fig. 1(a), taken here, incorporates multiple couplers with two tunable loads, enabling more control over a wider bandwidth.

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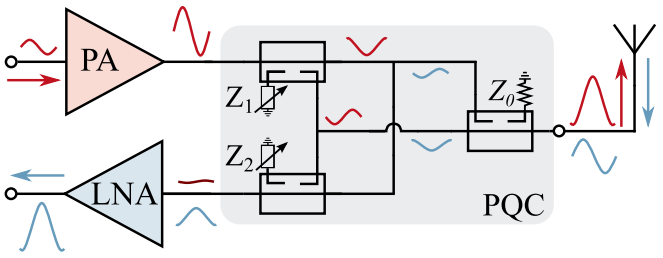
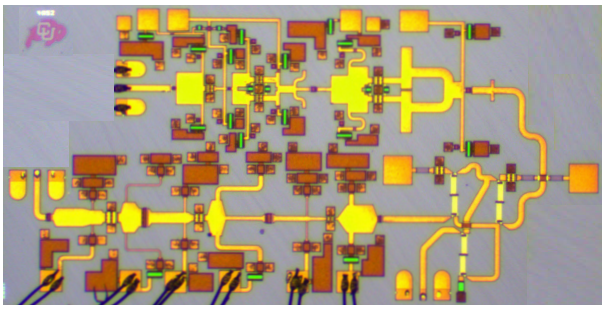


(a)



(b)

Fig. 1. (a) Block diagram of IBFD three-port front-end. The PQC network suppresses leakage from the PA to the LNA by more than 30 dB. All three components are integrated on the same GaN MMIC covering 75–100 GHz for an isolation better than 30 dB and return loss better than 10 dB. (b) Photo of the 4 × 2 mm^2 GaN MMIC die.

The quasi-circulator demonstrated in this article is a passive device amenable to monolithic integration over a wide bandwidth. We show that the Tx path does not have power limitations if active tunable devices are implemented at the isolation of the Lange couplers and not in the signal path. The device does not consume dc power and is tunable. To demonstrate this functionality, the PQC is integrated into a single MMIC with a PA and LNA for an IBFD front-end. The results in this article expand on the research presented at the IEEE International Microwave Symposium 2024, Washington, DC, USA [27]. The extension includes additional simulations and explanation of tunability, tunable load power handling capabilities, and small-signal measurements expanded to 50 GHz on the lower end of the band for the PQC and integrated front-end. In addition, large-signal measurements are performed with the separate PQC to validate that compression in the transmit path is not an issue. Furthermore, measurements of the noise figure (NF) in the receive path are performed from 75 to 110 GHz and large-signal transmit/receive integrated front-end characterization is presented.

The article is organized as follows. Section II details the design and characterization of the tunable PQC is shown, with a comparison to previous published work. Section III briefly discusses PA and LNA design for completeness, while Section IV gives final results of the transmit and receive behavior of the integrated front-end MMIC.

II. Passive Quasi-Circulator

The components and full Tx/Rx chip are designed in the HRL T3 process, featuring 40-nm GaN transistors fabricated on a 50-μm thick SiC substrate. The HEMTs have

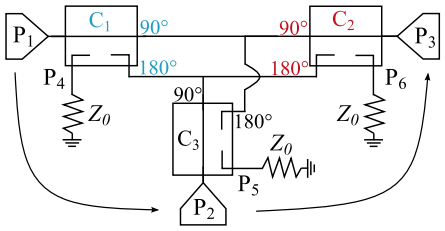


Fig. 2. PQC schematic showing the direction of circulation. The phases of the coupler outputs are indicated to show how they produce isolation.

a $f_T/f_{\max}$ = 200/400 GHz, a breakdown voltage greater than 50 V, and a power density of 1.5 W/mm [28], [29]. Transmission lines and air bridges use three metallization layers, with SiN capacitors and TaN or MESA resistors. The design of the PQC is presented next, followed by the experimental characterization of the fabricated MMIC. We note that the HRL T3 process has recently been expanded into T3L and T3.5 with improved power density and PAE at W-band [30].

A. PQC Design

A schematic of the PQC consisting of three 90° hybrids is shown in Fig. 2. The ideal phase of the *through* and *coupled* paths, referenced to the import port, are shown for each coupler in blue, black, and red, respectively. The coupler connections create a six-port network, and assuming lossless couplers and 50 Ω transmission-line connections between them, the scattering matrix is given by

$$[S]_{6\times6} = j\frac{2}{3}\begin{bmatrix} 0 & 1 & 0 & -\frac{1}{2} & 0 & 1 \\ 1 & 0 & 1 & 0 & -\frac{1}{2} & 0 \\ 0 & 1 & 0 & 1 & 0 & -\frac{1}{2} \\ -\frac{1}{2} & 0 & 1 & 0 & 1 & 0 \\ 0 & -\frac{1}{2} & 0 & 1 & 0 & 1 \\ 1 & 0 & -\frac{1}{2} & 0 & 1 & 0 \end{bmatrix}. \quad (1)$$

An input signal at P_1 is split evenly by coupler C_1, with a 90° phase between the *through* and *coupled* ports. Each signal is then split again at a T-junction, and recombined independently by couplers C_2 and C_3. Assuming 50 Ω lines, the three-port T-junctions are not ideally matched to the couplers, and this results in waves reflected back to the isolated coupler ports. The *through* and *coupled* ports from coupler C_1 connect to the same ports of C_2. They combine destructively at P_3 and constructively at P_2. Due to signal splitting, a 3 dB loss occurs from P_1 to P_2. There is also constructive combining at P_6, which can be terminated. The network operates similarly when a signal is an incident at P_2, thus a 3 dB loss is also experienced from P_2 to P_3.

Fig. 1(a) illustrates the signals when this network is used in a transmit–receive front end, with relative amplitudes shown. For IBFD operation, only three of the ports are used for Tx, Ant, and Rx, respectively, while the remaining ports are terminated. With P_1, P_2, and P_3 corresponding to Tx, Ant, and

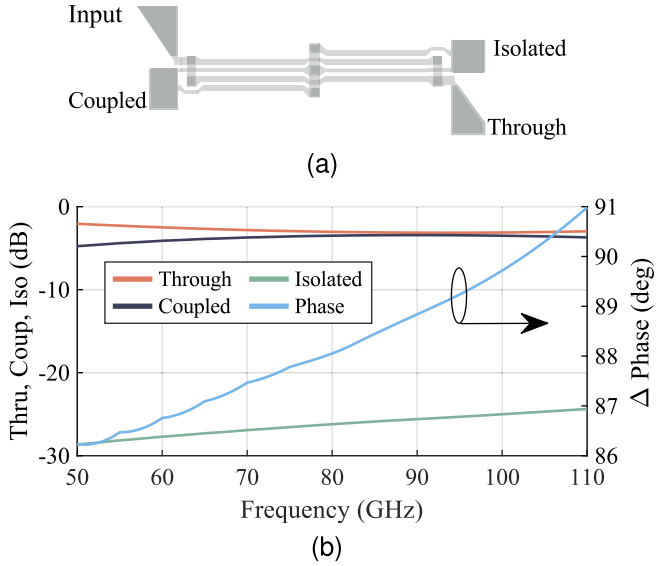


Fig. 3. (a) Layout of 375 × 140 μm^2 Lange coupler. (b) Simulated performance of Lange coupler across frequency with a Z_0 termination at the coupled port.

Rx, and with remaining ports terminated, a three-port PQC scattering matrix results

$$[S_{\mathrm{PQC}}] = j\frac{2}{3}\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \tag{2}$$

having $|S_{31}| = 0$, infinite isolation from Tx to Rx. and insertion loss in transmit and receive paths $|S_{21}| = |S_{32}| = 2/3$ or -3.5 dB.

The PQC is implemented using Lange couplers with the layout and simulated performance across V- and W-bands shown in Fig. 3, with the isolated port terminated in Z_0. The amplitude and phase imbalance is 2.5 dB and 5° from 50–110 GHz, while the isolation and match are better than 25 dB across the frequency range. The aspect ratio of the layout is convenient for placement in an MMIC, however, the transmission-line and crossover connections required for the PQC layout add loss and phase, changing the behavior relative to the ideal case.

Waves on the lines connecting the couplers cannot experience the same phase and amplitude differences without additional meandering of the transmission lines at the nodes between couplers. This is a challenge at the W-band, where a 300 μm transmission line is approximately $\lambda/4$ long at 90 GHz in the T3 process. Fig. 4 shows the difference in amplitude and phase of the transmission lines connecting C_1 to C_2, indicated in the layout in Fig. 5(a). For ideal cancellation, the difference in amplitude and phase would be zero. However, in the layout, the transmission lines connecting the couplers differ in length. To accommodate for proper phasing with unequal routing distances, the length between C_1 and C_3 is approximately twice as long as the connections between C_2 and C_3, as displayed in Fig. 5(a). The receive path connects to C_2 with a shorter path length, minimizing the impact on NF due to loss, while the transmit path connects to C_3. The bandwidth of the network is defined for the reflection

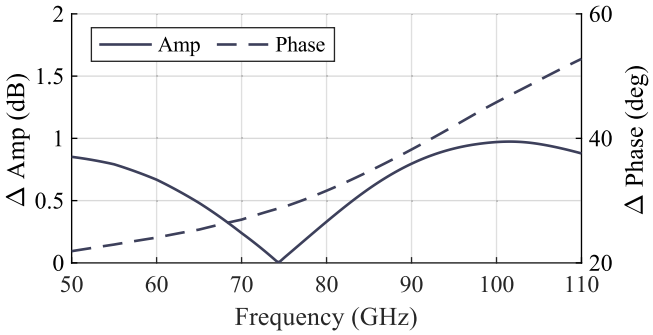


Fig. 4. Simulated difference in amplitude (solid) and phase (dashed) of transmission lines connecting C_1 and C_2 in Fig. 5(a).

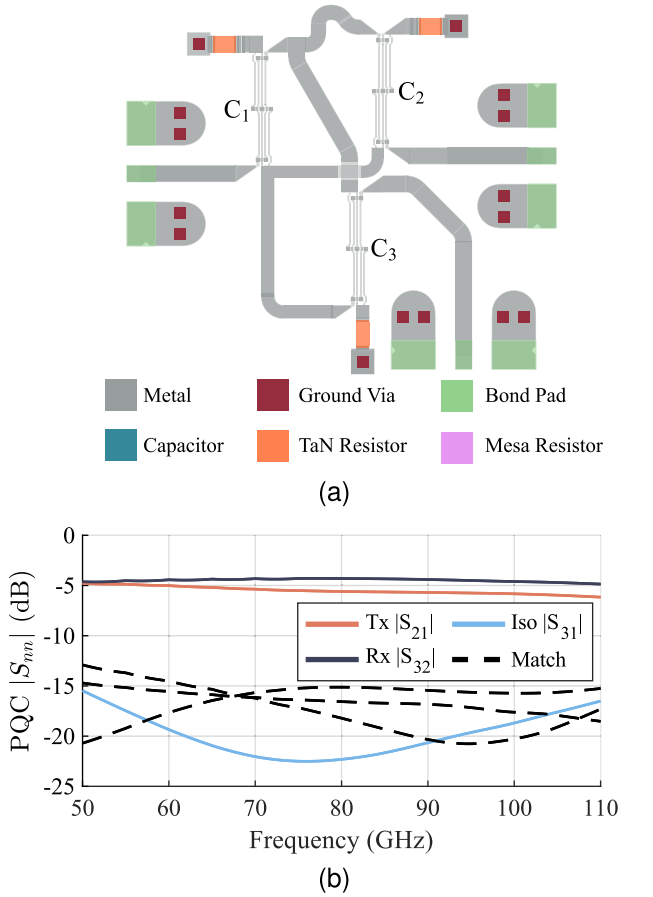


Fig. 5. (a) Layout of 1.1 × 1 mm^2 Z_0 terminated PQC. (b) Simulated circulator performance of Z_0 terminated PQC.

coefficient at all ports lower than -10 dB and the Tx–Rx tunable isolation range greater than 30 dB. Fig. 5(b) shows the simulated small-signal performance with ideal Z_0 terminations on all isolated ports of the couplers, with the maximum simulated isolation of 22 dB. For the simulated case with 50-Ω terminations, the isolation never reaches the desired level of 30 dB, motivating tunable loads added to the isolated ports of the couplers to compensate for degradation in isolation.

Tunable impedance loads in the T3 process can be realized using nonlinear HEMT devices provided by the foundry. The device models are not extracted for these specific configurations at 0 V drain bias, but are useful for predicting trends

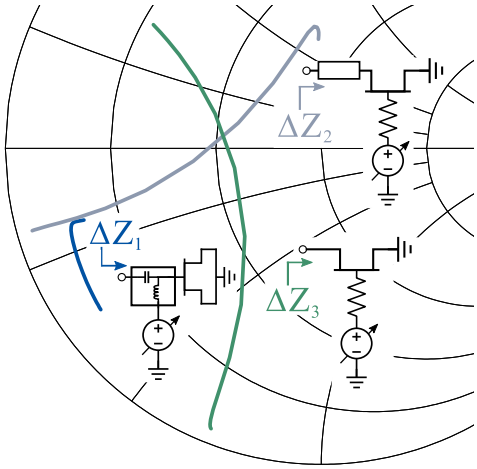


Fig. 6. Simulated impedance for different HEMT tunable load configurations. It is seen that the ΔZ_3 configuration (green) has the largest tuning range in phase combined with the simplest implementation.

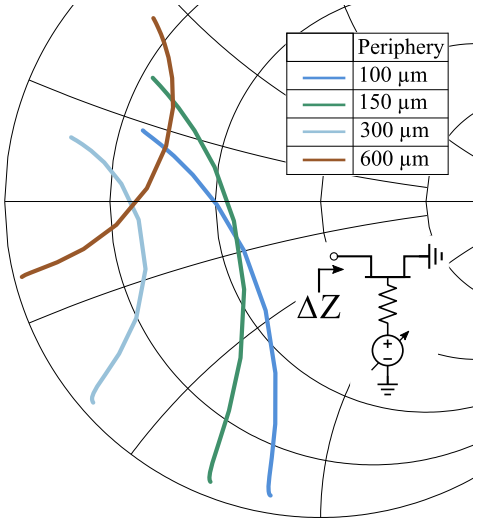


Fig. 7. Simulated impedance range of tunable load for 100, 150, 300, and 600 μm device periphery for a -1 to 1 V bias sweep. For the largest tuning range and nearest 50 Ω real impedance crossing, a 150 μm device size is chosen.

in performance. Since the tunable impedances are connected to the isolated ports of the Lange couplers, the loss of the loads is not a significant consideration. Using source-grounded HEMT devices, Fig. 6 shows three possible configurations for implementing a tunable load, with port impedances ΔZ_1 (blue), ΔZ_2 (gray), and ΔZ_3 (green). The tunable impedance of each configuration is plotted for -1 to 1 V bias sweep at 90 GHz, showing the total impedance range. Looking into the gate of the configuration ΔZ_1, simulated with an ideal bias tee, we observe the smallest impedance and the most complicated biasing structure. Both ΔZ_2 and ΔZ_3 are connected at the drain with a 100 μm transmission line added before the device in ΔZ_2, showing how the impedance of the device can be shifted. Both ΔZ_2 and ΔZ_3 have a much wider impedance range than ΔZ_1 along with a simpler biasing structure.

Comparing ΔZ_2 and ΔZ_3, and focusing on size and complexity in addition to impedance range, we note that both impedance traces cross the real axis, ΔZ_2 at ≈25 Ω and ΔZ_3 at ≈30 Ω. Taking the bias extremes at ±1 V, the impedance ranges become $\Delta Z_2 = 35 + \text{j}39\ \Omega$ and $\Delta Z_3 = 12 + \text{j}50\ \Omega$, with ΔZ_2 showing a larger amplitude difference and ΔZ_3 a larger phase difference. ΔZ_3 configuration is chosen for the tunable load for its smaller footprint and larger phase change. The variable load impedance is plotted for different device peripheries across bias in Fig. 7. The 150 μm periphery, realized with a 4 × 37.5 μm device, is chosen for the tunable load because it has the largest impedance range.

For large input signals, the nonlinear device impedance changes, degrading the performance of the tunable load. Setting a threshold impedance change of 5 Ω, the maximum power is determined. For the 4 × 37.5 μm device, Fig. 8 shows the real and imaginary parts of the impedance at $V_g = -1$, 0, 0.2, and 1 V bias across input power. Shown with a light blue trace, the impedance at 0 V shows the lowest tolerance to input power: at 7 dBm the real part of the impedance changes by 5 Ω. This bias point is the most sensitive, since the next 5 Ω change happens at 18 dBm (more than ten times the power).

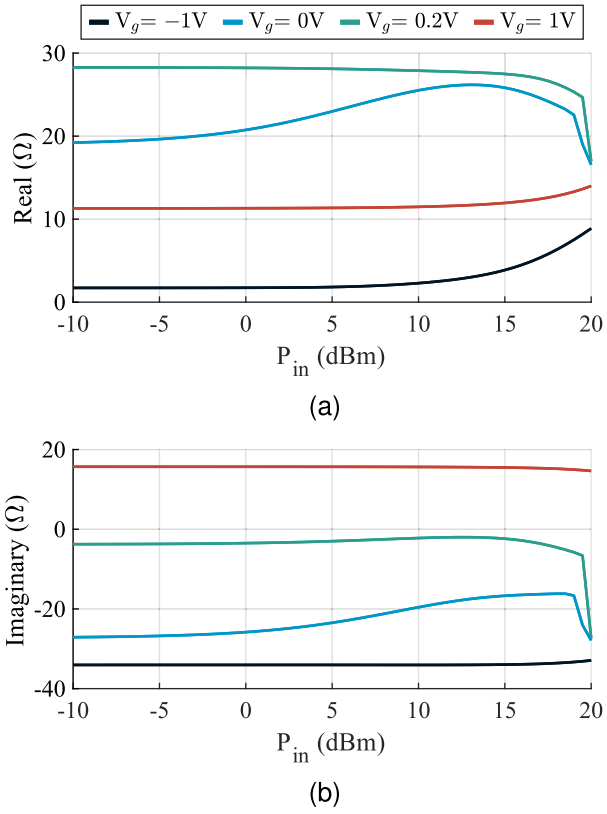


Fig. 8. Simulated (a) real and (b) imaginary parts of the tunable load impedance of a 4 × 37.5 μm (150 μm periphery) device across input power with $V_g = -1$, 0, 0.2, and 1 V.

To compensate for degradation in isolation due to interconnecting line lengths and other nonidealities, the isolated ports of two of the couplers (C_1 and C_2) are terminated with tunable loads, while the third coupler (C_3) isolated port is terminated in a 50 Ω resistor. This enables recovering isolation across frequencies based on the tunable-load bias. A plot of the simulated tunable range from 60 to 110 GHz is displayed

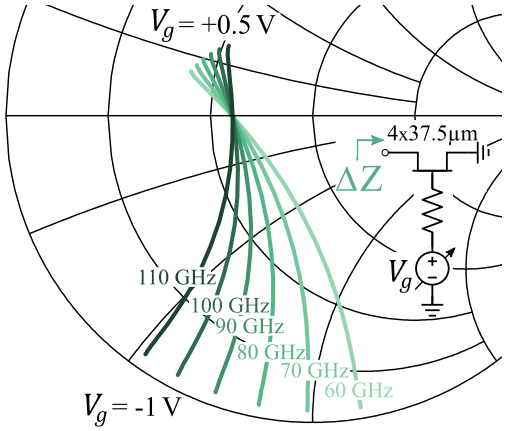


Fig. 9. Simulated impedance variation across gate bias from −1 to +0.5 V looking into the drain of a 4 × 37.5 μm device from 60 to 110 GHz.

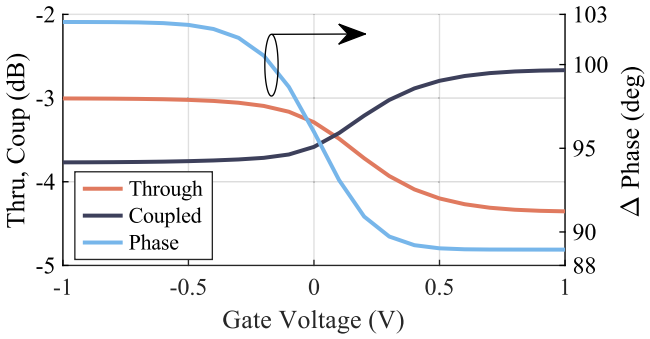


Fig. 10. Simulated performance of Lange coupler with tunable impedance connected at the isolated port at 91.5 GHz versus bias voltage of the tunable load. The *through* and *coupled* traces show the transmission coefficient. The phase trace is the relative phase difference between the two ports. Note the significant change of all parameters for a control voltage of −0.5 and +0.5 V.

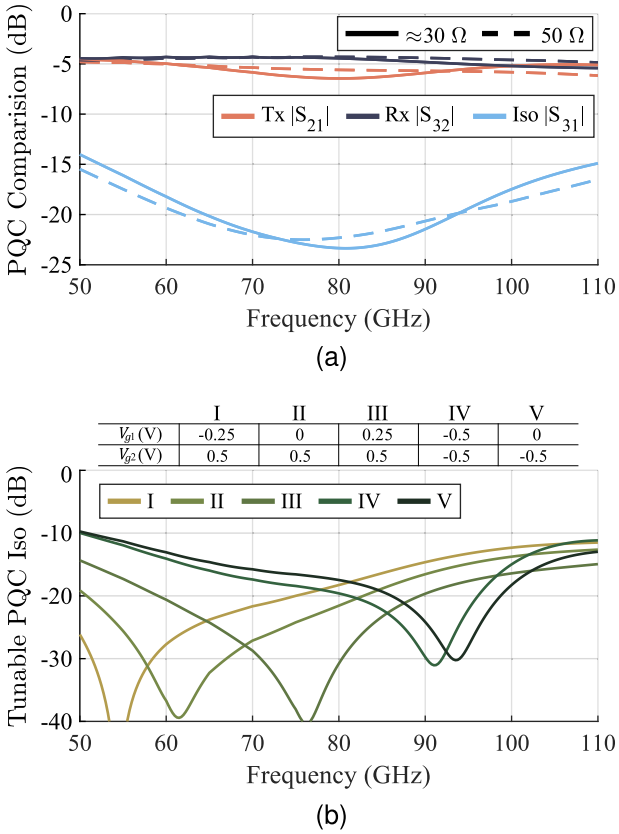


Fig. 11. (a) Simulated performance comparison of PQC with implemented tunable loads (solid) and 50-Ω terminated (dashed) PQC. The tunable loads are biased at 0.2 V for ≈30 Ω impedance presentation. (b) Simulated PQC isolation using the implemented tunable loads.

in Fig. 9. When the HEMT is pinched off, it appears purely capacitive. With the gate voltage at approximately +0.2 V, the impedance is purely real across frequency. At this bias point, the impedance is ≈30 Ω and is reasonably well matched to the 50 Ω coupler. Beyond this voltage, the HEMTs appear inductive.

With tunable loads added to the isolated port of the couplers, the coupling coefficient and the phase differences vary across bias. This can be seen in Fig. 10, which shows the simulated performance of the coupler at 91.5 GHz while the bias of the tunable load is varied from −1 to +1 V. The amplitude for both the through and coupled path varies more than 1 dB while there is a 13.5° change in phase. The most significant change in amplitude and phase happens from −0.5 to +0.5 V, which is used as the bias range during measurement.

Fig. 11(a) shows a comparison between the 50-Ω terminated PQC from Fig. 5 (dashed lines) and the PQC with tunable load terminations (solid lines) from 50 to 110 GHz. The plot shows a slight degradation in both Tx and Rx with an improvement in isolation around 80 GHz. Using the implemented tunable loads, Fig. 11(b) demonstrates multiple PQC isolation levels greater than 30 dB across frequency, a significant improvement over the 50-Ω case. Consistent with Fig. 10, the tunable load bias ranges from −0.5 to +0.5 V, where the most significant tunability occurs.

For large input signals, the power at the tunable loads compared to the input signal is reduced as the Lange coupler isolation is increased. Fig. 12 shows the power seen by the tunable load through the Lange coupler to the isolated port (P_{TL}) across bias at 90 GHz. From Figs. 8 and 12, the simulated maximum allowable input power of the PQC can be determined. Using a 0 V tunable load bias, which has the lowest power handling (see Fig. 8), the input power to the device should remain below 7 dBm. From Fig. 12, with a 0 V tunable load bias the device sees about 25 dB less power than the input signal to the Lange coupler, implying that the PQC has a simulated maximum input power of 32 dBm.

The implemented tunable PQC schematic with the Tx (red) and Rx (blue) signal paths are shown in Fig. 13(a) and (b), respectively. The two active devices in the network are only used for impedance tuning and are not in the signal path, they are in reverse bias and do not draw current, therefore we consider this network to be passive. The labeled layout of the tunable PQC MMIC is shown in Fig. 13(c) with a size of 1.1 × 1.1 mm^2.

B. PQC Measurements

The measured small-signal isolation of the PQC is shown in Fig. 14 for a range of control voltages given in Table I. The simulated performance of the PQC network is plotted for the voltages on both tunable load device gates of 0 V,

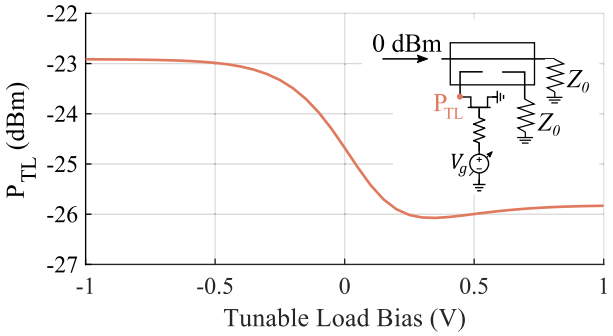


Fig. 12. Simulated power through the Lange coupler to the isolated port at the tunable load input (P_{TL}) across bias with a 0 dBm input power at 90 GHz. The tunable load power handling requirement is reduced with increased isolation of the Lange coupler.

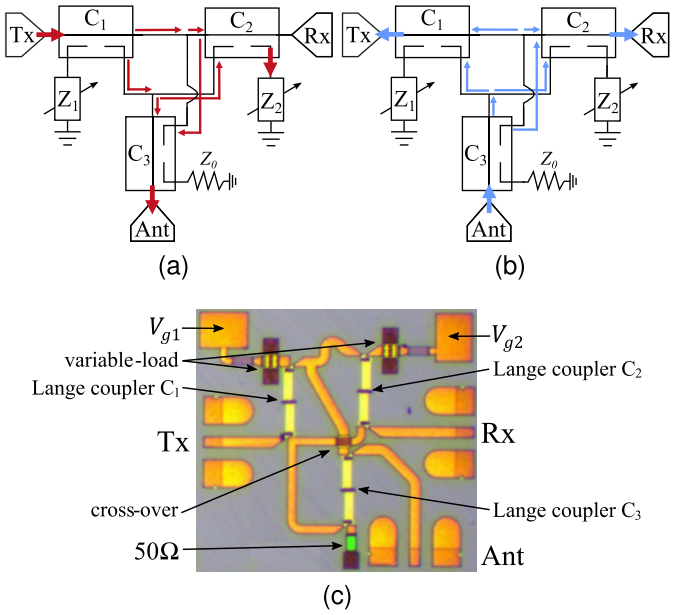


Fig. 13. Tunable PQC schematic for (a) Tx and (b) Rx signal paths, with inherent 3 dB loss in both paths. (c) Photograph of GaN MMIC PQC with a size of 1.1 × 1.1 mm^2, including RF and dc pads. The GSG pads at the RF ports have a 100 μm pitch.

TABLE I
TUNABLE LOAD BIAS FOR AN ISOLATION NOTCH < 30 dB

Trace	I	II	III	IV	V
V_{g1} (V)	0.25	0.5	0.5	0	0.4
V_{g2} (V)	0.5	0.25	0.15	0	0
Notch (GHz)	72 - 74	78 - 80	84 - 88	89 - 93	95 - 100

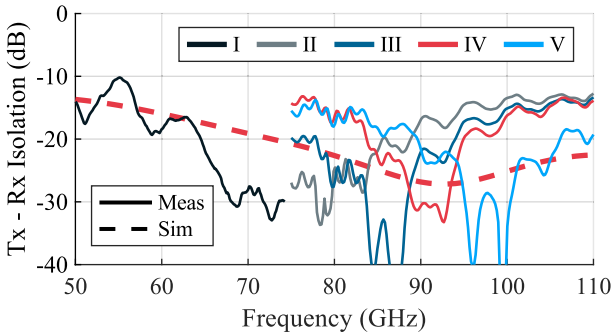


Fig. 14. Measured (solid) and simulated (dashed) Tx–Rx isolation notch of tunable PQC. In the simulation, the control voltage is held at 0 V. For the measurements, cases I–V correspond to control voltages from Table I.

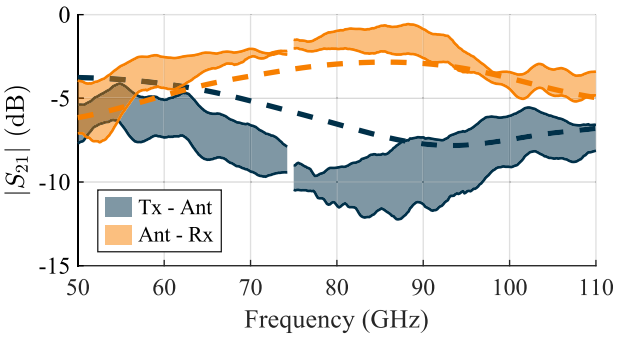


Fig. 15. Measured (solid) and simulated (dashed) characterization of PQC network. $|S_{21}|$ between Tx-Ant and Ant-Rx. The shaded region shows measurements when the gate control voltage is varied from ±0.5 V for both paths, showing the extreme values in the solid line. In the simulations, the control voltage is held at 0 V.

shown with a dashed red trace. This simulation is comparable to the measured trace $I - V$, shown with a solid red line. Simulation and measurement show a similar trend but clearly differ in isolation level, a result of the foundry HEMT devices lacking a validated 0 V drain bias model. From Fig. 14, it is seen that a notch below −30 dB is tunable within the operating frequency of the front-end for all measured control voltages. The interference cancellation is below 12.5 dB for the rest of the band. Gate voltages between 0 and 0.5 V are applied to move the notch within the frequency range. The notch center frequencies and bandwidths for each control voltage combination are given in Table I, demonstrating the upper and lower frequency range of tunable isolation with the implemented tunable loads.

The transmission between Tx-Ant and Ant-Rx ports is plotted in Fig. 15, where Tx-Ant is shown in gray and Ant-Tx is shown in orange. The shaded regions represent the range across bias when the voltages applied to the two gate pads are varied ±0.5 V to give the extremes of coupler tunability (see Fig. 10). To demonstrate the range of $|S_{21}|$, Fig. 15 plots the maximum and minimum transmission coefficient magnitude for any bias at a given frequency point. Simulation of $|S_{21}|$, shown with dashed traces, are done with a 0 V bias on both tunable loads. As predicted by simulation, the transmit path experiences the largest loss. A maximum insertion loss difference is measured between the two paths at 86 GHz, while they cross at 63 GHz when $|S_{21}| = -4.4$ dB. Simulations agree well with measurements above 90 GHz. Below this frequency, the simulated and measured transmission coefficients differ by as much as 3 dB, although the trends are predicted. Again, we attribute the differences between simulations and measurements to the HEMT model which does not accurately represent the tunable loads.

The return loss at the antenna (Ant) port is plotted in Fig. 16. For IBFD systems, return loss at the antenna can have a significant impact on performance. Namely, the transmit (Tx) signal can be reflected at the antenna port and then fed into the receive (Rx) chain, lowering Tx–Rx isolation.

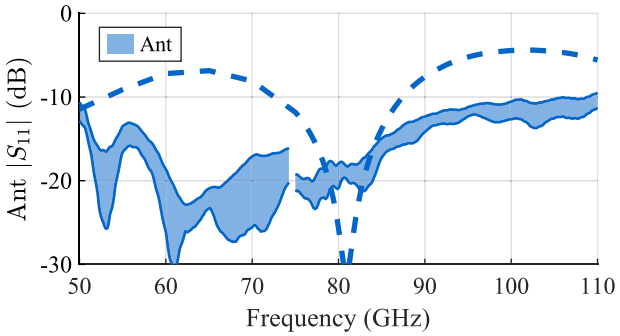


Fig. 16. Measured (solid) and simulated (dashed) match of tunable PQC at the antenna (ANT) port. The shaded region shows the measurement over a range of control voltages.

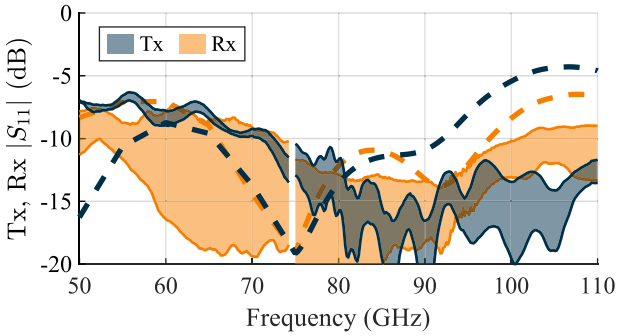


Fig. 17. Measured (solid) and simulated (dashed) match of tunable PQC at the transmit (Tx) and receive (Rx) ports. The shaded region shows the measurement over a range of control voltages.

Since reflections internal to the chip cannot be measured, the antenna port match can be quantified from the reflection coefficient at Port 3 when a 50 Ω antenna is attached to the port. Again, the measurement is done with the tunable load bias swept ±0.5 V for the most significant performance variation. The measurements show a return loss better than 10 dB at the antenna from 50 to 100 GHz across tunable load bias, which is shown as the shaded region in blue. Simulated performance with 0 V bias on both tunable loads is shown with a dashed line, having a narrowband return loss better than 25 dB at 80 GHz.

The reflection coefficients at the Tx and Rx ports are shown in Fig. 17, with the same tunable load bias sweep as in previous measurements. From 75 to 100 GHz, the return loss is better than 10 dB for all tunable load impedances, defining the bandwidth of the PQC. This is seen by the shaded region in gray (Tx) and orange (Rx). As expected, the return loss for both of these ports varies more with tunable load bias, due to the mismatched isolated port of the couplers.

For a demonstration of the PQC power handling, the transmitted power between the Tx and Ant ports is measured with an input power swept from 14 to 24 dBm at the Tx port, with the upper end limited by our driver amplifiers in the W-band. For on-wafer measurements, the tunable loads are wire-bonded to the ground for a bias of 0 V, reducing the number of required probes in the on-wafer measurements. The tunable loads are the only active devices in the PQC, potentially limiting the power handling, and a 0 V bias presents the most conservative condition. Measurements are done in 1 GHz steps

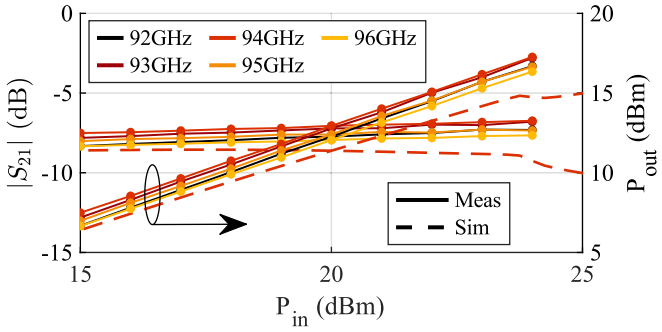


Fig. 18. Measured (solid) and simulated (dashed) large signal power sweep of PQC transmit path across frequency, with 0 V on tunable load bias. The Rx port is terminated in a matched load.

from 92 to 96 GHz, with results shown in Fig. 18 along with the simulated power handling of the PQC at 94 GHz. The measurements show no compression of the PQC up to the available input power of 24 dBm while simulations show compression slightly below 24 dBm.

The frequency of operation for the PQC, 75 to 100 GHz, is defined by a tunable SIC better than 30 dB and a return loss better than 10 dB at all ports. Across the frequency of operation, the insertion loss is averaged for both Tx and Rx to determine the loss of the PQC. Table II compares the performance of the PQC to other circulator-like networks, showing high frequency of operation, no dc power consumption, and high isolation, at the expense of insertion loss in Tx.

III. Integrated Full-Duplex Front-End

The PQC is combined into a single-chip transceiver MMIC as a proof of concept integrated analog front-end. A three-stage PA is integrated with a three-stage LNA and a tunable PQC that enables shared antenna IBFD operation. The layout of the full, 4 × 2 mm^2 chip, is given in Fig. 19. The three-stage PA is at the top, with the input denoted by Tx, and was separately characterized with results given in [31]. This reactively-combined PA has over 12 dB of simulated gain from 75 to 110 GHz, and 27 dBm of output power at an input power of 15 dBm. The PA output is fed to the PQC network, shown at the bottom right. The second port of the PQC is connected to the antenna GSG probe (Ant). The third port of the PQC network is connected to a three-stage LNA with a 50-Ω microstrip line. A photograph of the fabricated MMIC is shown in Fig. 1(b). A 50-Ω load GSG resistor is included in the layout close to the Tx and Rx GSG pads and bonded when needed so that the ports can be terminated without an additional probe. The resistors are not shown in the MMIC photograph [see Fig. 1(b)] or layout (see Fig. 19) for clarity.

Due to the full-duplex implementation, the peak PA output power and minimum isolation are of concern when considering the linearity of the LNA. Compression of the LNA degrades the linearity and limits the effectiveness of additional SIC later in the receive chain. A high compression level is a benefit of GaN LNAs [32], further making full Tx–Rx integration advantageous.

The 75–100 GHz LNA has three stages for sufficient receiver gain when the approximately 3 dB loss of the PQC

TABLE II
TUNABLE PQC COMPARISON TABLE

Reference	Technology	Frequency (GHz)	Insertion Loss (dB)	Isolation (dB)	DC Power (W)	P1dB (dBm)	Area (mm^2)
[14]	Ferrite	55 - 66	1	15	0	54	11
[17]	GaN	50 - 100	6.3	20	1.5	16	4.5
[20]	GaAs	10 - 12	4.5	35	0	35	8
[21]	SiGe	76 - 80	1	16	0.06	1	0.07
[22]	CMOS	0.9 - 1	2.5	30	0.17	30.5	16
[24]	PCB	2.5 - 2.8	3/4	25	0	-	-
This Work	GaN	75-100	9.5 Tx / 2.5 Rx	> 30	0	> 24	1.1

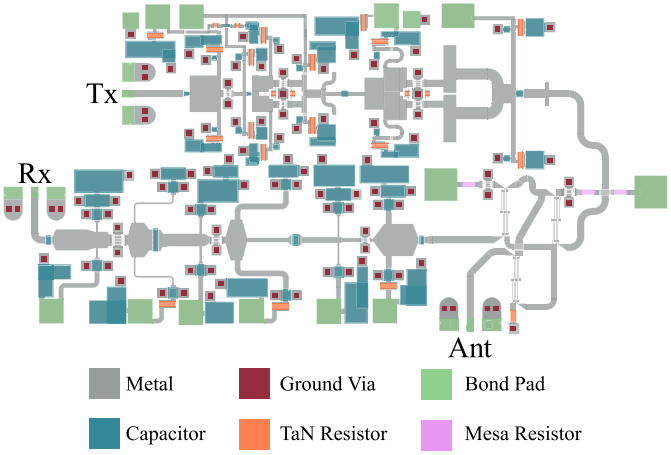


Fig. 19. Layout of the 4 × 2 mm^2 integrated full-duplex front-end GaN MMIC. A three-stage PA is on the top, while the LNA is on the bottom and the PQC network is between the output of the PA and the antenna port, with the third port connected to the LNA input.

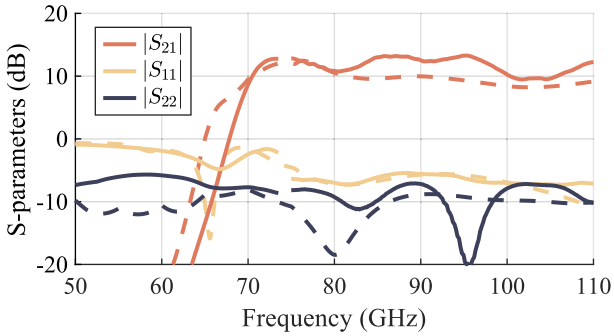


Fig. 20. Measured (solid) and simulated (dashed) small-signal characterization of front-end transmit path. Measurements and simulations are shown for 0 V bias on both tunable loads.

network is included. While the decrease in gain can be overcome by additional gain stages, the NF suffers. Placing an emphasis on NF, the smallest device with a validated model of 2 × 25 μm, giving the lowest NF of 2.1–2.7 dB from 75 to 100 GHz, is chosen for the first LNA stage. In stages two and three, the next largest validated devices of 4 × 37.5 μm and 6 × 50 μm are used, with an NF of 2.5 and 2.7 dB at 90 GHz. For stability, large shunt capacitors on the bias line in addition to low resistance are added, reducing gain at lower frequencies. Bias lines of each stage are separated for individual control of drain current for each stage if desired. The LNA has a simulated gain of 15.5–16.5 dB, an NF ranging from 3.5 to 3.9 dB from 75 to 100 GHz, and a P1dB of 1 dBm at 91 GHz.

IV. MEASURED FULL-DUPLEX FRONT-END

The front end is mounted on a gold-plated copper-molybdenum (CuMo) carrier, and the dc pads are wire-bonded with 1-mil gold bond wire to off-chip capacitors for stability. The circuit is measured on a Summit 9000 probe station with 100-μm pitch GSG probes and characterized in small-signal operation from 50 to 75 GHz, then 75 to 110 GHz using an HP8510C Vector Network Analyzer with V- and W-band extender heads, respectively. Network calibration for V- and W-band were done separately with on-wafer SOLT calibrations. The integrated front end is next measured in transmit and receive modes with the unused path unbiased and terminated with an on-chip load. A resistor is included in the layout close to the GSG pad and bonded when needed to the microstrip. The resistors are not shown in the layout for clarity. The bias on both tunable loads of the PQC is set to 0 V for both transmit and receive measurements. The operational bandwidth of the full-duplex front-end is determined by the return loss better than 5 dB and a 3 dB drop from the maximum gain.

A. Transmit Path Performance

The small-signal measured (solid) and simulated (dashed) transmit path parameters are displayed in Fig. 20. The measurements are carried out with the gate and drain bias of the PA tied together using off-chip capacitors, at a drain voltage of 12 V and a total drain current of 100 mA. The measured small-signal gain from 70 to 100 GHz ranges from 10.5 to 13.5 dB, which is up to 5 dB higher than the simulation at 95 GHz. Note that we observe an increase in gain at the higher end of the band at 110 GHz. The measured return loss is better than 5 dB above 75 GHz.

The 92–96 GHz large-signal setup is shown in Fig. 21. The measurements are conducted using a Keysight N5183B signal generator with an MI-Wave frequency multiplier and an MI-Wave 511 programmable attenuator, amplified by a QuinSTAR SSPA. The output of the SSPA is connected to a WR-10 waveguide bidirectional coupler that measures the incident wave with a WR-10 power sensor. Following this are WR-10 waveguide GGB GSG RF probes connected to the device under test (DUT). The output signal is then fed into an attenuator and a WR-10 power sensor.

Large signal measurements and simulations of the transmit path are shown in Fig. 22. The measurement is performed

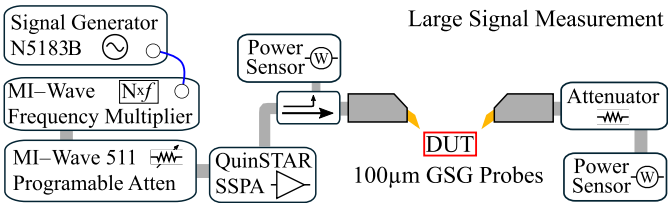


Fig. 21. Block diagram of the large-signal measurement setup.

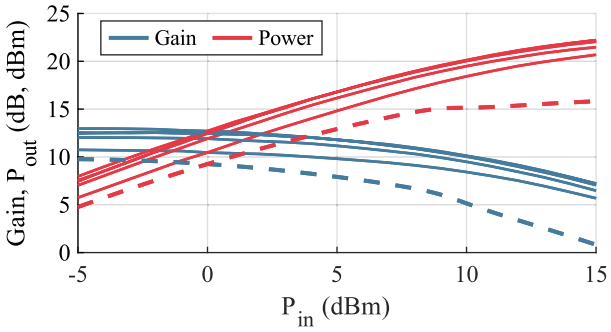


Fig. 22. Measured (solid) and simulated (dashed) large-signal characterization of transmit path. Measurements are shown from 92 to 96 GHz in 1 GHz steps and simulations are shown for 94 GHz. The measurements and simulations correspond to 0 V bias on both tunable loads.

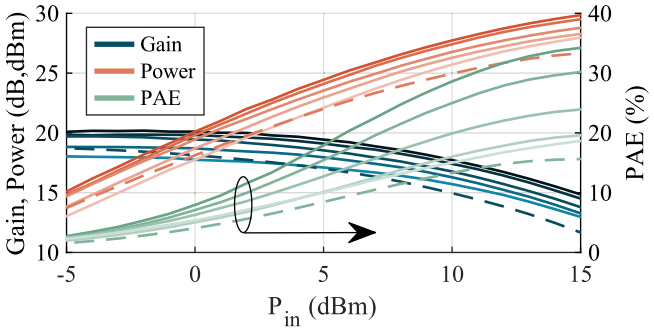


Fig. 23. Measured (solid) de-embedded PA from 92 to 96 GHz in 1 GHz steps from light to dark coloring and simulated (dashed) PA at 94 GHz. The PA is de-embedded with the large signal $|S_{21}|$ measured data in Fig. 18.

with an input power from −5 to +15 dBm across 92 to 96 GHz in steps of 1 GHz, shown in a solid line, while simulations are done at 94 GHz (dashed). The measured gain and output power are higher than simulation, as expected from small-signal measurements in Fig. 20 which are larger than simulated ones from 92 to 96 GHz. With an input power of 15 dBm, the transmit path demonstrates an output power of 22 dBm and a gain of 7 dB at 96 GHz.

Taking into account the PQC loss in the transmit path (see Fig. 18), the de-embedded measured (solid) large signal performance of the PA is shown in Fig. 23. The PA demonstrates a maximum output power of 30 dBm, remaining below the allowable input power to the PQC, and a peak PAE of 35% at 96 GHz. We note that the simulated standalone PA performance, shown at 94 GHz in the dashed line, is consistently lower across frequency than the measured performance. The small-signal measurements were done at two independent facilities with excellent agreement.

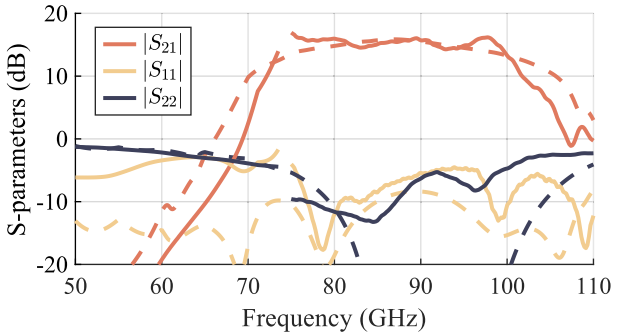


Fig. 24. Measured (solid) and simulated (dashed) small-signal characterization of receive path. The measurements and simulations are shown for 0 V bias on both tunable loads.

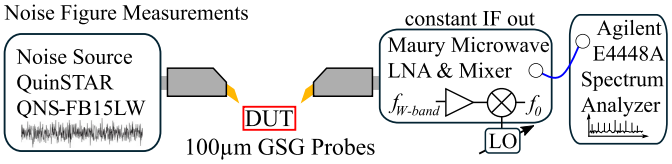


Fig. 25. Block diagram of on-wafer NF measurement setup using a fixed-IF topology with a QuinSTAR noise source and Maury Microwave LNA and mixer.

We attribute the improved measured performance to process improvements [30].

B. Receive Path Performance

The measured performance in receive mode is seen in Fig. 24. Both simulations and measurements are performed with gate and drain biases tied together, at a drain voltage of 12 V and a combined drain current of 95 mA. The measurements show a small-signal receive gain of 17–14 dB and input and output return losses better than 5 dB from 75 to 100 GHz. Based on the transmit and receive small signal measurements, the full-duplex single-chip analog front-end demonstrates a 25 GHz or 28.6% bandwidth from 75 to 100 GHz.

A diagram of the W-band NF measurement setup is shown in Fig. 25. The measurements are conducted using a Quinstar QNS-FB15LW WR-10 waveguide noise source feeding a WR-10 waveguide-to-GSG RF probe adaptor connected to the DUT. A Maury Microwave LNA/mixer combination is used for downconversion, with the LO varied for a constant IF frequency, measured with an Agilent E4448A Spectrum Analyzer NF personality option. This measures the raw NF, and the *S*-parameters of all of the components are characterized for postprocessing and correction.

The NF of the receive path is measured from 75 to 110 GHz, in 5 GHz steps, as seen in Fig. 26. The simulated performance of the receive path (blue) and LNA (red) are also plotted for comparison. The receive path has a measured minimum NF of 5 dB at 80 GHz, which aligns well with the simulated receive path NF of 5.5 dB at 80 GHz. The measured NF follows a similar trend to the simulated receive path NF across frequency, with a deviation at 110 GHz.

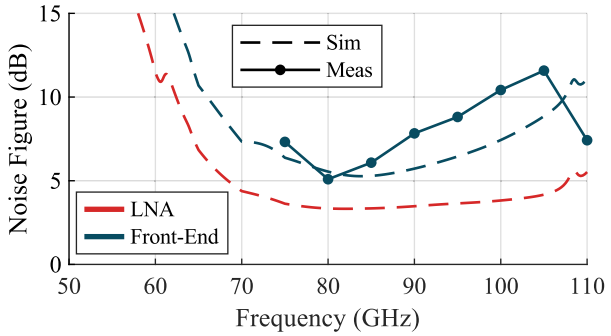


Fig. 26. Measured (solid) and simulated (dashed) NF of receive path with 0 V bias on both tunable loads. The simulated NF of the LNA alone is shown in red.

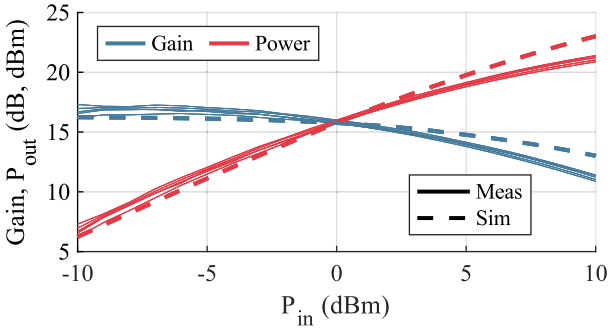


Fig. 27. Measured (solid) and simulated (dashed) large-signal characterization of receive path. Measurements are shown from 92 to 96 GHz in 1 GHz steps and simulations are shown for 94 GHz for 0 V bias on both tunable loads.

TABLE III
COMPARISON OF W-BAND INTEGRATED FONT-END GAN MMICS

Ref.	Freq. (GHz)	Duplex (Full/Half)	P_{out} (dBm)	NF (dB)	Area (mm^2)
This Work	75-100	Full	22	5-11	8
[9]	71-77	Half	30.6-31.5	4.7-5.5	10.75
[10]	75-110	Half	29	5.2-7.8	15
[11]	100-110	Half	30	6-6.4	19
[12]	75-86	Half	> 27	4.5	6.375

Receive path large-signal measurements and simulations are shown in Fig. 27. Measurements are performed with an input power from -10 to 10 dBm across 92 to 96 GHz in steps of 1 GHz, shown in solid line. Simulations are done at 94 GHz, shown in dashed line. The measured and simulated data are in good agreement, having an input P1dB of 1 dBm with similar gain and output power. This is expected as the receive path small signal data in Fig. 24, line up well from 92 to 96 GHz. This high-power LNA, integrated into the full-duplex front-end, will protect the receive chain from damage and remain linear while the high-power PA is transmitting.

The large signal measurements of the Tx and Rx paths shown in Figs. 22 and 27 differ in deep compression. This is due to the PA and LNA having different staging ratios of 1:2:3 for the PA and 1:3:6 for the LNA. The PA staging ratio is motivated by a high PAE which requires the previous stages to have enough gain and power handling to saturate the final stage for peak PAE. For the LNA the staging ratio is 1:3:6, motivated by high power handling and the diminishing effect the cascaded stages have on NF. In addition, each stage of the LNA uses a validated device while the first two stages of the PA use a device scaled from a validated model.

V. DISCUSSION AND CONCLUSION

In summary, this article presents a tunable PQC which is then integrated on-chip for an IBFD analog front-end GaN MMIC from 75 to 100 GHz. The PQC network is made of three Lange couplers with tunable loads, using 4×37.5 μm HEMT devices at the isolated ports of two of the couplers. This tunability allows for greater than 30 dB of isolation from transmit to receive across the band, achieved by varying the bias of tunable HEMT loads. The PQC demonstrates a return loss of better than 10 dB across the band and does not show any indications of compression up to 24 dBm of input power. Therefore, the SIC level remains constant up to the same input power level. Furthermore, in a nonideal environment, with varying antenna impedance, simulations show the tunable loads can be used to compensate for antenna mismatch. For the designed network the average path loss in the band for Tx and Rx differ, with an Rx loss of 2.5 dB and a Tx loss of 9.5 dB. The high loss of the Tx path is a result of different signal path lengths between Lange couplers, resulting in a phase change which degrades signal recombination. In addition, the required crossover of the connecting transmission lines contributes about 2 dB of loss.

Due to the compact size, ease of integration, large bandwidth, high isolation, and high linearity, the PQC is an attractive component for integrated transmit–receive IBFD front-ends. In addition, it is frequency-scalable and does not require any dynamic biasing or dc power. The main drawback is relatively high Tx insertion loss, which could be improved if the phase difference in the transmission lines connecting the coupler is reduced. For the implemented PQC at W-band, phase compensation was done with the tunable load on the isolated ports of the couplers. In future designs, the tunable loads can be used to compensate for mismatches in applications such as phased arrays, where the antenna impedance changes with scanning.

Using the PQC integrated with a three-stage PA and LNA, to the author's knowledge, the first W-band IBFD front-end GaN MMIC is demonstrated. The transmit path shows a small signal gain ranging from 10.5 to 13.5 dB across the band, with a peak output power of 22 dBm. For receive, the front-end demonstrates a minimum NF of 5 dB and a gain ranging from 17 to 14 dB across the band. In addition, the receive path shows a measured input P1dB of 1 dBm, allowing full-duplex operation without damage or compression of the receive chain. The PQC that enables full-duplex operation comes at the cost of additional loss, and therefore the output power of the presented front-end is lower than the compared half-duplex front-end MMICs. A comparison of W-band integrated switchable front-end T/R GaN MMICs is shown in Table III, for the closest comparison to the presented front-end MMIC. The table shows competitive performance to switched front-end modules in the frequency ranging of 75–100 GHz with a total area of 8 mm^2.

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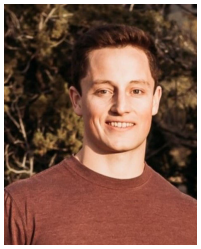

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