

Nonlinear Capacitance-Based Accurate ZVS Analysis for Full-Bridge T-Type Resonant Converters

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Abstract—To optimize the utilization of a T-type bridge structure in resonant converters, one must thoroughly examine the soft-switching criteria specific to the T-type configuration. This work proposes an energy-based method to determine the soft-switching requirements of a T-type bridge during its various switching transitions. The study estimates the minimum required zero voltage switching (ZVS) current while considering the nonlinearity and voltage dependence associated with the output capacitance of MOSFETs. Moreover, this paper demonstrates that existing studies on ZVS analysis for T-type bridge-based resonant dc-dc converters, which rely only on capacitive energy considerations, significantly underestimate the necessary ZVS current values, with errors as high as 50%. Simulation and hardware results on a T-type primary bridge circuit validate the accuracy of the proposed minimum ZVS current calculation. Hardware tests are conducted on a T-type bridge in a 20 kW electric vehicle charger.

Index Terms—EV, multi-level converter, nonlinear capacitance, three-level converter, T-type converter, zero-voltage switching (ZVS), resonant converter.

I. INTRODUCTION

In recent years, T-type converter-based topologies have gained prominence in hard-switching applications like grid-tied AC-DC converters. These topologies offer enhanced efficiency and power density, particularly at high switching frequencies [1]–[4]. The design focus of these applications revolves around minimizing losses, optimizing thermal management, and ensuring the optimal commutation pattern.

On the other hand, the T-type bridge structure, as shown in Fig. 1, is increasingly being utilized in soft-switched resonant dc-dc converters because of the enhanced control flexibility offered by the three-level structure. These applications of a T-type bridge in resonant converters require a comprehensive analysis of the soft-switching requirements of a T-type structure. The state-plane analysis is one approach for analyzing ZVS conditions in resonant converters [5]. However, in the context of a T-type structure, handling a five-level full-bridge T-type output voltage, as employed in [6], significantly complicates the application of the state-plane method

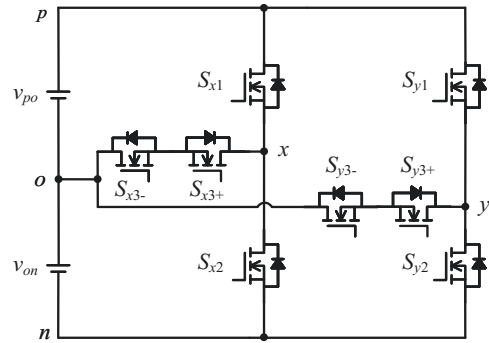


Fig. 1. Configuration of two legs in a T-type bridge circuit.

when dead-times are included as states in the state-plane analysis. Moreover, one application where the T-type bridge is utilized as a resonant converter bridge is for unfolding-based single-stage ac-dc converters [6]–[9]. The unfolding-based converter applications result in time-varying input voltages at the T-type bridge input. Consequently, zero-voltage switching (ZVS) analysis cannot rely on a constant MOSFET output capacitance (C_{oss}), as MOSFETs in the circuit exhibit nonlinear, voltage-dependent capacitances. Hence, analyzing ZVS requirements while including the effect of nonlinear output capacitance for the T-type bridge structure is of prime importance.

This work proposes an energy-based approach to determine the ZVS requirements for T-type bridges while considering the nonlinear nature of C_{oss} . It presents a generalized solution for determining the minimum ZVS current for various switching transitions within a T-type bridge. The proposed method is applicable across various modulation schemes and resonant tank circuits. Furthermore, the previous literature works [10]–[13] adopting the energy-based approach relies solely on capacitive (C_{oss}) energies. This paper demonstrates that the energy contributions from the voltage sources are not negligible. Ignoring these energy contributions and considering only capacitive energies leads to an underestimation of the minimum ZVS current requirement, with errors reaching up to 50%. Recently, the proposed method has been implemented for a T-type bridge in an unfolding-based ac-dc converter system [14]. However,

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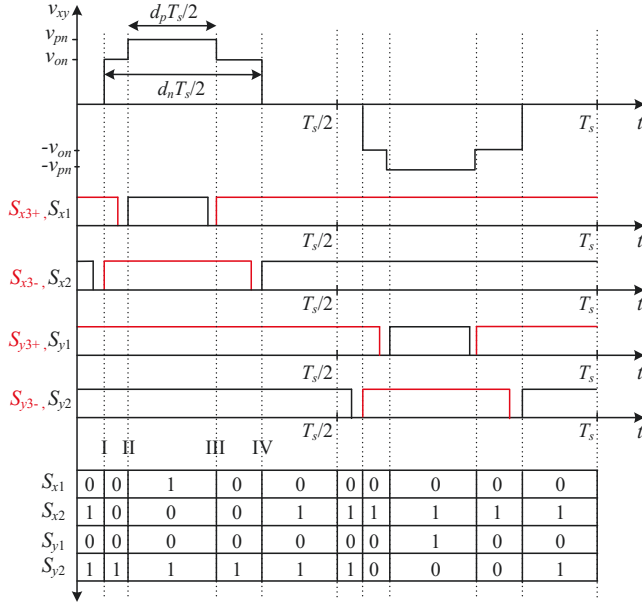


Fig. 2. Commutation sequence with zero state achieved by connecting both switch nodes to n node.

this work derives the minimum ZVS energy requirements for the H-bridge before delving into the T-type bridge for clarity. Furthermore, This work provides a simplified solution for ZVS requirements across various switching transitions in a T-type bridge, suitable for scenarios where a T-type full-bridge operates with constant input voltages.

II. CIRCUIT TOPOLOGY AND SWITCHING PATTERN

A. Circuit Topology

Fig. 1 illustrates a T-type bridge structure in a resonant converter used as a primary or secondary bridge. In addition to four H-bridge switches, a T-type bridge incorporates two series-connected common-source switches between the switch nodes (x node or y node) and the midpoint (o node) of the input dc-link, making it a three-port converter. In this paper, two voltage sources across the two input ports are denoted as v_{po} and v_{on} . A T-type bridge in Fig. 1 can also be viewed as two H-bridges in series. The switches S_{x1} and S_{x3+} establish connections between either the p or o node and the x switch node, while S_{y1} and S_{y3+} connect the p or o node to the y switch node. These four switches collectively form an H-bridge circuit, which is responsible for applying $\pm v_{po}$ voltages across switch nodes x and y . Additionally, switches S_{x2} , S_{x3-} , S_{y2} , and S_{y3-} apply $\pm v_{on}$ voltages across the switch nodes x and y . The voltage across x and y nodes is denoted as v_{xy} and the voltage across p and n nodes is denoted as v_{pn} .

B. Switching Pattern

There are numerous strategies to generate a switching pattern for a T-type bridge. As observed from Table I, there are a total of six possible active states and three possible zero states. Out of the various commutation sequences that can be

TABLE I
POSSIBLE SWITCH STATES AND CORRESPONDING OUTPUT VOLTAGE v_{xy} .

S_{x1} ($\overline{S_{x3+}}$)	S_{x2} ($\overline{S_{x3-}}$)	S_{y1} ($\overline{S_{y3+}}$)	S_{y2} ($\overline{S_{y3-}}$)	v_{xy}
0	0	0	0	0
0	0	0	1	v_{on}
0	0	1	0	$-v_{po}$
0	1	0	0	$-v_{on}$
0	1	0	1	0
0	1	1	0	$-v_{pn}$
1	0	0	0	v_{po}
1	0	0	1	v_{pn}
1	0	1	0	0

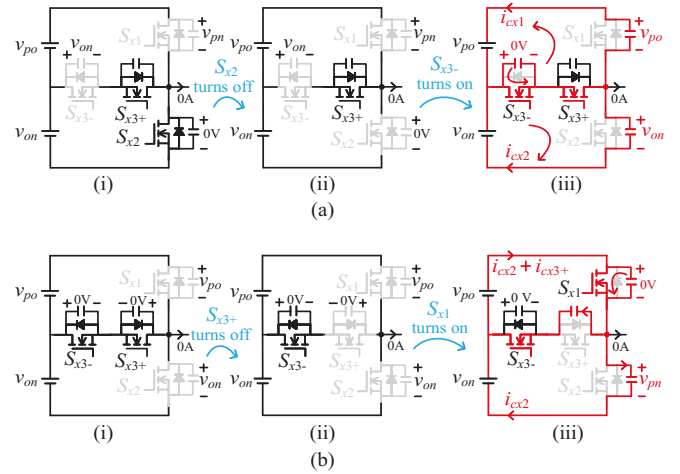


Fig. 3. A detailed commutation process involving charging and discharging of C_{oss} of MOSFETs during (a) transition I, (b) transition II. The circuits in (a) and (b) represent the time (i) before the device turns off (ii) during the dead time (iii) after the complementary device turns on.

derived from Table I, one of the commutation sequences is shown in Fig. 2, along with the T-type bridge output voltage v_{xy} . In Fig. 2, T_s denotes one complete switching period of the converter. The variables d_p and d_n represent the durations of the duty cycles during which v_{po} and v_{on} are applied at the output, respectively. Both d_p and d_n can vary from 0 to 1. In this commutation sequence, the zero state ($v_{xy} = 0$) is achieved by simultaneously keeping switches S_{x2} and S_{y2} on, connecting the switch nodes of both legs to the n node. The zero state can also be achieved by connecting switch nodes of both legs to the p node or o . The effectiveness of producing a zero state may vary depending on the specific duty cycle patterns and input voltage levels used. Comparison of various commutation patterns generated by opting for different zero states is beyond the scope of this paper.

The switching patterns depicted in Fig. 2 reveal that each T-type bridge leg undergoes four switching transitions (I, II, III, and IV). To understand the charging and discharging of MOSFET capacitances, switching transitions I and II for leg x are analyzed with zero tank current. The switching

TABLE II
CAPACITORS CHARGING AND DISCHARGING DURING DIFFERENT
TRANSITIONS.

Transition	S_{x1}	S_{x2}	S_{x3+}	S_{x3-}
I (n to o node)	v_{pn} to v_{po}	0 to v_{on}	-	v_{on} to 0
II (o to p node)	v_{po} to 0	v_{on} to v_{pn}	0 to v_{po}	-
III (p to o node)	0 to v_{po}	v_{pn} to v_{on}	v_{po} to 0	-
IV (o to n node)	v_{po} to v_{pn}	v_{on} to 0	-	0 to v_{on}

transitions III and IV are similar and they are skipped for brevity. Transition I is defined as the transition during which the switch node of leg x transitions from the n node to the o node. Similarly, other transitions are also defined as shown by Fig. 2. In Fig. 3, the switches that are turned on are shown in black, and the switches that are turned off are shown in gray. The active section of the circuit, where the current is flowing, is highlighted in red.

1) *Transition I (n to o node)*: As shown in Fig. 3(a), the switch S_{x2} initially turns off. Since there is no path for the capacitor of S_{x2} to charge during the no-load condition, the circuit remains unchanged in Fig. 3(a)(i) and (ii). After the dead time, S_{x3-} turns on, and its output capacitor discharges through its own channel. This also allows the output capacitor of S_{x2} to charge from 0 to v_{on} . Simultaneously, switch S_{x1} , which is already off, discharges from v_{pn} to v_{po} .

2) *Transition II (o to p node)*: As shown in Fig. 3(b), switch S_{x1} discharges completely from v_{po} to 0, connecting the switch node x to p node. Switch S_{x3+} charges from 0 to v_{po} , and switch S_{x2} charges from v_{on} to v_{pn} . It is crucial to note that despite the switch S_{x2} remaining off during transition II, it continues to charge. Therefore, an additional commutation loop is present in the case of a T-type converter, which can not be ignored during the estimation of switching losses. This observation holds true for all other transitions as well.

Table II summarizes the changes in capacitor voltages for these four transitions, which play a crucial role in determining ZVS requirements. Before delving into this discussion, the following section will concentrate on deriving the energy and charge equivalent values for the MOSFET's C_{oss} , which will be utilized in Section IV.

III. REVIEW OF CIRCUIT ORIENTED TREATMENT OF MOSFET'S NONLINEAR OUTPUT CAPACITANCE

The output capacitance of a MOSFET, denoted as C_{oss} , is a nonlinear function of the drain-to-source voltage (v_{ds}). This voltage dependence varies among different semiconductor technologies and different manufacturers' device implementation techniques, as illustrated in Fig. 4 for devices rated for 650 V, 30 A. It is often challenging to fit all these curves with a general empirical formula. Thus, defining an equivalent capacitor that provides the same charge or energy for a specific voltage change becomes highly beneficial. As the non-linearity can not be correctly modeled in terms of time, energy, and charge simultaneously using a single linear capacitor, the

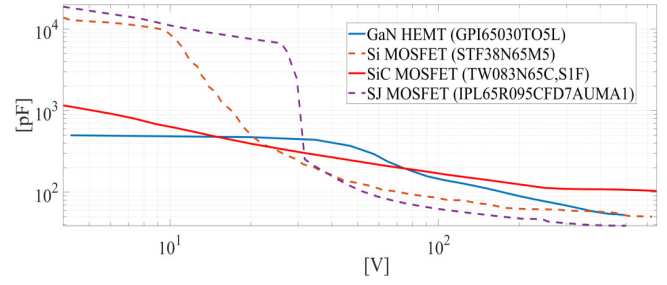


Fig. 4. Variation of output capacitance of MOSFET (C_{oss}) with drain to source voltage (v_{ds}).

energy equivalent capacitor denoted by $C_{eq,E}$, and charge equivalent capacitor denoted by $C_{eq,Q}$ are introduced [15]. These charge and energy equivalent capacitors are

$$C_{eq,Q} \Big|_0^{v_c} = \frac{1}{v_c} \int_0^{v_c} C_{oss|v} dv, \quad (1)$$

$$C_{eq,E} \Big|_0^{v_c} = \frac{2}{v_c^2} \int_0^{v_c} v C_{oss|v} dv. \quad (2)$$

Here, the energy stored in energy equivalent capacitor $C_{eq,E}$ at voltage v_c is the same as energy stored when the capacitor $C_{oss|v}$ voltage changes from 0 to v_c . Similarly, the charge stored in charge equivalent capacitor $C_{eq,Q}$ at dc voltage v_c is the same as the charge stored when charging the capacitor $C_{oss|v}$ from 0 to v_c , where v_c can be any value from 0 to rated operating voltage of the MOSFET as shown in Fig. 4.

To compute the charge-equivalent capacitance in the scenario where the capacitor is charging from v_1 to v_2 , the initial step involves calculating the total charge, given as

$$\begin{aligned} Q_c \Big|_{v_1}^{v_2} &= \int_0^{v_2} C_{oss|v} dv - \int_0^{v_1} C_{oss|v} dv, \\ Q_c \Big|_{v_1}^{v_2} &= C_{eq,Q} \Big|_0^{v_2} v_2 - C_{eq,Q} \Big|_0^{v_1} v_1. \end{aligned} \quad (3)$$

This provides the charge equivalent capacitance value for capacitor charging from v_1 to v_2 as

$$C_{eq,Q} \Big|_{v_1}^{v_2} = \frac{C_{eq,Q} \Big|_0^{v_2} v_2 - C_{eq,Q} \Big|_0^{v_1} v_1}{v_2 - v_1}. \quad (4)$$

Equation (4) can be employed to calculate the charge equivalent capacitance value when the capacitor is charging from v_1 to v_2 , where v_1 and v_2 can be any values from 0 to the rated operating voltage of the MOSFET.

IV. MINIMUM ENERGY REQUIREMENT FOR ZVS

In prior literature works [10]–[13], the energy needed from the tank inductor L to attain ZVS is directly equated to the sum of the absolute values of charging and discharging energies demanded by the C_{oss} of MOSFETs. For example, the minimum energy requirement during transition I is expressed as,

$$\frac{1}{2} L I_{L(\min)}^2 = \frac{1}{2} C_o (v_{pn}^2 - v_{po}^2) + \frac{1}{2} C_o v_{on}^2 + \frac{1}{2} C_o v_{on}^2, \quad (5)$$

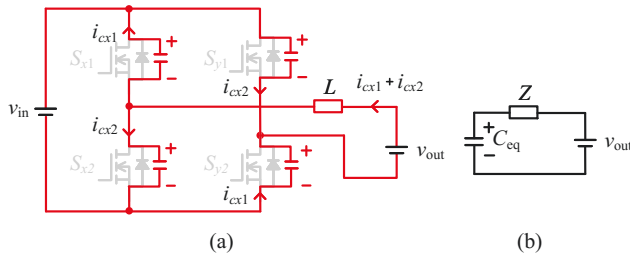


Fig. 5. (a) H-bridge during the dead time interval before switches S_{x1} and S_{y2} turn on, (b) H-bridge equivalent circuit for calculation of minimum ZVS current.

where, C_o is a constant value of the output capacitance of MOSFET, typically taken at the rated voltage of the MOSFET, and $I_{L(\min)}$ is the instantaneous inductor current available during the switching transition. However, using (5) results in inaccuracies as the energies delivered/absorbed by the sources in the circuit are neglected. This work considers the energies of all components in the circuit to precisely ascertain the energy demand of the tank inductor for achieving ZVS.

To enhance understanding, this paper first explains a similar derivation of the minimum current for an H-bridge before delving into the derivation for a T-type bridge.

A. Minimum Energy Requirement for H-bridge

In the context of an H-bridge circuit operating with a 50% complementary duty cycle, all 4 switches remain off during the dead time intervals and their output capacitors either charge or discharge, as illustrated in Fig. 5(a). The input voltage to the H-bridge is denoted as v_{in} , the reflected output voltage from the secondary bridge is represented as v_{out} , and L denotes the tank inductance. Both voltages, v_{in} and v_{out} , can either remain constant or vary with time. Consider the scenario where capacitors of switches S_{x1} and S_{y2} discharge, while those of S_{x2} and S_{y1} charge. To calculate the energy requirement from L for ZVS, the energies of each component in the circuit are calculated, and the energy conservation equation [16], given by

$$E_{c,\text{initial}} + E_{\text{delivered}} = E_{c,\text{final}} + E_{\text{dissipated}}, \quad (6)$$

is employed. Here, $E_{c,\text{initial}}$ is the total initial capacitive (C_{oss}) energy in the circuit before the particular switching transition and $E_{c,\text{final}}$ is the total final capacitive energy in the circuit after the switching transition. The terms $E_{\text{delivered}}$ and $E_{\text{dissipated}}$ denote the total energy delivered and the total energy dissipated in the circuit during the switching transition, respectively. The energies delivered by two sources v_{out} and v_{in} are

$$\begin{aligned} E_{v_{out}} &= \int (i_{cx1} + i_{cx2}) v_{out} dt \\ &= v_{out} \left(\int_{v_{in}}^0 -C_{\text{oss}}|_v dv + \int_0^{v_{in}} C_{\text{oss}}|_v dv \right) \\ &= 2 C_{\text{eq,Q}} \Big|_0^{v_{in}} v_{out} v_{in}. \end{aligned} \quad (7)$$

$$E_{v_{in}} = \int (i_{cx2} - i_{cx1}) v_{in} dt = 0, \quad (8)$$

As the energy delivered by the source v_{in} is zero, the entire H-bridge can be represented by an equivalent capacitor C_{eq} . This equivalent capacitor is charging from $-v_{in}$ to $+v_{in}$ as shown in Fig. 5(b).

Assuming that the initial and final energies of C_{eq} in Fig. 5(b) is same (hysteresis effect [17], [18] is neglected), and considering zero energy dissipation in the circuit during complete soft-switching ($E_{\text{dissipated}} = 0$), the energy balance equation, given by (6) is modified to,

$$E_{\text{delivered}} = E_L + E_{v_{out}} = 0. \quad (9)$$

Hence, energy delivered by the inductance L is

$$E_L = -E_{v_{out}} = 2 C_{\text{eq,Q}} \Big|_0^{v_{in}} v_{out} v_{in}. \quad (10)$$

If v_{out} is negative, $E_{v_{out}}$ is negative and source v_{out} absorbs power. If I_L is the instantaneous current during the switching transition, flowing into the primary bridge leg x , the minimum energy required by the inductor to satisfy ZVS condition is

$$E_L = \frac{1}{2} L I_L^2 \geq 2 C_{\text{eq,Q}} \Big|_0^{v_{in}} v_{out} v_{in}. \quad (11)$$

The required minimum current is

$$I_{L(\min)} = \sqrt{\frac{4 C_{\text{eq,Q}} \Big|_0^{v_{in}} v_{out} v_{in}}{L}}. \quad (12)$$

In cases when v_{out} is either positive or zero, there is no minimum energy requirement and soft switching is achieved if an adequate dead time is provided.

B. Minimum Energy Requirement for T-type Bridge

A similar analysis can be performed for a T-type bridge as in the previous subsection. Specifically, transition I and II are investigated to establish the minimum energy requirement for achieving ZVS. A generalized tank circuit is analyzed comprising of inductance L and reflected secondary voltage v_{out} . The equivalent circuits during dead time intervals of transition I and transition II are shown in Fig. 6(a) and Fig. 6(b), respectively.

Here, x leg switches are actively switching, while y leg is tied to n node. To achieve soft-switching during transition I, the tank current going into the bridge leg x is necessary, as illustrated in Fig. 6. The energy delivered by the voltage source v_{po} , v_{on} , and reflected secondary bridge source v_{out} are

$$E_{v_{po}} = - \int i_{cx1} v_{po} dt = -C_{\text{eq,Q}}(HB) \Big|_{v_{po}}^{v_{pn}} v_{po} v_{on}, \quad (13)$$

$$E_{v_{on}} = -v_{on}^2 \left(C_{\text{eq,Q}}(HB) \Big|_{v_{po}}^{v_{pn}} + C_{\text{eq,Q}}(CS) \Big|_0^{v_{on}} \right), \quad (14)$$

$$\begin{aligned} E_{v_{out}} &= v_{out} v_{on} \left(C_{\text{eq,Q}}(HB) \Big|_{v_{po}}^{v_{pn}} + C_{\text{eq,Q}}(CS) \Big|_0^{v_{on}} \right. \\ &\quad \left. + C_{\text{eq,Q}}(HB) \Big|_0^{v_{on}} \right). \end{aligned} \quad (15)$$

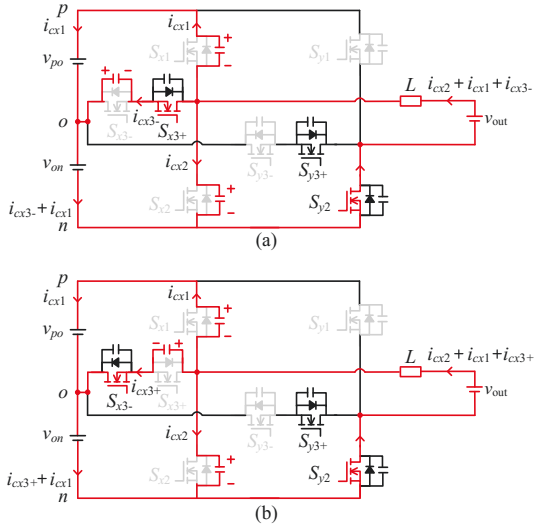


Fig. 6. (a) Circuit during the dead time interval of transition I, (b) Circuit during the dead time interval of transition II.

The term $C_{eq,Q(HB)}$ represents the charge-equivalent capacitance for half-bridge devices (S_{x1} , S_{x2} , S_{y1} , and S_{y2}) and $C_{eq,Q(CS)}$ represents the charge-equivalent capacitance for common-source devices (S_{x3+} , S_{x3-} , S_{y3+} , and S_{y3-}). In contrast to the H-bridge circuit, the total change in the capacitor energy is not zero for a particular transition in the case of a T-type bridge. The total change in energy during transition I is

$$\begin{aligned} \Delta E_c &= E_{c,initial} - E_{c,final} \\ &= \frac{1}{2} C_{eq,E(HB)} \Big|_0^{v_{pn}} v_{pn}^2 - \frac{1}{2} C_{eq,E(HB)} \Big|_0^{v_{po}} v_{po}^2 \\ &\quad + \frac{1}{2} \left(C_{eq,E(CS)} \Big|_0^{v_{on}} - C_{eq,E(HB)} \Big|_0^{v_{on}} \right) v_{on}^2. \end{aligned} \quad (16)$$

Assuming zero losses in the circuit ($E_{dissipated} = 0$) in case of complete ZVS, the energy that needs to be processed by the inductance L is

$$E_{L(trI)} = -E_{v_{out}} - E_{v_{po}} - E_{v_{on}} - E_{c,initial} + E_{c,final}. \quad (17)$$

Similar to the minimum current condition for ZVS in an H-bridge, the minimum current for ZVS in a T-type bridge can be calculated as

$$I_{L(min)} = \left\lceil \sqrt{\frac{2E_{L(trI)}}{L}} \right\rceil. \quad (18)$$

In cases where E_L is negative or zero, there is no minimum energy requirement and ZVS is achieved if adequate dead time is provided. If v_{out} is negative during transition I, as is typically the case for forward power flow direction, the term $E_{v_{out}}$ is negative. Consequently, all the terms $E_{v_{po}}$, $E_{v_{on}}$, and $E_{v_{out}}$ are negative in (13)-(15), as all sources are absorbing energy during the transition. These energies must be provided by tank inductor L in addition to the total change in capacitor energy required. Similar equations can be derived for transition II. The T-type bridge circuit during transition II is shown in Fig. 6(b).

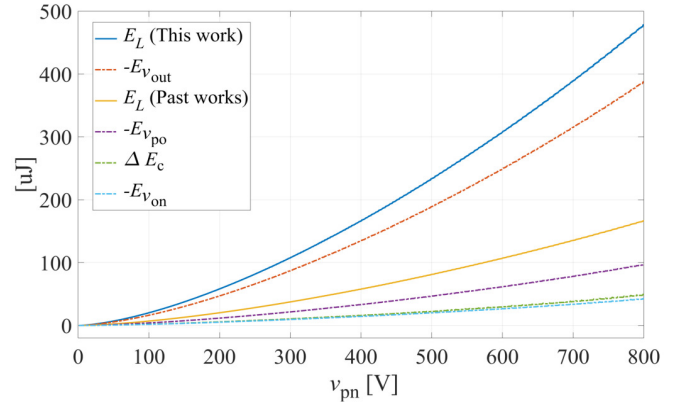


Fig. 7. Energies delivered by v_{po} , v_{on} , and v_{out} (with negative signs denoting energy absorption), the contribution of change in capacitive (C_{oss}) energy ΔE_c , and total energy required from the inductor L during switching transition I as a function of total input voltage v_{pn} .

To emphasize the energy contributions of sources present in the circuit, a plot showing the energies of all sources, change in capacitive energy required, and the minimum ZVS energy required by the tank inductance as a function of input voltage v_{pn} is shown in Fig. 7, with $v_{po} = v_{on} = v_{pn}/2$, and $v_{out} = v_{pn}$. The MOSFETs used for calculation are mentioned in Section VI.

From Fig. 7, it can be observed that the change in the capacitor energy required is minimal as compared to the energy contributions of the sources. Fig. 7 also shows the calculated minimum energy requirement from tank inductor L when (5) is used, which results in under estimation of the minimum energy requirement with error as high as 50%. For calculating E_L using (5), different values of charge equivalent capacitances are considered at each value of input voltage.

V. SIMPLIFIED EQUATIONS FOR EQUAL INPUT VOLTAGE CASE

Simplified equations for minimum energy requirement from the tank inductor can be written when $v_{po} = v_{on} = \frac{V_{dc}}{2}$, and using same switches for common-source and half-bridge devices such that $C_{eq,Q(CS)} = C_{eq,Q(HB)} = C_{eq,Q}$, and $C_{eq,E(CS)} = C_{eq,E(HB)} = C_{eq,E}$. For ZVS during transition I and transition II, respectively, the simplified equations are given in Table III. The ZVS energy requirement for the transition from o to n (transition I) and n to o (transition IV) are the same, only difference is the direction of the tank current. Similar is the case for the transition from o to p (transition II) and p to o (transition III), as given in Table III.

Table III specifies the minimum ZVS energy requirement for the T-type bridge when the zero state is generated using n of both legs. A similar process can be adopted to determine ZVS requirements if the zero state is generated using o node or p node.

TABLE III
SIMPLIFIED EQUATIONS FOR EQUAL INPUT VOLTAGE CASE

Transition	Minimum energy requirement from the tank inductor ($E_{L(\min)}$)
Node n to o or vice-versa	$C_{eq,Q}\bigg _0^{\frac{V_{dc}}{2}} \left(\frac{-V_{dc}}{2} - v_{out} \right) \frac{V_{dc}}{2} + C_{eq,Q}\bigg _0^{V_{dc}} (V_{dc} - v_{out}) V_{dc} + \frac{1}{2} C_{eq,E}\bigg _0^{\frac{V_{dc}}{2}} \left(\frac{V_{dc}}{2} \right)^2 - \frac{1}{2} C_{eq,E}\bigg _0^{V_{dc}} V_{dc}^2$
Node p to o or vice-versa	$C_{eq,Q}\bigg _0^{\frac{V_{dc}}{2}} \left(\frac{3V_{dc}}{2} - v_{out} \right) \frac{V_{dc}}{2} - C_{eq,Q}\bigg _0^{V_{dc}} v_{out} V_{dc} - \frac{1}{2} C_{eq,E}\bigg _0^{\frac{V_{dc}}{2}} \left(\frac{V_{dc}}{2} \right)^2 + \frac{1}{2} C_{eq,E}\bigg _0^{V_{dc}} V_{dc}^2$

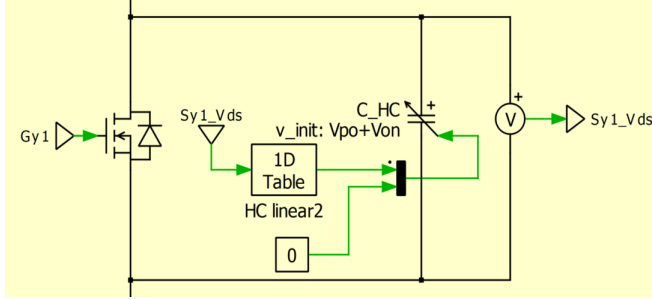


Fig. 8. PLECS simulation capture showing modeling of the nonlinear capacitance of MOSFET across one of the T-type bridge switches.

TABLE IV
SIMULATION-BASED VERIFICATION OF MINIMUM ZVS CALCULATION.

Case	Circuit Conditions	$I_{L(\min)}$ (this work)	$I_{L(\min)}$ (past works)
9(a)	$L = 29.3 \mu H$, $v_{po} = v_{on} = 340$ V, $v_{out} = -760$ V, $I_{L(tr)} = 5.217$ A	5.195 A	2.963 A
9(b)	$L = 29.3 \mu H$, $v_{po} = v_{on} = 340$ V, $v_{out} = -760$ V, $I_{L(tr)} = 6.154$ A	6.217 A	2.963 A

VI. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Simulation-based Verification

To verify the accuracy of the ZVS analysis, simulations are performed using PLECS software for a T-type bridge-based dc-dc converter with a commutation sequence depicted in Fig. 2 and tank circuit represented with an inductor and voltage source v_{out} . The simulation introduces nonlinear output capacitances across the drain-to-source of an ideal MOSFET device as shown in Fig. 8. The C_{oss} nonlinearity of the MOSFETs is modeled using a 1D look-up table, making C_{oss} a voltage-dependent quantity. Fig. 9(a) and (b) show the simulation results for verification of minimum ZVS current for transition I and transition II respectively. The relevant circuit conditions, minimum current value calculated in this work, and its comparison with previous literature work is specified in Table IV. It can be observed that the transient current during boundary ZVS case ($I_{L(tr-boundary)}$) matches well with the calculated $I_{L(\min)}$ in this work.

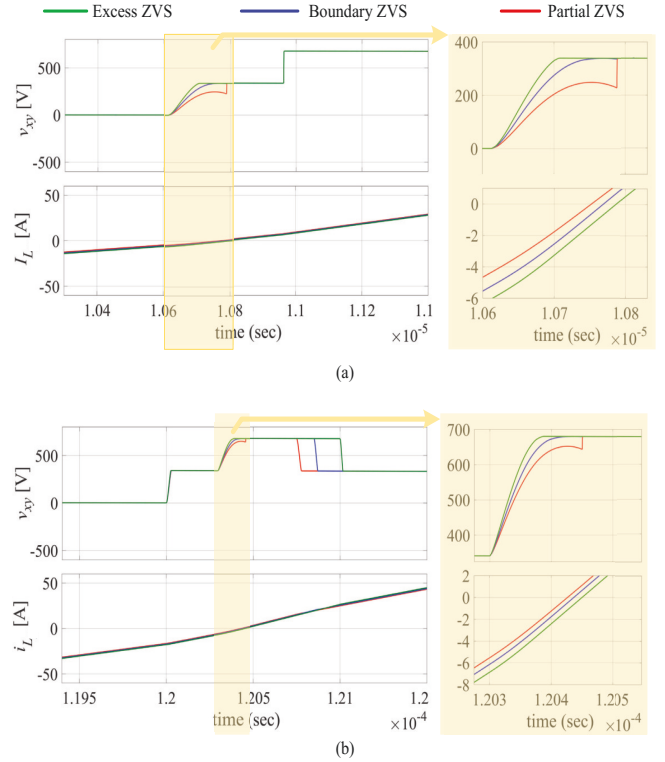


Fig. 9. Simulation results showing boundary, excess, and partial ZVS case. The switch node voltage v_{xy} and tank current i_L are shown (a) during transition I, and (b) during transition II.

TABLE V
SiC MOSFETs USED IN THE HARDWARE SETUP.

Component	Description
Half bridge MOSFETs (HB) $S_{x1}, S_{x2}, S_{y1}, S_{y2}$	Onsemi NVH4L020N120SC1 1200 V, 102 A
Common-source MOSFETs (CS) $S_{x3+}, S_{x3-}, S_{y3+}, S_{y3-}$	Onsemi NVH4L040N120SC1 1200 V, 58 A

B. Experimental Verification

Experiments are conducted on an ac-dc converter circuit comprising a three-phase grid-tied Unfolder followed by a resonant dc-dc converter. The primary bridge of the dc-dc converter is a T-type bridge, as shown in Fig. 10. Following

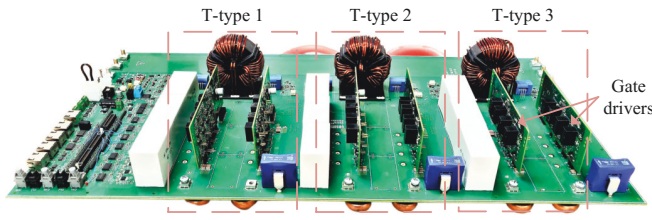


Fig. 10. The hardware image displays a setup featuring three independent T-type bridges, one of which is utilized for this work. This configuration is designed for a 3x20-kW unfolding-based *LCL* resonant converter [6].

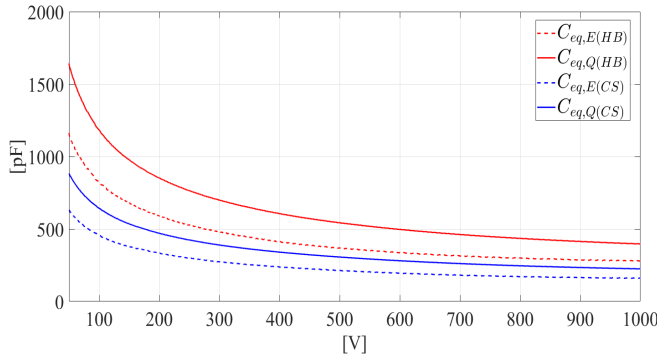


Fig. 11. Charge and energy equivalent capacitance values for drain-to-source voltage variation from 0 V to 1000 V for two of the Omsemi Silicon Carbide (SiC) MOSFETs utilized in this work. Solid lines represent the charge-equivalent capacitance values, while dotted lines indicate the energy-equivalent capacitance values.

the primary bridge, there is a *LCL* tank circuit and a diode bridge rectifier. The voltage across the parallel capacitor in the *LCL* tank circuit represents the reflected voltage source v_{out} . The tank inductance has a value of 29.3 μ H. Additional details about the hardware setup can be found in [6].

Fig. 11 shows the charge and energy-equivalent capacitances calculated for two of the 1200 V Omsemi Silicon Carbide (SiC) MOSFETs employed in this work which are given in Table V. These values are calculated at various drain-to-source voltages ranging from 0 V to 1000 V. To create these curves, data points are extracted from the $C_{oss} - v_{ds}$ curves provided in the datasheets [19], [20], and numerical integration is performed in MATLAB as provided in [14].

The verification of minimum current conditions is conducted for different sets of input voltages, v_{po} and v_{on} . In Fig. 12, an operational state is shown where v_{po} is 283 V, v_{on} is 394 V, v_{out} is -752 V, and the system operates at the boundary ZVS current. The estimated minimum current for these circuit conditions is 6.2 A, aligning closely with the experimental result of 6.3 A. Fig. 13 displays another operating scenario with v_{po} at 192 V, v_{on} at 488 V, and v_{out} at -712 V. In this case, there is insufficient current for ZVS, leading to partial ZVS waveforms. The estimated minimum current for these conditions is 5.5 A, which is more than the available current of 4.2 A during the switching instant, resulting in partial ZVS. During the estimation of minimum current, an

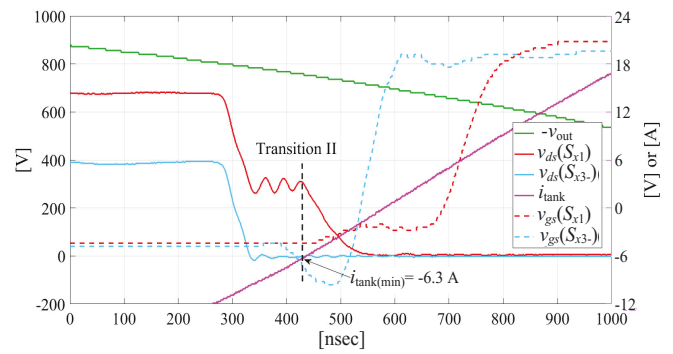


Fig. 12. Experimental results with boundary ZVS current with commutation sequence A, focusing on the minimum current required for transition II. The left y-axis shows drain-source voltages of switches S_{x1} and S_{x3} , and reflected tank voltage (v_{out}), right y-axis show the gate to source voltages and tank current. Here, $v_{po} = 283$ V, $v_{on} = 394$ V, $v_{out} = -752$ V.

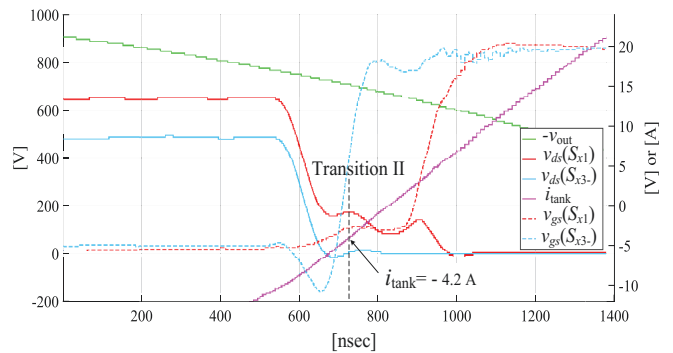


Fig. 13. Experimental results with partial ZVS with commutation sequence A, focusing on the minimum current required for transition II. The left y-axis shows drain source voltages and reflected voltage from the tank circuit (v_{out}), right y-axis shows the gate to source voltages and tank current. Here, $v_{po} = 192$ V, $v_{on} = 488$ V, $v_{out} = -712$ V.

additional capacitance of 150 pF is added across switch nodes and the input node to compensate for the PCB capacitance.

VII. CONCLUSION

This work proposes an energy-based method to determine the minimum ZVS current requirement for a T-type bridge employed in a resonant converter. The nonlinear output capacitances of the MOSFETs are considered by using charge and energy equivalent capacitors. The simulations and hardware results verify the proposed solution. A simplified solution is provided for an equal input voltage case to the T-type bridge. Below are the further concluding remarks.

- The proposed method applies to any kind of resonant converter tank with the use of equivalent tank circuit representation. It also applies to either constant or time-varying input voltages to the T-type bridge.
- If the dead times are sufficiently shorter than the switching frequency, the tank circuit can be analyzed using the fundamental harmonic approximation method, while the proposed method, used in conjunction, ensures ZVS operation.

- The proposed method can be extended for various commutation sequences of a T-type bridge and several other multi-level converter topologies.

REFERENCES

- [1] S. Satpathy, P. P. Das and S. Bhattacharya, "Power Layout Design of a GaN HEMTs-Based High-Power High-Efficiency Three-Level ANPC Inverter for 800 V DC Bus System," in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 5, no. 2, pp. 565-576, April 2024, doi: 10.1109/JESTIE.2024.3355881.
- [2] X. Zhao et al., "Design and Implementation of SiC-Based 200-kW High-Density High-Speed High-Altitude Electric Propulsion AC Drive System," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2024.3419149.
- [3] S. Satpathy, S. Bhattacharya and V. Veliadis, "Comprehensive Loss Analysis of Two-level and Three-Level Inverter for Electric Vehicle Using Drive Cycle Models," *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, Singapore, 2020, pp. 2017-2024, doi: 10.1109/IECON43393.2020.9254520.
- [4] B. Liu, R. Ren, E. A. Jones, F. Wang, D. Costinett and Z. Zhang, "A Modulation Compensation Scheme to Reduce Input Current Distortion in GaN-Based High Switching Frequency Three-Phase Three-Level Vienna-Type Rectifiers," in *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 283-298, Jan. 2018, doi: 10.1109/TPEL.2017.2672756.
- [5] S. Gurudiwan, A. Zade, R. Hatch, H. Wang and R. Zane, "ZVS Boundary Assessment for T-type-based Dual Active Bridge Series Resonant Converters using State-Plane Analysis," 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024, pp. 2098-2105, doi: 10.1109/APEC48139.2024.10509450.
- [6] A. Zade et al., "A 21 kW Unfolding-Based Single-Stage AC-DC Converter for Wireless Charging Applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2023.3309588.
- [7] A. Zade, S. Gurudiwan, D. Maksimović and R. Zane, "High-Bandwidth Control of a 20-kW Single-Stage Unfolding-Based AC-DC Converter Using the Extra Element Theorem and Current Emulation Technique," in *IEEE Transactions on Power Electronics*, doi: 10.1109/TPEL.2024.3423705.
- [8] A. Blinov, D. Zinchenko, J. Rąbkowski, G. Wrona and D. Vinnikov, "Quasi Single-Stage Three-Phase Filterless Converter for EV Charging Applications," in *IEEE Open Journal of Power Electronics*, vol. 3, pp. 51-60, 2022, doi: 10.1109/OJPEL.2021.3134460.
- [9] M. S. Khan, S. S. Nag and A. Das, "A High Efficiency Non-Isolated Three-Phase Unfolding Based Electric Vehicle Powertrain," in *IEEE Transactions on Industry Applications*, doi: 10.1109/TIA.2024.3383803.
- [10] K. Kalayci, O. Demirel, U. Arifoglu and H. Hizarci, "Analysis of Three-Level T-Type LLC Resonant Isolated Bidirectional DC-DC Converter Under Three-Degrees-of-Freedom Modulation," in *IEEE Access*, vol. 11, pp. 60605-60625, 2023, doi: 10.1109/ACCESS.2023.3285265.
- [11] D. Liu, Y. Wang, F. Deng, Q. Zhang and Z. Chen, "Zero-Voltage Switching Full-Bridge T-Type DC/DC Converter with Wide Input Voltage Range and Balanced Switch Currents," in *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10449-10466, Dec. 2018, doi: 10.1109/TPEL.2018.2800902.
- [12] B. Zhang, S. Xie, Z. Li, P. Zhao and J. Xu, "An Optimized Single-Stage Isolated Swiss-Type AC/DC Converter Based on Single Full-Bridge With Midpoint-Clamper," in *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11288-11297, Oct. 2021, doi: 10.1109/TPEL.2021.3073742.
- [13] L. Jin, B. Liu and S. Duan, "ZVS Soft Switching Operation Range Analysis of Three-Level Dual-Active Bridge DC-DC Converter Under Phase Shift Control Strategy," in *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 1963-1972, March-April 2019, doi: 10.1109/TIA.2018.2872121.
- [14] S. Gurudiwan, A. Zade, H. Wang and R. Zane, "Accurate ZVS Analysis of a Full-Bridge T-Type Resonant Converter for a 20-kW Unfolding-Based AC-DC Topology," in *IEEE Open Journal of Power Electronics*, vol. 5, pp. 692-708, 2024, doi: 10.1109/OJPEL.2024.3400256.
- [15] D. Costinett, D. Maksimovic and R. Zane, "Circuit-Oriented Treatment of Nonlinear Capacitances in Switched-Mode Power Supplies," in *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 985-995, Feb. 2015, doi: 10.1109/TPEL.2014.2313611.
- [16] M. Kasper, R. M. Burkart, G. Deboy and J. W. Kolar, "ZVS of Power MOSFETs Revisited," in *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063-8067, Dec. 2016, doi: 10.1109/TPEL.2016.2574998.
- [17] G. Zulauf, Z. Tong, J. D. Plummer and J. M. Rivas-Davila, "Active Power Device Selection in High- and Very-High-Frequency Power Converters," in *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6818-6833, July 2019, doi: 10.1109/TPEL.2018.2874420.
- [18] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn and J. Rivas-Davila, "COSS Losses in 600 V GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters," in *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10748-10763, Dec. 2018, doi: 10.1109/TPEL.2018.2800533.
- [19] Omsemi Silicon Carbide (SiC) MOSFET, NVH4L020N120SC1, N-Channel EliteSiC, 20 mohm, 1200 V, M1, TO247-4L, <https://www.onsemi.com/download/data-sheet/pdf/nvh4l020n120sc1-d.pdf>
- [20] Omsemi Silicon Carbide (SiC) MOSFET, NVH4L040N120SC1, N-Channel EliteSiC, 40 mohm, 1200 V, M1, TO247-4L, <https://www.onsemi.com/download/data-sheet/pdf/nvh4l040n120sc1-d.pdf>