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Reducing the Barrier Height in Organic Transistors

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Reducing the Schottky barrier height and Fermi level de-pinning in metal-organic semiconductor contacts are crucial for enhancing the performance of organic transistors. The reduction of the Schottky barrier height in bottom-contact top-gate organic transistors is demonstrated by adding 1 nm thick atomic layer deposited Al_2O_3 on the source and drain contacts. By using two different donor-acceptor copolymers, both *p*- and *n*-type transistors are investigated. Temperature-dependent current–voltage measurements from non-treated, self-assembled monolayer treated, and Al_2O_3 treated Au source-drain contact field-effect transistors with varying channel lengths are carried out. The drain current versus drain voltage near zero gate voltage, which may be described by the thermionic emission model at temperatures above 150 K, allows the estimation of the Schottky barrier height (φ_B). The Al_2O_3 contact-treated transistors show more than 40% lower φ_B compared with the non-treated contacts in the *p*-type transistor. Similarly, an isoindigo-based transistor, with *n*-type transport, shows a reduction in φ_B with Al_2O_3 treated contacts suggesting that such ultrathin oxide layers provide a universal method for reducing the barrier height.

1. Introduction

The past 20 years have seen a revolution in flexible and wearable electronics owing to the extensive research and development in organic semiconductors and device engineering, enabling efficient charge injection and extraction, the two most important elements in organic light-emitting diodes (OLEDs) and organic solar cells. OLEDs are now an integral part of consumer electronics, offering a viable path for flexible displays.[1] Organic transistors, on the other hand, which were thought to be an alternative to inorganic transistors for large-area integrated circuits, have yet to achieve the same status as OLEDs in consumer electronics. Organic transistors still struggle to attain transit frequencies >10 MHz, although there are a few reports of transit frequencies >20 MHz.[2–4] Compared to inorganic semiconductors, where metal oxide semiconductor field-effect transistors (MOSFETs) and gallium nitride high electron mobility transistors routinely achieve Rc (channel-width normalized contact resistance) as low as 0.01 Ωcm,[5,6] organic transistors typically show Rc in the range of 100 kΩcm, and at best 100 Ωcm.[7] Thus far, the strategies for lowering Rc in organic transistors have mainly focused on controlling the thin-film morphology near the source-drain contacts by using self-assembled monolayers and/or exploiting solution processing conditions for polymeric semiconductors.[8–10] Combining contact modification and using extremely thin gate dielectrics have resulted in the value of Rc to be just under 30 Ωcm,[11] and with a transfer metal contact technique, Rc of 14 Ωcm has been achieved in C_{10}-DNTT transistors.[12] Few efforts have been aimed at reducing the Schottky barrier height by de-pinning the Fermi level for improving the performance of organic field-effect transistors (FETs). This barrier refers to the energy mismatch between the Fermi level of the metal contact and the majority carrier band edge.

Most organic FETs operate in the accumulation region, where charge injection, and thus the contact work function of the metal (φ_m), is a key parameter. Obtaining Ohmic contact at the metal-organic semiconductor interface is a challenge due to the formation of a Schottky barrier (φ_B), an interface dipole barrier (Δ), an interfacial van der Waals gap (d_{vdW}), and the width of the depletion region. Although there are several strategies for reducing Δ and d_{vdW}, for example by adding self-assembled monolayers

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.202400503

DOI: 10.1002/aelm.202400503

to the contacts,[13] such strategies do not necessarily alter the final barrier heights if the Fermi level gets "pinned." Since R_c depends on φ_B, a reduction in the barrier height reduces the contact resistance as well. A recurring theme in inorganic semiconductors such as GaAs is the problem of Fermi level pinning due to the formation of interfacial mid-gap states.[14] The consequence of such states in organic semiconductors is that the Fermi level may be pinned with respect to the transport levels, implying that the changes in the contact work function are independent of the electron/hole barrier heights. Although the barrier height may only have a moderate influence on the FET channel current and the device geometry and processing conditions strongly impact the FET performance,[15] insights from 2D materials-metal interfaces highlight the role metal-induced mid-gap states, which may induce semiconductor to metal transitions.[16] Metal-induced gap states are intrinsic to organic FETs employing contact metals such as Au, which have a high density of states at the Fermi level. It is, therefore, important to reinvestigate the correlation between the barrier height, de-pinning the Fermi level by filling the mid-gap states, and FET performance including universal strategies for de-pinning the Fermi level in both *p*- and *n*-type transport.

There have been recent efforts in reducing the barrier height in organic FETs. Introducing oxygen between the metal and the organic semiconducting layer is seen to greatly reduce R_c, resulting in carrier mobilities as high as 11 $cm^2\ V s^{-1}$ in C_{10}-DNTT-based FETs.[17] However, this method is beneficial only for *p*-type FETs and not for *n*-type transport, suggesting that a more universal method should be sought after for reducing the barrier height in organic transistors. As such, doping the semiconductor is a means for reducing the barrier height and has been demonstrated to significantly enhance the performance of organic FETs.[18,19] However, contact doping can be challenging in organic FETs due to the diffusion of dopants within the bulk and the presence of counterions, which can deteriorate the transport characteristics. The use of an interlayer with a higher ionization energy compared with the organic semiconductor is seen to assist the formation of an Ohmic contact for hole injection in organic diodes by a realignment of the Fermi level.[20] A similar strategy by choosing an interlayer with a lower electron affinity compared with the organic semiconductor helps achieve Ohmic electron injection in diodes.[21] However, since some of these interlayers readily dissolve in solvents used for dissolving the organic semiconductor, bottom-contact FETs may suffer. Moreover, since Au contacts are ubiquitous for several classes of organic semiconductors for both *p*- and *n*-type transport in FETs, a robust route toward reducing φ_B is required.

In metal-inorganic semiconductor interfaces, the incorporation of a thin dielectric layer has been known to reduce φ_B by de-pinning the Fermi level.[22,23] In Ti/n-Si, for example, a 1 nm thick TiO_2 interfacial layer reduces φ_B by 55% compared with the architecture that has no TiO_2 layer.[24] The barrier layer, however, may effectively reduce the tunneling probability and injection efficiency. Hence, one must judiciously tune the thickness of the barrier layer to obtain the full benefit of de-pinning along with high carrier injection. A similar approach was used in top-contact bottom-gate (TCBG) pentacene FETs where a 1 nm thick metal-oxide layer in between a semiconducting pentacene layer and Au contacts was seen to reduce R_c, although this method was not shown to be universal for both *p*- and *n*-type transport.[25] Moreover, the deposition of thin metal oxide layers on top of several classes of solution-processable polymeric semiconductors is not feasible. To modify metal-Si interfaces for achieving good Ohmic contacts, Zheng and co-workers used <1 nm Al_2O_3 barrier layer embedded with sub-2 nm Pt nanoparticles.[26] This strategy not only resulted in a partial de-pinning of the Fermi level but also provided a mechanism for tuning φ_B by changing the size of the metal nanoparticles.

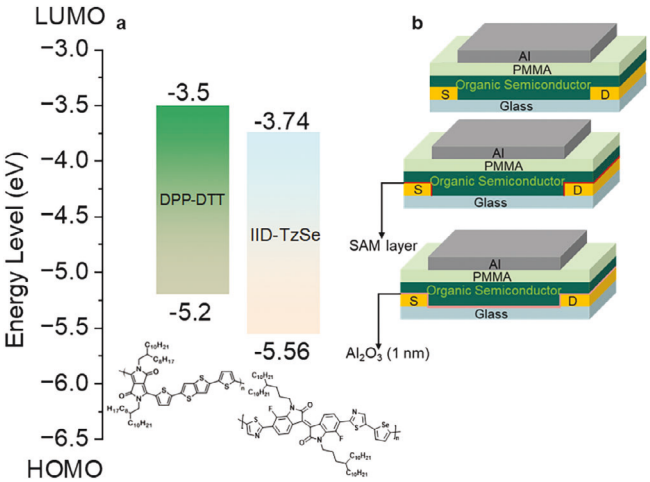

Figure 1. Energy levels and device architectures. a) Energy levels and chemical structures of the two copolymers: DPP-DTT and IID-TzSe. b) Device architectures with different treatments to the metal contacts.

Taking a cue from metal-Si interfaces, in this work we add an ultrathin (1 nm) layer of atomic layer deposited (ALD) Al_2O_3 on Au contacts in bottom contact top gate (BCTG) organic FET geometries. Two donor-acceptor copolymers were used as the active semiconducting layer and polymethylmethacrylate (PMMA) was used as the gate dielectric layer for fabricating the FETs. Diketopyrrolopyrrole (dithienylthieno[3,2-b]thiophene (DPP-DTT) predominantly served as *p*-type FETs and thiazole-selenophene linked fluorinated isoindigo (IID-TzSe) served as *n*-type FETs. **Figure 1a,b** shows the energy levels, chemical structures, and device architectures used in this work. We note that DPP-based copolymer may show ambipolarity and by tuning φ_m of the metal, both *p*- and *n*-type FETs have been demonstrated.[27,28] IID-TzSe also shows ambipolarity, although in BCTG architectures it exclusively shows *n*-type transport.[29] To further compare the effect of the ultrathin Al_2O_3 layer on the contacts, DPP-DTT-based FETs with a self-assembled monolayer (SAM) layer treatment using pentafluorobenzenethiol (PFBT) were also employed. Detailed current–voltage measurements as a function of temperature reveal that the Al_2O_3-treated devices outperform the SAM layer-treated devices. By adopting the Schottky emission model at zero gate bias voltage, the temperature-dependent current–voltage measurements from the FETs allow an estimation of φ_B. The 1 nm Al_2O_3 treated DPP-DTT FETs show a 40% reduction in φ_B compared with only 20% reduction in φ_B when PFBT is used. The reduction in φ_B is in comparison with the as-is (untreated) devices. Concomitantly, the *p*-type carrier mobility is also enhanced in Al_2O_3-treated DPP-DTT FETs. To demonstrate the universality of the Al_2O_3 layer for reducing the barrier height, we developed IID-TzSe-based *n*-type

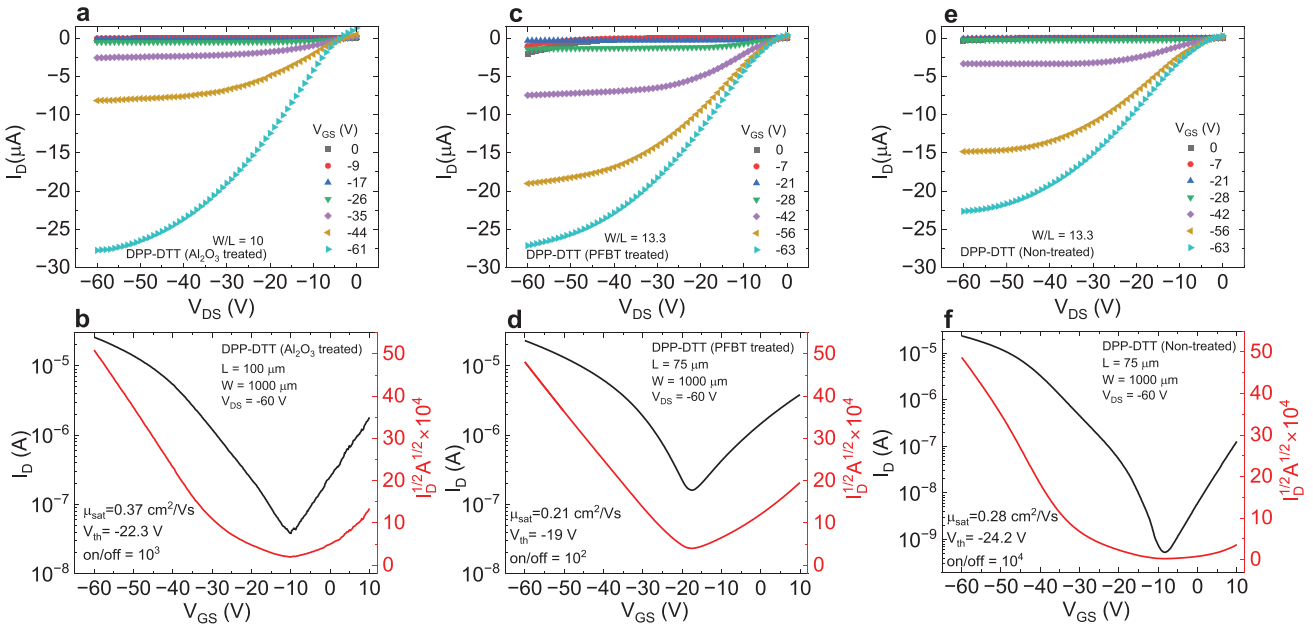

Figure 2. Output and transfer characteristics of DPP-DTT FETs. (a,b) represent an Al_2O_3 treated FET with L = 100 μm and W = 1000 μm. c,d) represent a PFBT treated FET with L = 75 μm and W = 1000 μm. e,f) represent a non-treated FET with L = 75 μm and W = 1000 μm.

FETs. Again, the Al_2O_3-treated FETs show a lower φ_B compared with non-treated IID-TzSe FETs. Although the carrier mobilities are comparable, the threshold voltage, on/off ratio, and subthreshold swing are seen to significantly improve in the Al_2O_3 barrier-modified IID-TzSe FETs compared with the non-treated devices. This work demonstrates that an ultrathin Al_2O_3 layer in BCTG FET architectures enhances the injection of carriers from the metal to the semiconductor layer, irrespective of *p*- or *n*-type transport.

2. Results and Discussion

The growth of the 1 nm Al_2O_3 layer on the Au contacts was accomplished using ALD as discussed in ref. [26]. Several optimization steps revealed that increasing the oxide layer to ≥2 nm deteriorates the transistor characteristics in DPP-DTT FETs most likely since a thicker layer impedes charge injection. Moreover, a thinner Al_2O_3 layer of 0.5 nm resulted in no change in the FET characteristics of DPP-DTT FETs, suggesting that 1 nm thickness in within the optimized range. The FET carrier mobilities were determined in the saturation region from the transfer characteristics, where $\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2$, by measuring the drain current (I_D) as a function of the gate-source voltage (V_{GS}) and by keeping the drain-source voltage (V_{DS}) constant in the saturation region. Several FETs were tested with different channel length (L) and width (W). All the FETs reported here have W = 1000 μm with variable L. The on/off ratio and subthreshold swing (SS) demonstrate how distinct the "on" and "off" states are and how quickly the device switches between them, respectively. Temperature-dependent transfer and output characteristics were measured from FETs using both copolymers.

2.1. DPP-DTT Transistors

The highest occupied molecular orbital (HOMO) level of DPP-DTT is close to the φ_m of Au (≈5.0 eV); hence with bare Au contacts, DPP-DTT FETs mainly display *p*-type transport. It should, however, be noted that substrates, inhomogeneities in surfaces, and deposition methods impact the φ_m of Au; a range of values from 4.6 to 5.6 eV has been reported in the literature.[30,31] **Figure 2a–f** shows the output and transfer characteristics at room temperature from three representative devices with Al_2O_3 treated, PFBT treated, and non-treated Au contacts. The FET with 1 nm of Al_2O_3 on Au contact shows the highest mobility of μ_{sat} = 0.37 cm^2 $V^{-1}s^{-1}$. Several devices were measured and histograms of the carrier mobilities for Al_2O_3, PFBT, and non-treated FETs are presented in Figure S1 (Supporting Information). The PFBT-treated devices show slightly higher mean carrier mobility (0.28 cm^2 $V^{-1}s^{-1}$) compared with the non-treated ones (0.22 cm^2 $V^{-1}s^{-1}$) but the Al_2O_3 treated FETs outperform with mean carrier mobility of 0.41 cm^2 $V^{-1}s^{-1}$.

A shorter channel length (L = 50 μm) of an Al_2O_3 treated FET demonstrates μ_{sat} = 0.81 cm^2 $V^{-1}s^{-1}$ along with a more ambipolar transport, as seen in both the output and transfer characteristics (see Supporting Information). These values of μ for DPP-DTT FETs (with Al_2O_3 treatment) are similar to those obtained with contact-free nonlinear optical methods.[32] As proof of concept, we further show that a surface modification layer of polyethylenimine ethoxylated (PEIE) on the Au contacts in BCTG DPP-DTT based devices results in *n*-type transport, suggesting that it is easy to switch between *p* – and *n*-type transport in DPP-DTT. These results are shown in Figure S2 (Supporting Information). To further gain insights into the nature of transport and how the barrier height

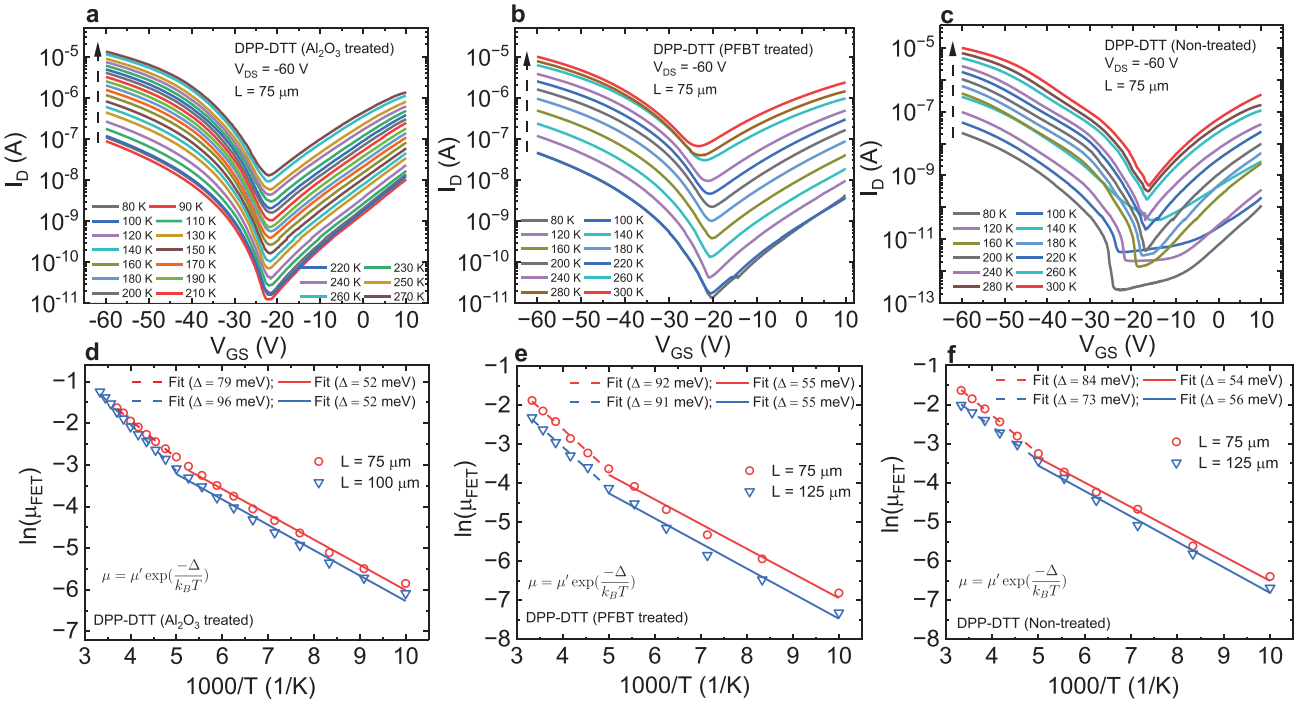

Figure 3. Temperature-dependent current–voltage measurements from DPP-DTT-based FETs. a–c) Temperature-dependent transfer characteristics of Al_2O_3 treated, PFBT treated, and non-treated FETs. The dashed arrow denotes increasing temperature. d–f) Arrhenius plots of carrier mobilities from Al_2O_3 treated, PFBT treated, and non-treated FETs for two different channel lengths (L).

changes by adding a 1 nm thick Al_2O_3 layer, temperature-dependent current–voltage measurements (80–300 K) were performed from representative DPP-DTT FETs with Al_2O_3 treated, PFBT-treated, and non-treated Au contacts with different W/L ratios.

2.1.1. Temperature-Dependent Current–Voltage Measurements

Figure 3a–c shows the transfer characteristics from three FETs as a function of temperature with contacts modified by Al_2O_3, PFBT, and a non-treated DPP-DTT FET. All three devices have the same channel L (75 μm) and W (1000 μm). Similar measurements were carried out for L = 50, 100, and 125 μm. In each case, the current increases with increasing temperature. μ_{sat} was determined at each temperature. Figure 3d–f shows the Arrhenius plots of μ_{sat} for two different channel lengths for treated and non-treated FETs. All devices show a thermally activated transport, where the carrier mobility (μ) changes with temperature (T), such that $\mu = \mu' \exp(\frac{-\Delta}{k_B T})$ with μ' being the carrier mobility in the absence of traps, Δ is the activation temperature and k_B is the Boltzmann constant. Two distinct regions are seen: 200–300 K and 100–200 K. The value of Δ is smaller for all devices in the 100–200 K regions compared with the high-temperature range. The 200–300 K range shows slight variations but the overall trends across all three architectures at two different channel lengths are similar.

The I_D-V_{DS} sweeps at V_{GS} = 0 V can be described by the thermionic emission model, which is characterized by the Richardson–Schottky equation, allowing the estimation of φ_B.[33] In this model, the current (I) is given by:

$$I = AA^* T^2 \exp\left(\frac{-(\varphi_B - \sqrt{q^3 V/4\pi\varepsilon_0\varepsilon_r d})}{k_B T}\right) \quad (1)$$

where A is the device area, A^* is the effective Richardson constant, φ_B is the Schottky barrier height, q is the element charge, V is the applied voltage between the S/D contacts, d translates to the channel length, ϵ_0 is the vacuum permittivity, ϵ_r is the dielectric constant of the semiconductor, and k_B is the Boltzmann constant. **Figure 4a** plots $\ln(I/T^2)$ versus $1/T$ for the Al_2O_3 treated, PFBT, and non-treated DPP-DTT FETs. Between 150 and 300 K, a linear region is seen, depicting the range for thermionic emission. The low-temperature region (<140 K) is representative of tunneling of carriers.[34] By assuming ϵ_r to be 3 for DPP-DTT and from the slope, we estimate φ_B for the three devices. The Al_2O_3 treated FET shows the lowest φ_B value of 82 ± 5 meV compared with 140 ± 6 meV for the non-treated device. The PFBT-treated FET yields a value of φ_B to be 111 ± 8 meV.

Our results show that the PFBT SAM layer helps in reducing the barrier but is not effective as the 1 nm layer of Al_2O_3, suggesting that the Fermi level may still be pinned. Figure 4b shows a schematic of the energy levels with and without the Al_2O_3 layer. ALD-grown Al_2O_3 uses trimethylaluminum and deionized water (DI) as precursors, where the DI water promotes the formation of the OH bonds on the surface of the oxide film. It is likely that the OH groups on the Al_2O_3 layer help in filling the trap states, thus de-pinning the Fermi level and reducing φ_B. The SAM layer

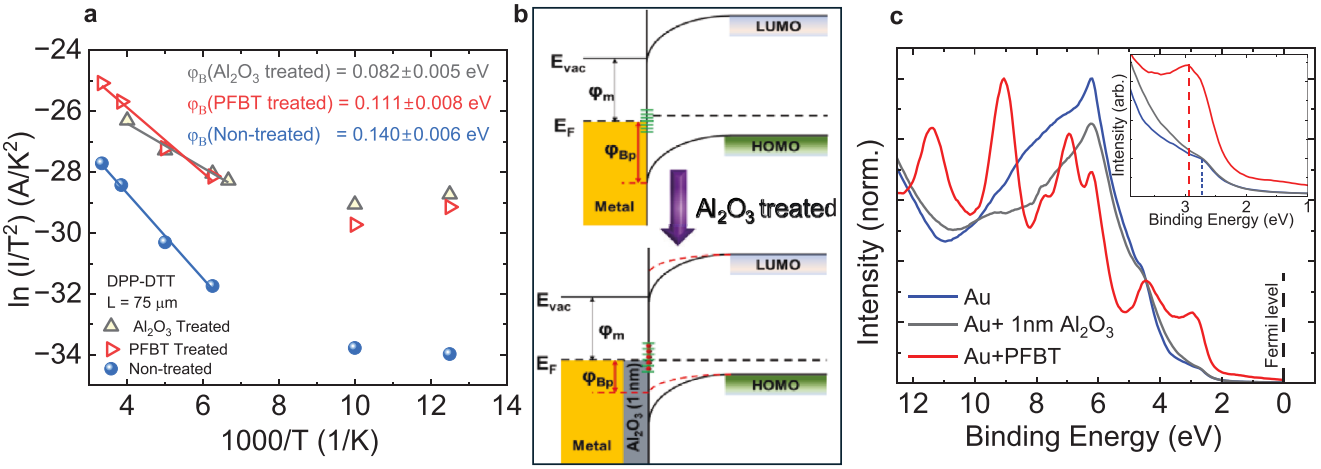

Figure 4. a) Comparison of I/T^2 vs $1/T$ characteristics of DPP-DTT FETs with Al_2O_3 treated, PFBT treated, and non-treated contacts. The bold lines are fits to Equation (1). b) Schematic energy band diagrams for *p*-type transport where the Fermi level is pinned due to interface states (top) and with the application of a 1 nm Al_2O_3 layer (bottom), which helps in de-pinning the Fermi level. φ_{Bp} denotes the Schottky barrier for the holes and φ_m represents the work function of the metal. c) UPS spectra for bare Au, Au + 1 nm Al_2O_3, and Au+PFBT. The inset shows a zoomed-in region with scaled intensities. The red and blue dashed lines depict the topmost peak position of Au 5*d* orbitals.

treatment, on the other hand, reduces φ_m without filling the traps; thus, the Fermi level remains partially pinned. This argument is further deduced from the estimation of the contact resistance. Using the transmission line method (TLM), the contact resistance (R_C) normalized with W is related to the total resistance (R) in the channel and is given by:

$$RW = R_C W + \frac{L}{\mu_{eff} C_i (V_{GS} - V_{Th})} \quad (2)$$

where μ_{eff} is the effective mobility free from the contact resistance and V_{Th} is the threshold voltage. From three or four different devices with different W/L ratios, $R_C W$ was estimated as 143 kΩ cm for the non-treated FET, 19.5 kΩ cm for the PFBT-treated FET, and 7 kΩ cm for the Al_2O_3-treated FET. See Figure S4 (Supporting Information) for the plots. These results show a similar order of magnitude for $R_C W$ after treating with PFBT and with the thin Al_2O_3 layer, suggesting that the further reduction of φ_B with Al_2O_3-treated FETs arises from a de-pinning of the Fermi level.

As a further check, we have measured the ultraviolet photoelectron spectra (UPS) from bare Au, Au treated with 1 nm Al_2O_3, and Au treated with PFBT. The filled valence states (0–12 eV binding energy) of the three samples are shown in Figure 4c. The intensities are normalized, and the Fermi edge is shown by the dashed line. We denote the occupied states below the Fermi edge as positive energies. The photon energy is 21.2 eV and the work function of photoelectron detector is 4.5 eV. The Au sample is grounded with the photoelectron detector; hence, direct determination of the work function of the metal (Au) is not feasible.[35] However, the data allows us to see the trends and to infer how the surface of Au behaves differently when treated with PFBT versus with Al_2O_3. The features in the UPS spectra from 2 to 6 eV mainly arise from the 5*d* band of Au. The sharp peaks from 6 to 8 eV in the PFBT+Au sample are from the pentafluorthiophenol ring.[36] A sample fit for the PFBT+Au interface is included in Supporting Information along with the peak positions (Figure S6, Supporting Information). The inset of Figure 4c shows a zoomed-in region ≈(2–3 eV). A clear peak shift is seen in PFBT+Au compared with bare Au and Al_2O_3 on Au. The topmost peak from the Au 5*d* orbitals is marked by the red and blue dashed lines in the inset of Figure 4c. A shift in energy of the 5*d* electrons in PFBT+Au implies a change (of 0.2 eV) in the work function compared with bare Au due to the electron transfer from Au to PFBT. The UPS spectra of Al_2O_3 on Au and bare Au, on the other hand, are almost identical, suggesting that the role of the thin Al_2O_3 layer is mainly in depinning the Fermi level without altering the work function when interfaced with the organic semiconductor in FET architectures. To test the universality of such a thin oxide layer for reducing the barrier height in organic FETs, we investigated an *n*-type FET, the results of which are provided in the next section.

2.2. IID-TzSe Transistors

Another class of donor-acceptor copolymers based on electron-deficient Isoindigo (IID) units have attracted considerable attention in organic solar cells[37,38] and transistors.[39–41] Selenium substituted fluorinated IID (IID-TzSe), with chemical structure shown in Figure 1a, has been known to show *n*-type FET transport and combined with other *p*-type FETs has promising applications in complementary inverter circuits.[29,42] Using a similar ALD-grown 1 nm Al_2O_3 on Au contacts as in the DPP-DTT devices, BCTG FETs were fabricated using IID-TzSe as the active semiconducting layer.

Figure 5a–d plots the output and transfer characteristics for two similar IID-TzSe FETs (with L = 50 µm), one with Al_2O_3 Au contacts and the other non-treated. Both FETs show *n*-type transport. Although the carrier mobilities are similar, the on/off ratio, SS, and V_{th} all seem to improve in the Al_2O_3-treated device. V_{th} decreases from 27 V in the non-treated to device to 17.7 V in the Al_2O_3-treated device. We note that the molecular weight of IID-TzSe in this work is different from ref. [29],

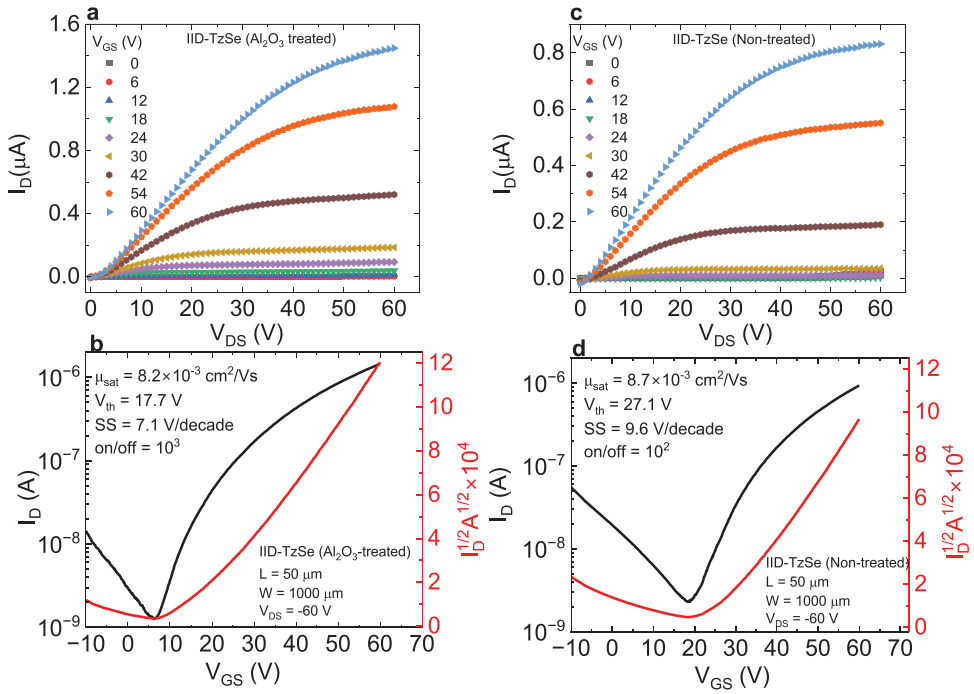

Figure 5. a,b) Output and transfer characteristics of an IID-TzSe FET with Al_2O_3 treated contacts. c,d) Output and transfer characteristics of an IID-TzSe FET with non-treated contacts.

resulting in slightly lower carrier mobilities here. To determine φ_B, temperature-dependent current–voltage measurements were performed. The transfer characteristics further allow us to estimate μ_{sat}, V_{th}, and SS as a function of temperature.

Figure 6a,b displays the transfer curves from IID-TzSe FETs with and without Al_2O_3 treated contacts as a function of temperature. The Al_2O_3 treated device was measured up to 360 K; beyond 340 K there is some degradation due to which all analysis has been carried out only till 300 K. The *n*-type carrier mobilities, extracted at each temperature, are plotted as natural log versus 1/T in Figure 6c. Similar to the DPP-DTT FETs, an activated transport is seen with two temperature regimes. The high-temperature region (200–300 K) shows a similar activation barrier (Δ ≈90 meV) for both treated and non-treated FETs. From the I_D-V_{DS} sweeps at $V_{GS} = 0$ V at different temperatures, I/T^2 is obtained and plotted as a function of $1/T$ in Figure 6d. Using Equation (1), φ_B is obtained as 120 ± 7 meV for the non-treated device and 93 ± 1 meV for the Al_2O_3-treated device. Thus, even for *n*-type transport in IID-TzSe, we observe more than 20% reduction in the Schottky barrier height. Although this reduction in φ_B does not strongly impact the carrier mobility, there is a reduction in V_{th} for Al_2O_3-treated IID-TzSe FETs at all temperatures compared with the non-treated device (Figure 6e). Similarly, at higher temperatures beyond 200 K, the SS values in the Al_2O_3-treated FET is lower compared with the non-treated FET.

An ultrathin 1 nm ALD-grown Al_2O_3 on Au contacts universally reduces the barrier height for charge injection in both *p*- and *n*-type organic FETs. This contrasts other methods such as oxygen adsorption at the metal-semiconductor interface which mainly benefits *p*-type transport but not *n*-type transport in organic FETs.[17] The lowering of φ_B in both DPP-DTT and IID-TzSe FETs with an ultrathin layer of Al_2O_3 suggests that unlike SAM layers, which mainly alter the work function of the metal to better match the HOMO or the LUMO level of the semiconductor, the oxide layer helps in de-pinning the Fermi level by filling the interface mid-gap states (Figure 4b).

To gauge whether a combination of Al_2O_3 and SAM layer may further improve the FET performance, we treated Al_2O_3-Au contacts with PFBT for fabrication of DPP-DTT FETs. Since the Al_2O_3 layer is deposited at high temperatures, it is not possible to add the oxide layer on PFBT-treated contacts. These devices were fabricated with a different batch of the DPP-DTT copolymer; hence, the carrier mobilities are slightly lower than the ones shown in Figure 1. The FET current-voltage characteristics of Al_2O_3-treated and Al_2O_3+PFBT-treated devices are shown in Figure S7 (Supporting Information). Although the on/off ratios are similar, the carrier mobility is lower for the Al_2O_3+PFBT treated transistor, suggesting that a SAM layer can disrupt the effectiveness of the ultrathin oxide layer on the Au contact.

Solution-processed organic semiconductors pose a problem with top polymeric gate architectures due to solvent incompatibility. Since PMMA dissolved in DMSO does not affect the DPP-DTT or the IID-TzSe layers, we used PMMA as the dielectric layer. It should, however, be noted that the dielectric constant (κ) of PMMA ≤3.5, implies limitations in achieving low-operating voltage FETs. As seen for both DPP-DTT and IID-TzSe FETs, the saturation voltages here are close to 60 V. Such high voltages with polymer dielectrics can lead to substantial gate currents, reducing the overall performance of the transistors. Polymer ferroelectrics such as polyvinylidene (PVDF) with $\kappa > 8$ are a good choice and can dramatically lower the operating voltages[43,44] but are difficult to integrate into top-gate architectures. It is conceivable that

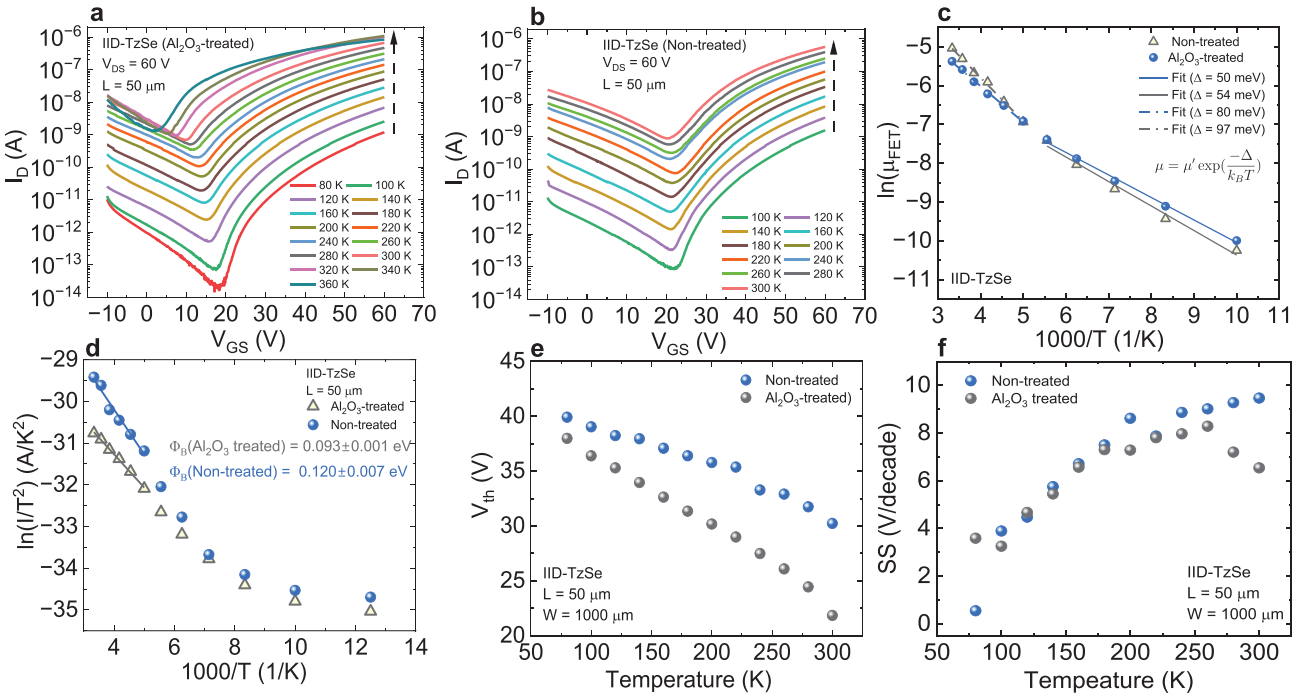

Figure 6. a,b) Transfer characteristics of IID-TzSe FETs as a function of temperature with Al_2O_3 treated contacts and non-treated contacts, respectively. The channel length and width are identical for both devices. The dashed arrow represents increasing temperature. c) Arrhenius plots of carrier mobilities for Al_2O_3 treated and non-treated FETs. d–f) Comparison of I/T^2, V_{th}, and SS as a function of temperature for Al_2O_3 treated (grey circles) and non-treated (blue circles) FETs, respectively.

with a better choice of a dielectric layer such as a combination of a thin fluoropolymer and high κ oxide dielectric, the operating voltages of DPP-DTT and IID-TzSe FETs are reduced with further enhancement in carrier mobilities. Additional modifications to the Al_2O_3 layer by embedding sub-2 nm metal nanoparticles, as realized in metal/Si interfaces,[26] may further aid in de-pinning the Fermi level and lowering φ_B. This work is a proof-of-concept that an ultrathin oxide layer improves charge injection for both *p*- and *n*-type transport. Reduction in the channel length would further benefit the performance of the devices. The processing conditions and molecular weight of the copolymers play a significant role in the chain conformation, and thus, in dictating the values of carrier mobilities, especially in DPP-based systems.[27,45] Future directions involving varying the processing conditions of the copolymers along with modifications of the ultrathin oxide layer with metal nanoparticles may further enhance the performance of organic FETs.

3. Conclusion

In summary, we report an effective strategy for modifying the contacts with an ultrathin oxide layer, which lowers the Schottky barrier height in both *p*- and *n*-type organic transistors. Unlike SAM layers that mainly alter the work function of the metal, the ultrathin Al_2O_3 layer helps in filling up the trap states at the metal-semiconductor interface, thus de-pinning the Fermi level and reducing the overall barrier height. In DPP-DTT FETs, which demonstrate *p*-type transport, φ_B reduces from 140 meV to 82 meV when the Au contacts are treated with a 1 nm ALD-grown Al_2O_3. Similarly, for IID-TzSe FETs demonstrating *n*-type transport, φ_B reduces from 120 to 93 meV upon treating the contacts with Al_2O_3. This work reveals the importance of a relatively simple treatment of the metal contacts by an ultrathin oxide layer which has advantages to both *p*- and *n*-type transport in organic transistors for improving charge injection.

4. Experimental Section

Materials: The copolymer of DPP (DPP-DTT) was purchased from 1-Material Inc. (Dorval, Quebec, Canada). IID-TzSe was synthesized based on a protocol reported earlier.[29] All solvents were procured from Sigma-Aldrich. Pentafluorothiophenol (PFBT), polymethylmethacrylate (PMMA), and polyethylenimine ethoxylated (PEIE) were also purchased from Sigm-Aldrich.

Device Fabrication: 1″ × 1″ glass microscope slides were organically cleaned by rinsing and sonication in an acetone bath for 20 min, rinsing and sonication in an isopropanol bath for 20 min, and finally rinsing and sonication in a DI-water bath for 20 min. The substrates were then baked at 125 °C in an oven for 30 min to remove all moisture. 50 nm of Au contact was thermally evaporated onto the surface of the glass with a patterned mask for the source/drain contacts. Each substrate has four devices with the same channel width of 1000 μm and varying channel lengths of 50, 75, 100, and 125 μm. The substrates with the Au contacts were plasma cleaned for 10 min in a Harrick Plasma PDC-32G plasma cleaner at a chamber pressure between 300 and 500 mTorr of O_2 gas. In one case, 10 mM concentration solution of PFBT was made by mixing 40 μL of the PFBT solution in 30 mL of isopropanol. After mixing for 1 min, the cleaned substrates with the Au contacts were immersed in the mixture for 30 min to allow the monolayer to form. The substrates were then rinsed with isopropanol, submerged in an isopropanol bath, and then finally dried with either

compressed air or nitrogen gas. For the other substrates, 1 nm of Al_2O_3 was deposited using atomic layer deposition (ALD), details of which are given below. To form the semiconducting film, DPP-DTT precursor solution was made by dissolving it in 1,2-dichlorobenzene (DCB) with a concentration of 5 mg mL^{-1}. A magnetic stirrer was added, and the solution was heated sequentially at 100 °C for 1 h, 130 °C for 1 h, and finally maintained at 145 °C for over 12 h while stirring at 200 RPM. The solution was then allowed to stir overnight at room temperature. The solution was filtered through a 0.45 µm PTFE filter and then returned to the hotplate for ≈30 min prior to spin-coating. 75 µL of the DPP-DTT solution was dynamically spin-coated on the Au contacts at 900 RPM for 60 s under nitrogen atmosphere. The DPP-DTT film was restricted to a small channel during spin-coating by applying Teflon tape. After removing the Teflon tape, the film was annealed at 120 °C for an hour under nitrogen atmosphere. PMMA, used as the top gate dielectric, was dissolved in dimethyl sulfoxide (DMSO) at a concentration of 60 mg mL^{-1}, which was then heated at 80 °C and magnetically stirred for ≈2 h. The PMMA thin film was formed by spin-coating at a spin speed of 5000 RPM for 60 s with 100 µL being cast statically on the substrate. The PMMA film was then annealed at 100 °C for 20 min, resulting in a thickness of 170–200 nm. Finally, 50 nm of Al gate electrode was thermally evaporated on top of the PMMA layer.

The IID-TzSe precursor solution was prepared by dissolving IID-TzSe in 1,2-dichlorobenzene (DCB) at a concentration of 5 mg/mL. The solution was stirred (≈200 rpm) and heated at 100 °C (1 h), 135 °C (1 h), and finally at 145 °C (>12 h). Subsequently, the solution was allowed to be stirred at room temperature overnight. The solution was filtered via 0.45 µm PTFE filter and then returned to the hotplate (≈30 mins) prior to spin-coating. To deposit the IID-TzSe onto the Au contacts, 75 µL of the solution was dynamically spin-coated at 900 RPM for 40 s under nitrogen atmosphere. Prior to the spin-coating process, Teflon tape was applied as a mask to pattern the IID-TzSe film onto a specific region. Following the removal of the tape, the film was annealed at 180 °C for 10 min under nitrogen atmosphere.

ALD Deposition: 1 nm of Al_2O_3 was precisely deposited by Atomic Layer Deposition (ALD) employing the S200 system sourced from Cambridge NanoTech. This process involved introducing deionized water (DI-water) and trimethylaluminum (TMA) obtained from Sigma-Aldrich into the system. Both the chamber and the lid O-ring heater were set to 300 °C. Following sample loading, a continuous flow of 5 sccm N_2 was introduced into the chamber, and then it was increased to 20 sccm. Deposition proceeded through 11 cycles, each consisting of 0.01 s pulse of DI-water, 8 s of N_2 purge, 0.015 s pulse of TMA vapor, followed by another 8 s of N_2 purge. The entire process lasted ≈4 min. Upon completion of deposition, the N_2 flow rate was reduced to 5 sccm, and the samples were ready for removal.

Characterization: Current–voltage (*I–V*) measurements under low temperature were performed using a Keithley 4200A-SCS parameter analyzer and a Janis cryogenic (liquid nitrogen flow) probe station. Room temperature *I–V* measurements were done both under ambient conditions as well under vacuum (33–55 mTorr). Low temperature *I–V* measurements were carried out from 80 K and upward. The UPS measurements were performed using a SPECS PHOIBOS 150 hemisphere analyzer with a SPECS UVS 300 helium discharge lamp (He I-E_{ph} = 21.2 eV).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors acknowledge support of this work through the U.S. National Science Foundation (NSF) under Grant No. ECCS-2324839. G.B. was supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, Division of Materials Science and Engineering, under Grant No. DE-SC0024294.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

A.G. fabricated the devices, conducted the electrical measurements, and analyzed the data. S.G. and S.G. conceived the work. C.M. optimized and performed the ALD and helped in the setup of low-temperature electrical measurements. S.A. and M.A.H. carried out the synthesis and characterization of the IID copolymer. J.C. and G.B. conducted the UPS measurements. S.G. and S.G. helped with the analysis of the data. The manuscript was written by S.G. and A.G. with contributions from all authors. All authors have approved the final version of the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

atomic layer deposition, Al_2O_3, donor-acceptor polymers, organic transistors, Schottky barrier

Received: July 8, 2024
Revised: September 4, 2024
Published online: October 4, 2024

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