A Prototype Millimeter-Wave Reflectionless Diplexer based on Silicon Micromachining

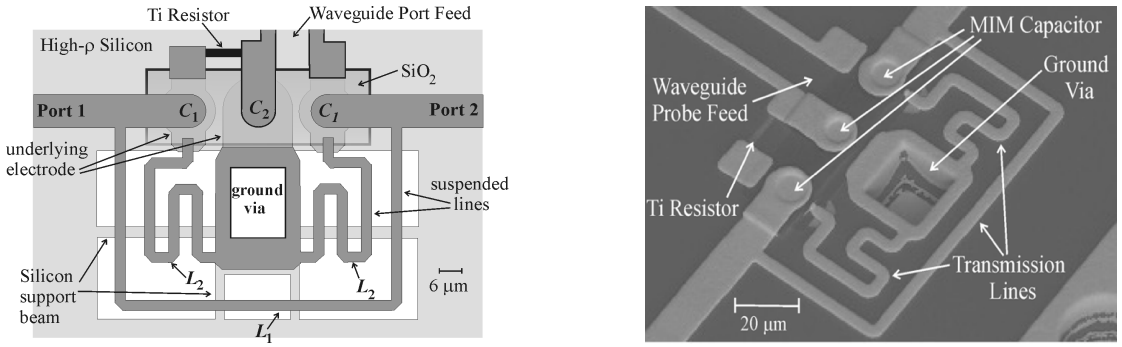
Noah D. Sauber[(1)], Matthew Bauwens[(2)], Michael Cyberey[(1)], N.S. Barker[(1)].
A.W. Lichtenberger[(1)] and Robert M. Weikle, II[(1)]

(1) University of Virginia, Charlottesville, VA, USA, (weikle@virginia.edu)
(2) Dominion Microprobes, Inc., Charlottesville, VA, USA (https://www.dmpi.co)

Millimeter and submillimeter wave instrumentation operating above 100 GHz typically utilizes rectangular waveguide as the primary propagation medium and, consequently, is limited to operation over restricted bands bound by the cut-off frequencies for single- mode propagation. Diplexers provide an option for overcoming the band limitations imposed by conventional waveguide-based instruments. This paper reports, to our knowledge, the first implementation of a prototype "quasi-reflectionless" diplexer based on the reflectionless filter concept developed by Morgan, operating at millimeter-wave frequencies, and utilizing the integration of passive elements onto a silicon-on-insulator platform.

Figure 1(a) shows the physical geometry used in this work to implement the diplexer architecture, designed for the 0—220 GHz band with target cross-over frequency at 170 GHz. Microstrip lines feed the low-band input (port 1) and output (port 2) of the diplexer and are bridged by meandered suspended lines. Capacitive elements are metal-insulator-metal structures with underlying contacts, a shared SiO_2 insulating layer, and metal overlays. A titanium thin-film resistor provides a high-band termination for the low-band input and a coplanar stripline feed with characteristic impedance of 127 Ω interfaces a high-band WR-5.1 waveguide input to the diplexer output (port 2). This stripline terminates in a bilateral radial-stub probe that couples to the high-band WR-5.1 rectangular waveguide.

The diplexer is implemented using a silicon-on-insulator (SOI) micromachining process that has been used broadly as a platform for integration. Fabrication utilizes frontside lithography, sputter deposition and electroplating processes to form thin-film titanium resistors (nominal impedance of 50 Ω, 2 μm ×10 μm, 50 nm thick), metal-insulator-metal capacitors (radii of 4.6 μm and 3.8 μm with SiO_2 insulator thickness of 200 nm) and meandered high-impedance microstrip transmission lines (width of 3 μm, lengths of 180 μm and 90 μm) on a 15 μm thick, high-resistivity (>20 kΩ-cm) silicon membrane. An image of the circuit prior to backside processing is shown in fig. 1(b). After the topside features of the diplexer have been formed, the SOI wafer is bonded topside-down to a temporary carrier to allow backside processing. Scattering parameter measurements of the diplexer show that the desired characteristics, but with a low-band to output low-pass characteristic with a soft roll-off. Modeling suggests this characteristic is associated with parasitic inductance and resistance contributed by the metallized the ground via.



(a) (b)

Figure 1. (a) Geometry of the "quasi-reflectionless" diplexer. (b) Scanning electron micrograph (SEM) of a SOI-implemented reflectionless diplexer circuit prior to backside processing.