A Picowatt CMOS Voltage Reference Using Independent TC and Output Level Calibrations

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***Abstract*— We propose a low-power voltage reference that enables independent adjustment of temperature sensitivity and output level. This design enhances the temperature sensitivity without impacting the output level distribution, in contrast to previous methods. The proposed circuit achieves this by integrating a separate control system that utilizes diode-connected pMOS transistors and an analog multiplexer for output level adjustment, along with biasing current control to improve the temperature sensitivity. In a 180-nm CMOS process, the prototype circuit generates a stable reference voltage averaging 192 mV, maintaining an accuracy of ±8.8 mV (±3σ) from 0 °C to 75 °C across ten samples. In addition, it consumes only 35.8 pW at 0.6 V and 25 °C.**

***Index Terms*— Calibration, low power, trimming, voltage reference.**

I. Introduction

WIRELESS sensing systems have shrunk to the millimeter scale, operating on the battery power [1], [2] or wirelessly transferred energy [3]. To maximize the energy efficiency during tasks and recharging, it is crucial to minimize the circuit power consumption. For example, a millimeter-scale temperature sensor can recharge using just 8.2 nA of indoor light (179 lx) [4]. However, size constraints limit harvested power to 12.8 nA due to the photovoltaic cell's dimensions (1.3 × 1.1 mm). The sensor can maintain energy autonomy with circuits consuming as little as 4.6 nA in the sleep mode. Therefore, the power-efficient circuit design is vital for advanced miniature wireless systems, whether to reduce the size or to incorporate additional features with limited energy resources.

One fundamental low-power technique is duty-cycling, which turns off most components and keeps only essential circuits active during the sleep mode. Always-on circuits significantly contribute to overall energy consumption, as the sleep mode dominates the active mode. A voltage reference is essential in these systems but must minimize the power consumption alongside other always-on circuits.

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Traditional voltage references commonly use bandgap reference methods based on bipolar junction transistors (BJTs). However, their high power consumption (e.g., 99 μW [5]) makes them unsuitable for millimeter-scale sensors. Low-power CMOS voltage references have been proposed, utilizing the subthreshold current injected into diode-connected transistors (e.g., 30 pW [6], 34 pW [7], and 137 pW [8]). While these designs reduce voltage spread, they often compromise temperature sensitivity (e.g., 37% [7] and 12% [8]).

This article introduces a low-power voltage reference that minimizes the voltage spread while maintaining temperature sensitivity, building upon our prior work (see [9]). It incorporates an output-level selection scheme into a CMOS subthreshold voltage reference, employing 400 diode-connected pMOS transistors and an analog multiplexer (mux) to reduce voltage spread. In addition, it integrates a biasing current control scheme to optimize the temperature sensitivity. In a 180-nm CMOS process, this circuit generates a stable voltage of 192 mV across 0 °C–75 °C, consuming only 35.8 pW at a 0.6-V supply voltage (V_{DD}) and room temperature. Across ten samples, it achieves a ±3σ inaccuracy of 8.8 mV, with a maximum difference of 5.5 mV for the entire temperature range—representing improvements of 4.5× and 1.1× over previous low-power CMOS voltage references that utilized calibration. This article employs absolute accuracy as a metric, making the design suitable for various applications, including nonratiometric sensing, signal thresholding, off-chip sensor readout, subthreshold biasing, energy source monitoring, and data converters [10].

Adjusting the output voltage using a resistor divider and an output mux is a common technique for voltage references and low-drop-output (LDOs) regulators. This study incorporates this concept into a picowatt voltage reference with notably reduced power consumption. It explores the complexities of implementing a low-power design by employing a low-power voltage divider featuring 400 diode-connected transistors, presenting a novel approach for creating an ultralow-power voltage reference.

This article is structured as follows. Section II explains the operation principle of the circuit. Section III covers the key design considerations. Section IV presents the prototype measurements and compares them with other published voltage references. Finally, Section V provides the conclusion.

II. Proposed Voltage Reference

Fig. 1 illustrates a previous voltage reference design [7], along with its reference voltage (V_{REF}) and temperature coef-

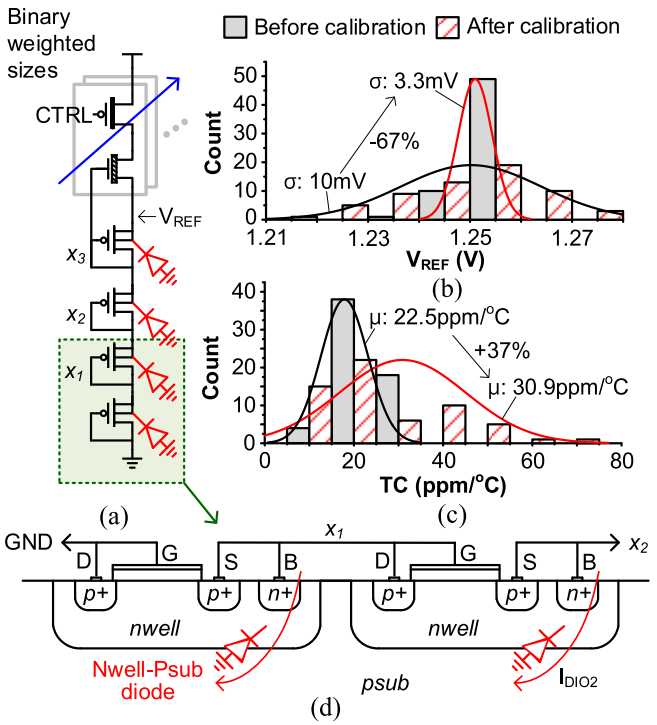

Fig. 1. Previous low-power CMOS voltage reference [7]. (a) Circuit. (b) V_{REF} distribution at single temperature. (c) TC. (d) Cross section of diode-connected pMOS transistors with Nwell–Psub diode.

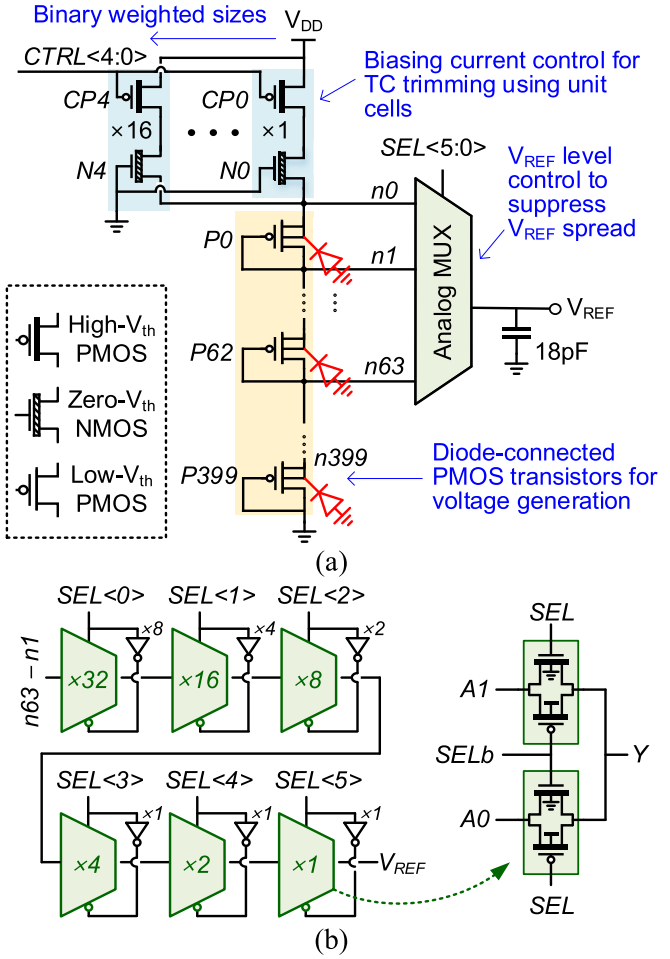

Fig. 2. Proposed voltage reference. (a) Overall circuit diagram. (b) Schematic of the 64-input analog mux.

ficient (TC) before and after calibration. This design generates a picowatt bias current through the top zero-threshold voltage (V_{th}) nMOS transistor, producing a stable V_{REF} by passing this current through several diode-connected pMOS transistors. The previous circuit achieves a V_{REF} of 1.25 V by employing four high-V_{th} pMOS transistors at the bottom. To reduce the output voltage variability, adjustments to V_{REF} can be made solely by modifying the width of the nMOS transistors. Notably, trimming is not applied to the bottom pMOS transistors to minimize the Nwell–Psub diode leakage current. Calibration significantly reduces the standard deviation (σ) of V_{REF} from 10 to 3 mV at a single temperature. However, it also increases the voltage variation across temperatures by 37% due to the deviation from the optimal configuration, which arises from the absence of a dedicated control mechanism.

Fig. 2(a) displays the proposed voltage reference mechanism, which generates V_{REF} over a temperature range of 0 °C–75 °C for typical applications. It achieves this using the top zero-V_{th} nMOS transistors (N0–N4) in combination with diode-connected pMOS transistors (P0–P399). The current passing through the diode-connected pMOS transistors is controlled by binary-sized sets of the top pMOS transistors (CP0–CP4) and nMOS transistors (N0–N4). Similar to the design in Fig. 1, trimming is not applied to the bottom pMOS transistors. Instead, it is exclusively applied to the nMOS transistors to prevent any further increase in the Nwell–Psub diode leakage current.

The current density and V_{th} of the bottom pMOS transistors are crucial in determining their drain–source voltage (V_{DS}) and temperature sensitivity. At higher temperatures, the subthreshold current increases exponentially while V_{th} decreases. V_{th}, influenced by the manufacturing process, directly affects the absolute voltage level and temperature sensitivity of the intermediate nodes ($n0$—$n399$). These nodes can be adjusted using the current control block (CP0–CP4 and N0–N4). However, inherent process variations can lead to voltage spreading when fine-tuning for minimal temperature sensitivity.

The current control block is based on a unit cell that includes a high-V_{th} pMOS and a zero-V_{th} nMOS transistor, enhancing linearity, while accounting for leakage current through the pMOS switch. In addition to temperature sensitivity calibration, our design features offer a trimming knob to adjust V_{REF}, minimizing voltage variation due to the temperature and process factors. Specifically, P0–P399 generates 400 distinct voltage levels, and the analog mux selects one of the top voltages ($n0$–$n63$) as V_{REF} using a 6-bit control signal (SEL).

Fig. 2(b) illustrates the detailed mux design. The body terminal of the pMOS in the mux is connected to V_{DD} to minimize layout size, which accounts for 13.3% of the total design. This configuration avoids the impact of the diodes between the n-well and sources across most supply voltage ranges (e.g., <2.6 V). If the body were connected to the source, additional N-well/Psub diodes would be introduced to P0–P399, further degrading the TC performance of the voltage reference, even at the low supply voltage.

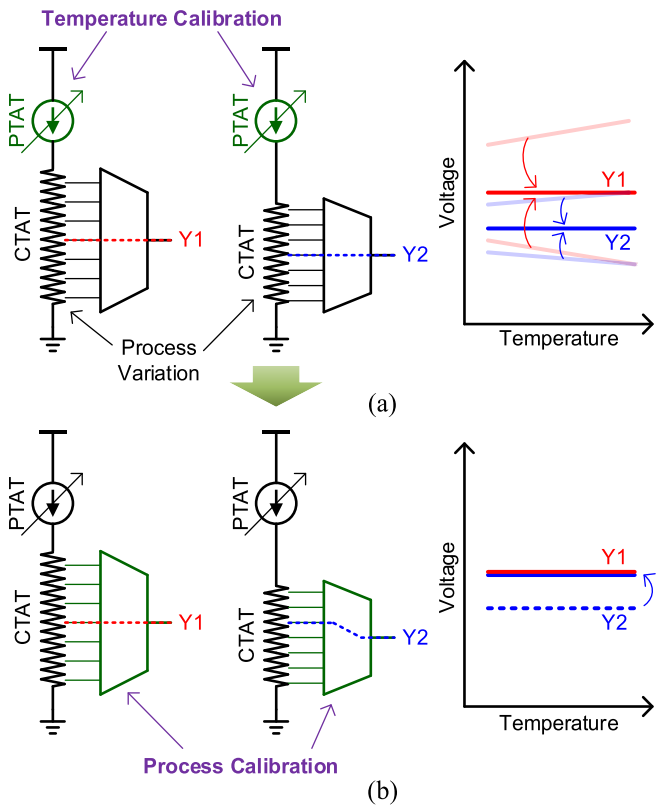

Fig. 3. Proposed calibration approaches. (a) Temperature calibration. (b) Process calibration.

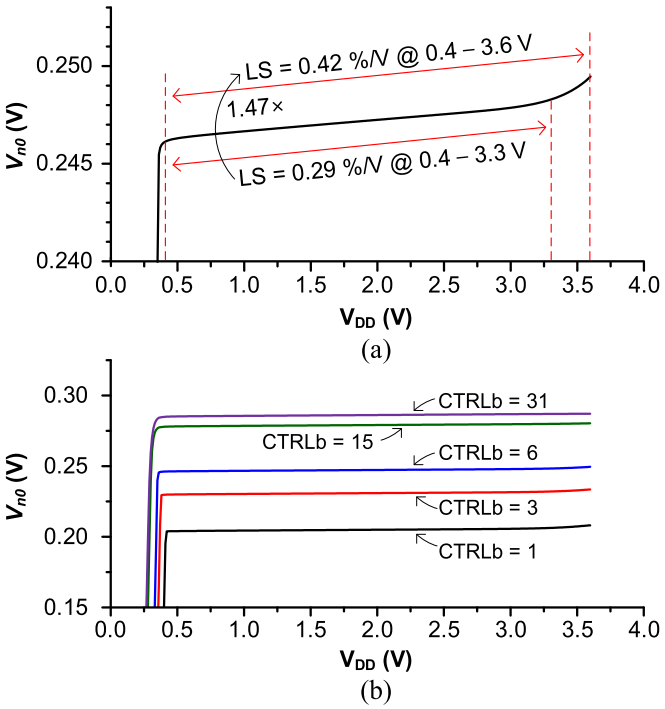

Fig. 4. Supply sensitivity of V_{n0} without including the mux. (a) CTRLb = 6. (b) Different CTRLb.

Fig. 3 visually demonstrates how the proposed circuit effectively mitigates temperature sensitivity and process variation. The top proportional to absolute temperature (PTAT) currents are generated by N0–N4 in Fig. 2, while the bottom resistors represent the resistance through P0–P399. These elements exhibit an exponential relationship between voltage and current in the subthreshold region; however, we simplify this behavior using a current source and a resistor for a linear approximation.

Initially, we calibrate each voltage reference to reduce TC by adjusting the PTAT current value through the CTRL parameter in Fig. 2. Due to resistance variations from different manufacturing processes, the calibrated voltages may differ between circuits, as shown in Fig. 3(a). To address this, our design includes an additional calibration step that selects an appropriate resistor tap using a mux to achieve identical output voltage levels, as illustrated in Fig. 3(b). This adjustment ensures that the temperature sensitivity, compensated in the initial step, remains consistent across circuits. The trimming also corrects simulation mismatches in transistors operating in the subthreshold region.

N0–N4 and P0–P399 operate in the subthreshold region, where the subthreshold current is described by the equation [11]

$$I_d = \mu C_{\text{ox}} \frac{W}{L}(m-1)V_T^2 e^{\left(\frac{V_{\text{gs}}-V_{\text{th}}}{mV_T}\right)}\left(1-e^{-\frac{V_{\text{ds}}}{V_T}}\right). \quad (1)$$

Here, μ represents the mobility, C_{ox} is the oxide capacitance, W and L are the transistor's width and length, m is the subthreshold slope factor, and V_{T} is the thermal voltage. The same current flows through the combined N0–N4 and each P0–P399. Assuming that all P0–P399 are identical, we derive the following equation:

$$\mu_1 C_{\text{ox1}} \frac{W_1}{L_1}(m_1-1)V_T^2 e^{\left(\frac{-V_{n0}-V_{\text{th1}}}{m_1 V_T}\right)}\left(1-e^{-\frac{V_{\text{DD}}-V_{n0}}{V_T}}\right) = \mu_2 C_{\text{ox2}} \frac{W_2}{L_2}(m_2-1)V_T^2 e^{\left(\frac{V_{n0}/N-|V_{\text{th2}}|}{m_2 V_T}\right)}\left(1-e^{-\frac{V_{n0}}{NV_T}}\right). \quad (2)$$

Here, W_1 is the total width of N0–N4 connected to V_{DD} through CP0–CP4, and L_1 is their length. W_2 and L_2 represent the size of each P0–P399. N denotes the total number of P0–P399 (e.g., 400 in the proposed circuit). V_{n0} refers to the source voltage for N0–N4 (or P0).

Importantly, N0–N4 maintain a V_{DS} greater than $6V_{\text{T}}$ at the minimum V_{DD} of 0.6 V. This allows the term $1 - \exp\{-(V_{\text{DD}} - V_{n0})/V_{\text{T}}\}$ to be approximated as 1 with less than 0.3% error, ensuring excellent line sensitivity (LS) or regulation against supply voltage changes without complex amplifier design. Fig. 4(a) shows the LS of V_{n0} as V_{DD} ranges from 0.4 to 3.6 V with CTRL = 11 001. Simulations include Nwell–Psub diode leakage from P0 to P399 but exclude the analog mux, achieving a competitive LS of 0.29%/V for V_{DD} from 0.4 to 3.3 V. However, the supply sensitivity degrades when V_{DD} exceeds 3.3 V due to increased subthreshold current from drain-induced barrier lowering (DIBL). Between 3.3 and 3.6 V, LS increases from 0.29 to 0.42%/V (1.47×). In Fig. 4(b), we observe V_{n0} with varying CTRL values. As CTRL decreases (higher CTRLb), the top nMOS transistor injects more current into the bottom pMOS transistors, resulting in a higher voltage.

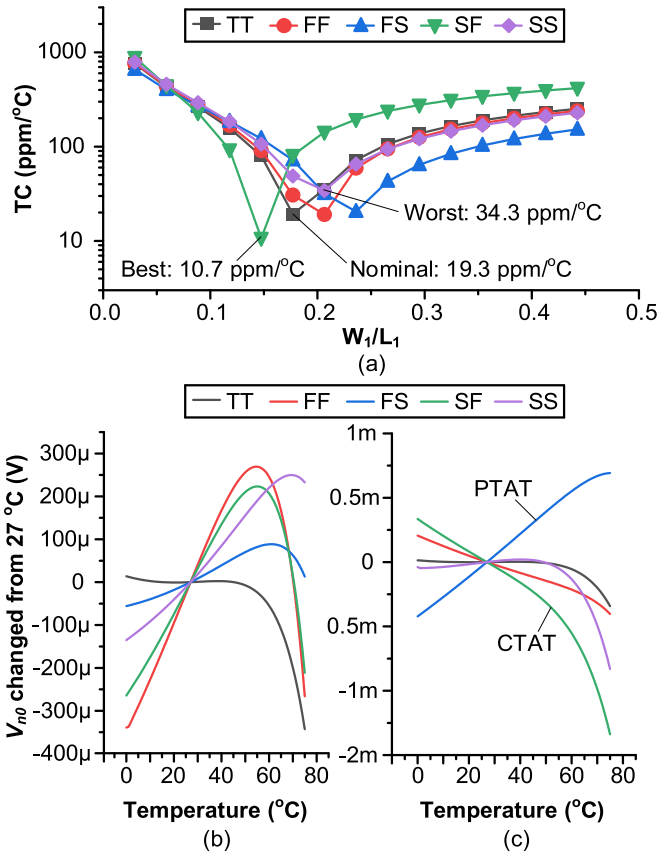

Fig. 5. Temperature sensitivity of V_{n0} at different corners without the mux. (a) TC versus W_1/L_1. (b) V_{n0} changed from 27 °C with the optimal W_1/L_1 at each corner. (c) V_{n0} changed from 27 °C with the same W_1/L_1 optimized at TT.

Dealing with the term $1 - \exp\{-V_{n0}/NV_T\}$ on the right-hand side of (2) is challenging due to the small value of V_{n0}/NV_T, which is 0.0215 in this design. This allows us to approximate the term as V_{n0}/NV_T using $e^x \approx 1 + x$ for small x. Consequently, (2) can be expressed as follows:

$$\mu_1 C_{\text{ox1}} \frac{W_1}{L_1}(m_1 - 1)e^{\left(\frac{-V_{n0}-V_{\text{th1}}}{m_1 V_T}\right)} = \mu_2 C_{\text{ox2}} \frac{W_2}{L_2}(m_2 - 1)e^{\left(\frac{V_{n0}/N-|V_{\text{th2}}|}{m_2 V_T}\right)}\left(\frac{V_{n0}}{NV_T}\right). \quad (3)$$

Rearranging gives us

$$\frac{V_{n0}}{NV_T}e^{\left\{\left(\frac{N}{m_1}+\frac{1}{m_2}\right)\frac{V_{n0}}{NV_T}+\frac{V_{\text{th1}}}{m_1 V_T}-\frac{|V_{\text{th2}}|}{m_2 V_T}\right\}} = \frac{\mu_1 C_{\text{ox1}}(W_1/L_1)(m_1 - 1)}{\mu_2 C_{\text{ox2}}(W_2/L_2)(m_2 - 1)}. \quad (4)$$

The format $V_{n0} \cdot e^{\alpha V_{n0}+\beta} = \gamma$ indicates a unique solution for V_{n0} since γ is positive. However, (4) complicates matters by including "V_{n0}/NV_T" on the left-hand side, making it difficult to derive a closed-form solution for V_{n0} and address its insensitivity to temperature changes, as shown in [7].

To address this challenge, Fig. 5(a) presents an alternative approach to minimize the TC of V_{n0} by adjusting the sizes of N0–N4, while keeping P0–P399 constant across various corners. This adjustment makes V_{REF} PTAT with large W_1/L_1 ratios, and complementary to absolute temperature (CTAT) with small W_1/L_1 ratios. Fig. 5(b) shows V_{n0}'s voltage variation at 27 °C with optimized transistor sizes, achieving a low TC of 10.7–34.3 ppm/°C. The proposed design effectively compensates for TC through proper transistor sizing and maintains a small V_{DS} for P0–P399. Fig. 5(c) further demonstrates how the W_1/L_1 optimization at the typical–typical (TT) corner applies to all other corners.

TABLE I
TRANSISTOR SIZES OF THE DESIGNED CIRCUIT

	Unit transistors of *CP0 – CP4*	Unit transistors of *N0 – N4*	*P0 – P399*	NMOS (PMOS) of Mux
W/L (µm)	0.44 /0.70	0.59 /20	8.77 /0.30	0.35/0.30 (0.30/0.30)

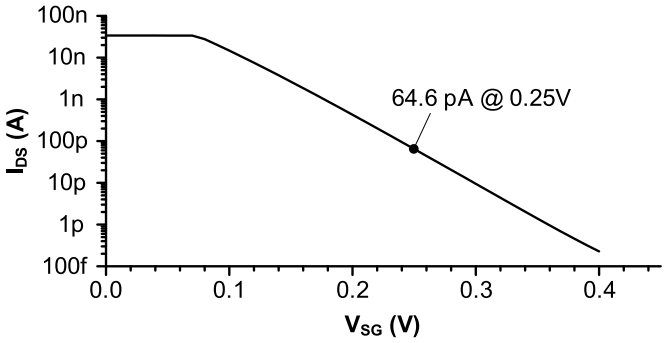

Fig. 6. Drain current versus V_{SG} of the top nMOS transistor. V_{SG} equals V_{n0} in the proposed circuit.

III. CIRCUIT DESIGN

Table I details the transistor sizes used in our circuit design. CP0–CP4 and the transistors in the analog multiplexer act as digital switches, so they are sized either at minimum or slightly larger values to minimize device mismatch. For P0–P399, the dimensions (W_2 and L_2) were selected based on factors, such as current consumption, desired V_{n0} level, and target V_{REF} control step. Fig. 6 shows the relationship between V_{SG} and I_{DS} at W_1/L_1 dimensions of 3.54/20 μm (with CTRL set to 11 001) and V_{DD} of 0.6 V. At these settings, V_{n0} is approximately 250 mV, achieving an I_{DS} of 64.6 pA. W_1/L_1 reflects the total size of the turned-on transistors (N0–N4), determined by the CTRL setting. For CTRL = 11 001, N2 and N1 are activated, resulting in a W_1/L_1 of 0.177 (3.54/20 μm), which matches the optimal size shown in Fig. 5(a) under the TT corner conditions.

Between V_{n0} and ground, there is a series connection of 400 transistors (P0–P399). This number was chosen to balance V_{REF} control step size, transistor area, and TC. Using more transistors would reduce the voltage step size but increases the circuit area and worsen TC due to larger current differences between upper (P0) and lower (P399) pMOS transistors. The current decreases from P0 to P399 due to Nwell–Psub diode leakage.

Fig. 7(a) shows the current (I_{BOT}) through the bottom transistor (P399) compared with P0 (I_{P0}) at different numbers of transistors at 75 °C, and TC, excluding the mux. Fig. 7(b) illustrates how V_{n0} changes with temperature. Larger

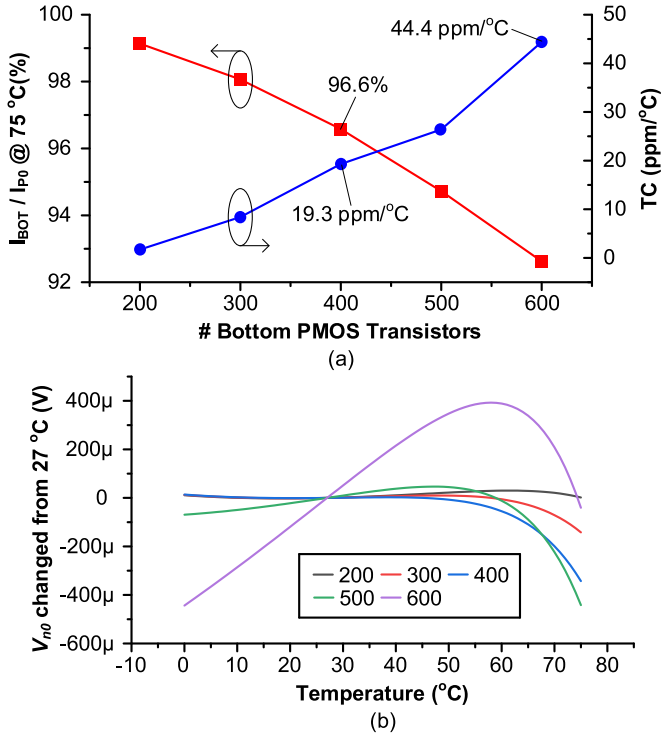

Fig. 7. Impact of the number of the bottom pMOS transistors. (a) Ratio of the current through very bottom pMOS transistor and the supply current and TC across the number of pMOS transistors. (b) Normalized V_{n0} across temperature with different number of the bottom pMOS transistors.

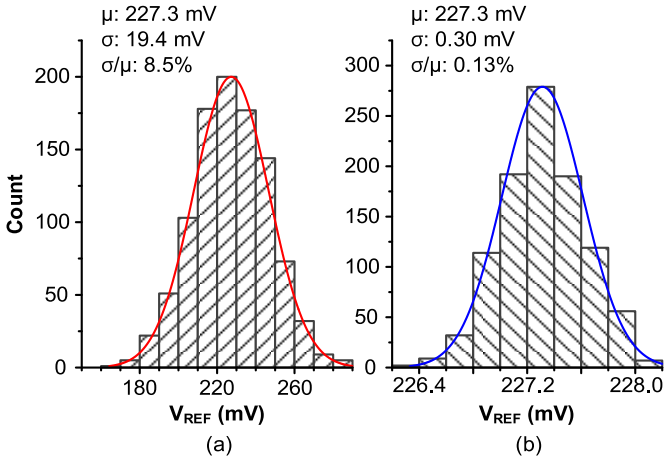

Fig. 8. Distribution of V_{REF}. (a) Process variation and device mismatch. (b) Device mismatch only.

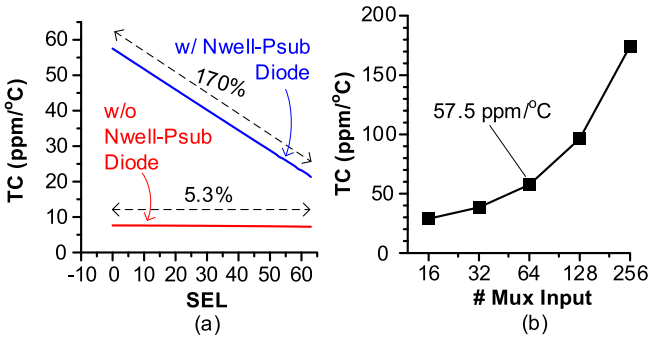

Fig. 9. Impact of the mux on TC. (a) TC versus SEL. (b) TC versus the number of the mux inputs.

current imbalances worsen V_{n0}'s curvature and TC. As the number of transistors varies from 200 to 600, while W_2/L_2 remains constant. As the transistor count increases, V_{REF} rises from 246 to 252 mV at 27 °C, and the supply current decreases from 150 to 50.4 pA. Without N-well-to-Psub diodes, a design with 600 transistors achieves a TC of 8.8 ppm/°C, indicating that unbalanced current, not decreased current, is the primary cause of TC degradation.

The 400-transistor configuration provides a V_{REF} control step of 0.625 mV, only 2.1× larger than the worst-case variation (0.3 mV) across temperatures and supply voltages. W_2/L_2 is set to 8.77/0.3 μm, drawing 74.2 pA at V_{n0} = 246 mV using a low-V_{th} pMOS transistor. pMOS transistors are preferred over nMOS for V_{REF} generation because nMOS requires deep n-wells to avoid body effects, leading to larger areas and increased spacing between transistors.

To improve TC compensation, the top nMOS transistors are divided into five binary-sized groups, totaling 63 fingers. Each unit transistor in these groups is sized at 0.59/20 μm. This arrangement reduces TC from 35 to 80 to 20 ppm/°C with minor CTRL adjustments near the optimal point. It also allows flexibility to increase the current up to four times the designed value, compensating for potential deviations like reduced pull-up current from N0 to N4 or increased pull-down current from P0 to P399, which may arise due to inaccurate modeling, especially in the picowatt range.

The analog mux consists of six-stage transmission gates made with high-V_{th} thick-oxide transistors to minimize leakage and support V_{DD} voltages above 1.8 V. While there are 400 possible output nodes ($n0$–$n399$), only the top 64 are connected to the mux, balancing leakage current concerns and required output voltage levels for load circuits. These 64 nodes allow fine-tuning of V_{REF} within a 38.8-mV range, determined as 2σ of V_{REF} from a 1000-sample Monte-Carlo simulation accounting for process and mismatch variations, as shown in Fig. 8.

Fig. 9(a) shows how TC varies with different mux selection bits (SEL). When SEL changes from 0 (min.) to 63 (max.), TC increases by 170% when Nwell–Psub diodes are present, with the highest V_{REF} (V_{n0}) optimized for TC. However, TC worsens at lower V_{REF} levels due to increased current imbalances from diode leakage. Without the diodes, TC changes by only 5.3%, with a maximum of 7.64 ppm/°C at SEL = 0, and a minimum of 7.26 ppm/°C at SEL = 63. TC decreases monotonically from SEL = 0 to SEL = 63, primarily due to the reduction in V_{REF}. The low supply voltage (0.6 V) minimizes the impact of mux leakage. Fig. 9(b) shows the worst-case TC changes for different mux input counts. To maintain consistent V_{REF} control, mux inputs are connected sequentially from V_{n0} to lower taps without skipping. As the number of inputs increases, minimum V_{REF} decreases, leading to higher TC. With the selected 64-input mux, a TC of 57.5 ppm/°C is achieved.

Fig. 10 shows the TC variation across V_{DD} from 0.4 to 3.6 V with the lowest V_{REF} selected. Below 0.6 V, the mux's

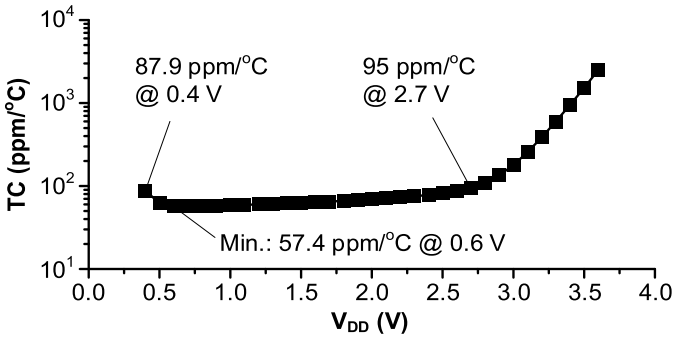

Fig. 10. TC of V_{REF} across the supply voltages.

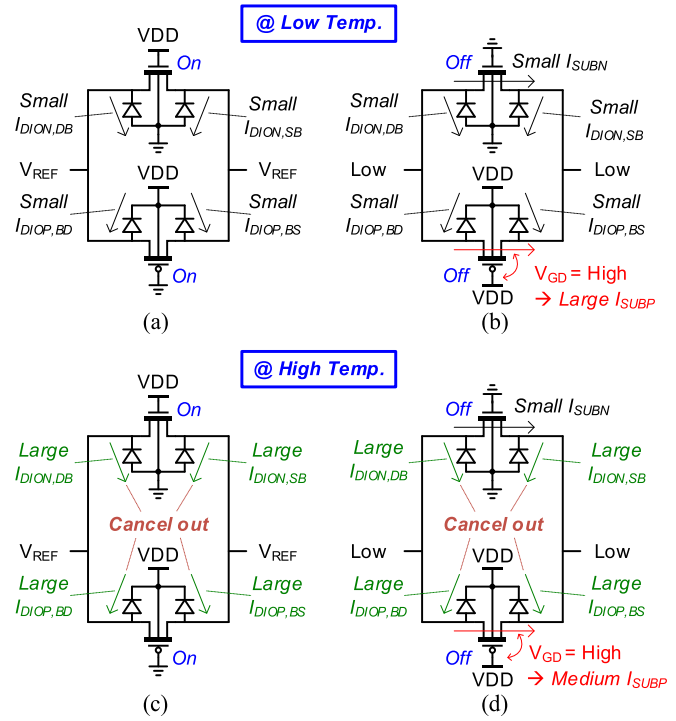

Fig. 11. Leakage currents in mux transmission gates at high V_{DD}. (a) Turned-on gate at low temperature. (b) Turned-off gate at low temperature. (c) Turned-on gate at high temperature. (d) Turned-off gate at high temperature.

high-V_{th} transmission gates are not fully activated, causing TC degradation. Above 2.6 V, DIBL increases leakage currents in the top nMOS switches (N0–N4), raising TC. The circuit maintains a TC below 95 ppm/°C up to 2.7 V, with W_1/L_1 optimized for 0.6 V. At higher V_{DD}, adjusting W_1/L_1 improves TC, reaching 38.8 ppm/°C at 3.0 V and 137.7 ppm/°C at 3.3 V.

Fig. 11 shows the mux leakage currents at high V_{DD} under low and high temperatures. The mux transmission gate has six key leakage currents: $I_{DION,DB}$, $I_{DION,SB}$, $I_{DIOP,BD}$, $I_{DIOP,BS}$, I_{SUBN}, and I_{SUBP}. $I_{DION,DB}$ and $I_{DION,SB}$ are reverse-biased diode leakage currents between the nMOS body (ground) and drain/source, while $I_{DIOP,DB}$ and $I_{DIOP,SB}$ are similar currents between the pMOS body (V_{DD}) and drain/source. I_{SUBN} and I_{SUBP} are the subthreshold leakage currents between the drain and source when the transistor is off. At low temperatures [Fig. 11(a) and (b)], the turned-off pMOS transistor

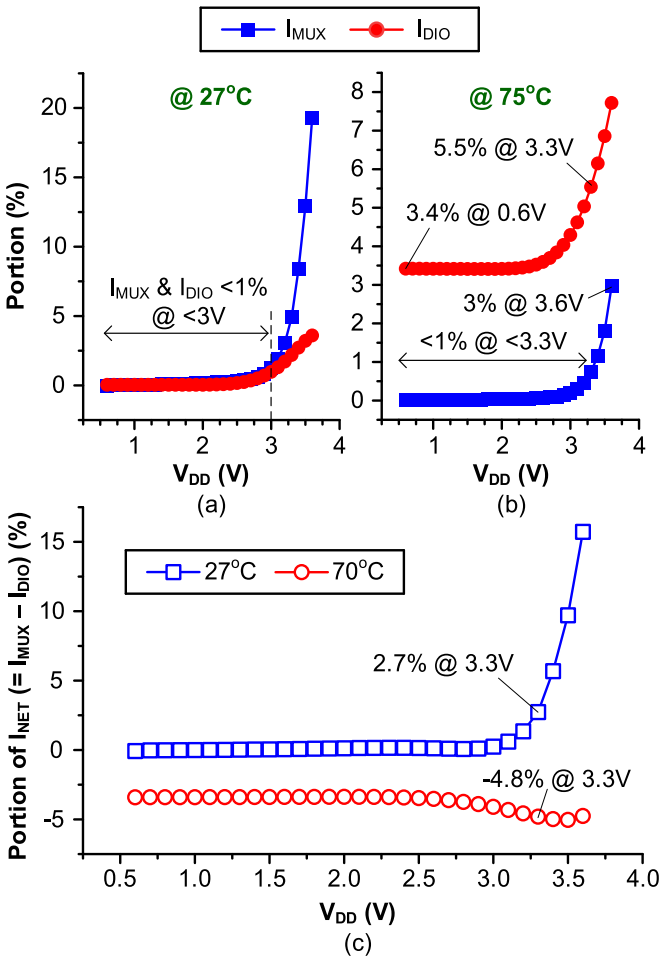

Fig. 12. Portion of I_{MUX}, I_{DIO}, and "$I_{MUX} - I_{DIO}$" across V_{DD}. (a) I_{MUX} and I_{DIO} at 27 °C. (b) I_{MUX} and I_{DIO} at 75 °C. (c) "$I_{MUX} - I_{DIO}$" at 27 °C and 75 °C.

experiences a large gate-to-drain voltage (V_{GD}), causing significant I_{SUBP} due to gain-induced drain leakage (GIDL) [12], which degrades LS at high V_{DD} by shorting the mux's input nodes ($n0$–$n63$). In contrast, nMOS transistors have a small V_{GD}, resulting in minimal leakage. At high temperatures [Fig. 11(c) and (d)], reverse-biased diode leakage currents ($I_{DION,DB}$, $I_{DION,SB}$, $I_{DIOP,BD}$, and $I_{DIOP,BS}$) increase significantly, surpassing I_{SUBN} and I_{SUBP}. However, their impact on TC is minimal since diode leakage becomes independent of voltage across it (V_D) for $V_D > 150$ mV [6], [7], and they cancel out. According to the diode current equation

$$I_{DIO} = I_S\left(1 - e^{-\frac{V_D}{V_T}}\right) \approx I_S \tag{5}$$

where I_S depends on intrinsic carrier concentration (n_i^2) and diffusion coefficients. For $V_D > 150$ mV, the exponential term becomes negligible (0.3% error), making diode leakage nearly constant. While most diode leakages cancel out, the N-well–Psub diode leakage (I_{DIO}) at the main branch does not, dominating overall leakage.

Fig. 12(a) and (b) shows the current components through the mux (I_{MUX}) and the Nwell–Psub diode leakage (I_{DIO}) at 27 °C and 75 °C. Notably, "$I_{P0} + I_{MUX}$" equals "$I_{P399} + I_{DIO}$,"

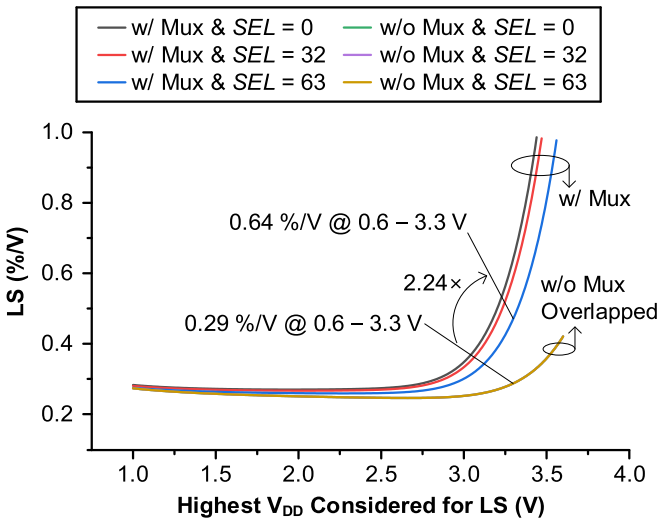

Fig. 13. LS of V_{REF} for different highest V_{DD} w/ and w/o including the Nwell–Psub diodes, when SEL is chosen as 0, 32, or 63.

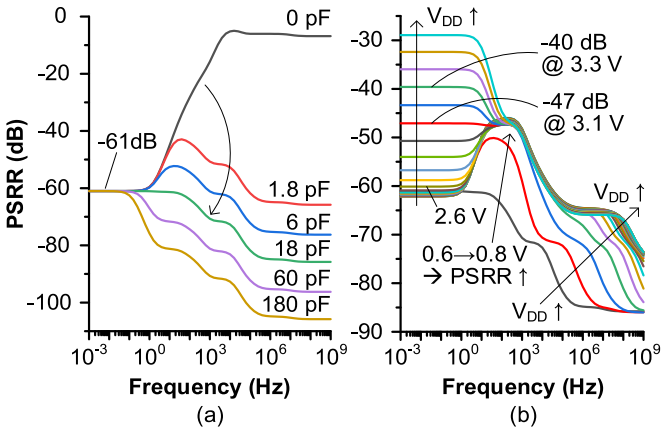

Fig. 14. PSRR versus frequency. (a) PSRR with different output decoupling capacitances. (b) PSRR with a different V_{DD}.

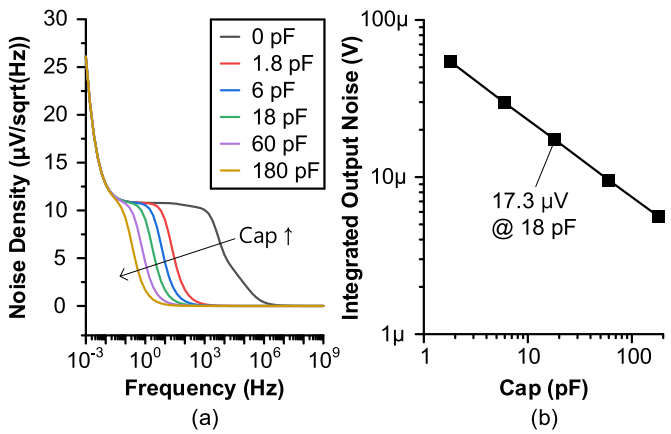

Fig. 15. Output noise. (a) Noise density over frequency with different output decoupling capacitances. (b) Integrated output noise versus output decoupling capacitances.

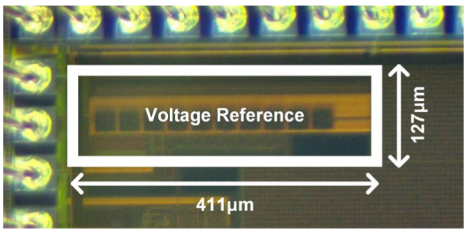

Fig. 16. Prototype chip photograph.

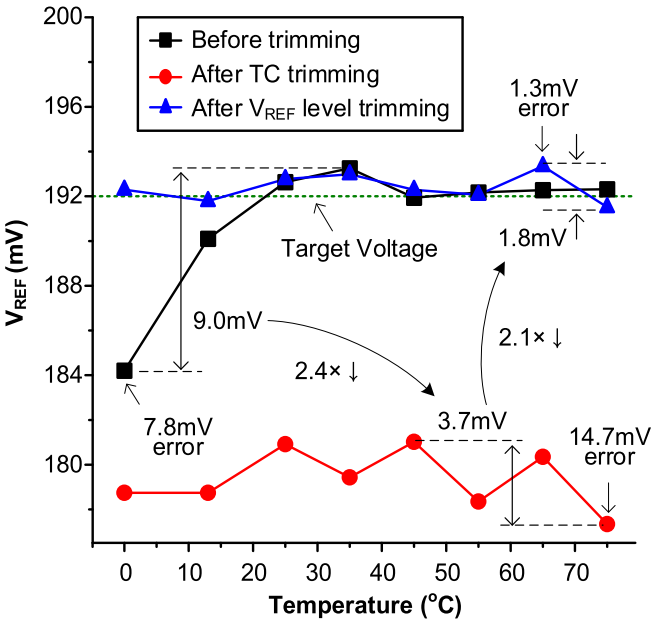

Fig. 17. Measured V_{REF} with calibration from single sample.

accounting for 100% of the current. I_{P0} and I_{P399} represent the currents through transistors P0 and P399, respectively. I_{P0} and I_{MUX} originate from V_{DD}, while I_{P399} and I_{DIO} flow toward the ground. I_{MUX} represents the total leakage from all 64 mux inputs, and along with I_{DIO}, causes current imbalance among the P0–P399 transistors. Fig. 12(c) shows the net current (I_{NET}), calculated as I_{MUX}–I_{DIO}. At 27 °C, both I_{MUX} and I_{DIO} remain under 1% for V_{DD} below 3.0 V. Above 3.0 V, I_{MUX} increases faster than I_{DIO}, leading to I_{NET} reaching +2.7% at 3.3 V. At 75 °C, I_{MUX} exceeds 1% at V_{DD} above 3.4 V, reaching 3.0% at 3.6 V, while I_{DIO} stays above 3.4% even at a low V_{DD} (0.6 V), peaking at 5.5% at 3.3 V. As a result, I_{NET} shows −4.8% at 3.3 V. This behavior occurs because subthreshold current (I_{P0} and I_{P399}) and I_{DIO} increase more with temperature than the mux's GIDL current (I_{MUX}). Thus, I_{MUX} has less impact at high temperatures, significantly affecting TC at V_{DD} above 3.0 V, as shown in Fig. 10.

Fig. 13 shows how LS changes with and without the mux at the maximum, center, and minimum V_{REF} settings. I_{MUX} increases LS by 2.24×, from 0.29%/V (without I_{MUX}) to 0.64%/V (with I_{MUX}) over the V_{DD} range from 0.6 to 3.3 V for the minimum V_{REF} (worst case scenario).

An 18-pF metal-to-metal (MIM) capacitor is connected to V_{REF} to improve the power supply rejection ratio (PSRR). Fig. 14(a) shows how PSRR varies with different output decoupling capacitances. The 18-pF capacitor is chosen to reduce PSRR at frequencies above 1 Hz, lowering it below the dc level (−61 dB). Fig. 14(b) illustrates PSRR versus

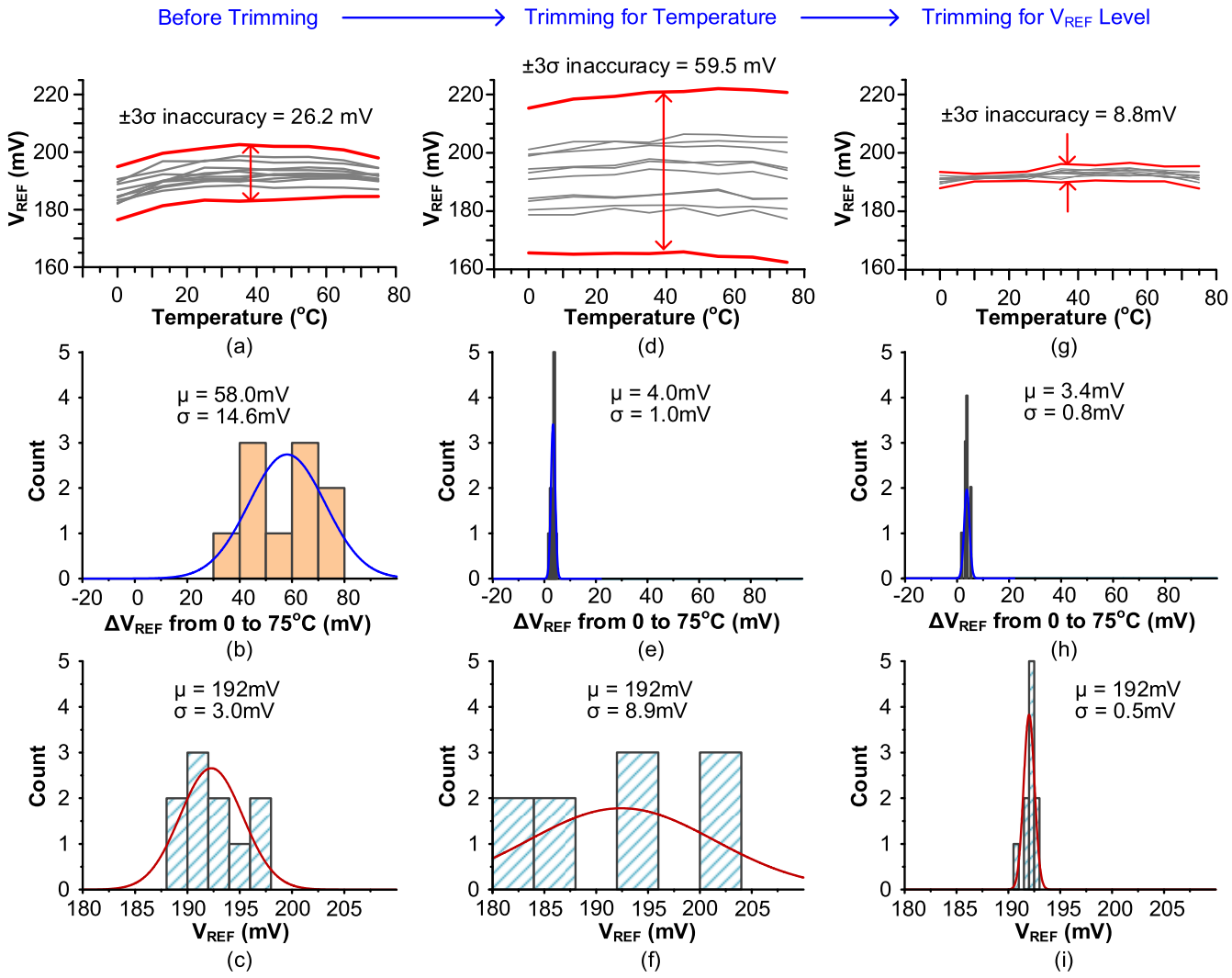

Fig. 18. Measured voltage V_{REF} from ten samples. (a)–(c) Before calibration. (d)–(f) After TC trimming. (g)–(i) After V_{REF} level trimming. (a), (d), and (g) V_{REF} across temperatures. (b), (e), and (h) Histogram of V_{REF} range from 0 °C to 75 °C. (c), (f), and (i) Histogram of V_{REF} at 25 °C.

V_{DD}. As V_{DD} increases from 0.6 to 0.8 V, PSRR peaks around 10 and 100 Hz due to better activation of high-V_{th} transmission gates. Beyond 2.6 V, PSRR at low frequencies increases significantly, surpassing the −47-dB level around 10 and 100 Hz at 3.1 V, due to GIDL effects in the mux. At V_{DD} up to 3.3 V, PSRR reaches −40 dB.

Fig. 15 depicts the noise spectrum and integrated noise with various decoupling capacitors. The 18-pF capacitor reduces integrated output noise from 1.64 mV (without capacitor) to 17.3 μV, a 95× reduction.

IV. Experimental Results

The proposed voltage reference is fabricated using a 180-nm CMOS process, occupying a total area of 0.052 mm^2 (Fig. 16). The performance is evaluated using a sample of ten devices, with measurements taken via on-chip analog buffers and a 24-bit NI-9239 voltage input module. The buffer's offset is calibrated using an external input through a separate analog multiplexer. The power consumption was measured with a Keithley 2450 sourcemeter. For optimization, V_{REF} is calibrated at 25 °C and 65 °C by adjusting the current control switches (CP0–CP4), with SEL fixed at 32. At 25 °C, SEL is then adjusted to fine-tune V_{REF} to a target voltage (e.g., 192 mV) while maintaining the optimized CTRL settings for best temperature performance. This target voltage is intended for subthreshold computing applications, minimizing energy use in digital signal processing. The reference voltage can also be used to design an LDO to supply subthreshold circuits, such as a 180-mV FFT processor [13].

Fig. 17 shows the measured V_{REF} from a voltage reference circuit using the proposed calibration process. Before calibration, V_{REF} varies by 9.0 mV across 0 °C–75 °C. The temperature calibration reduces this variation to 3.7 mV (a 2.4× improvement), though it remains 14.7 mV off the target at its maximum deviation. After adjusting the SEL control, V_{REF} reaches 192.8 mV, with a 2.1× reduction in temperature variation. The maximum V_{REF} error from the target voltage is reduced from 7.8 to 1.3 mV (a 6.0× improvement) across 0 °C–75 °C, covering the commercial temperature range [14]. While typical CMOS junction temperatures can reach up to 85 °C, the target subthreshold computing application, with its low power consumption, is expected to stay

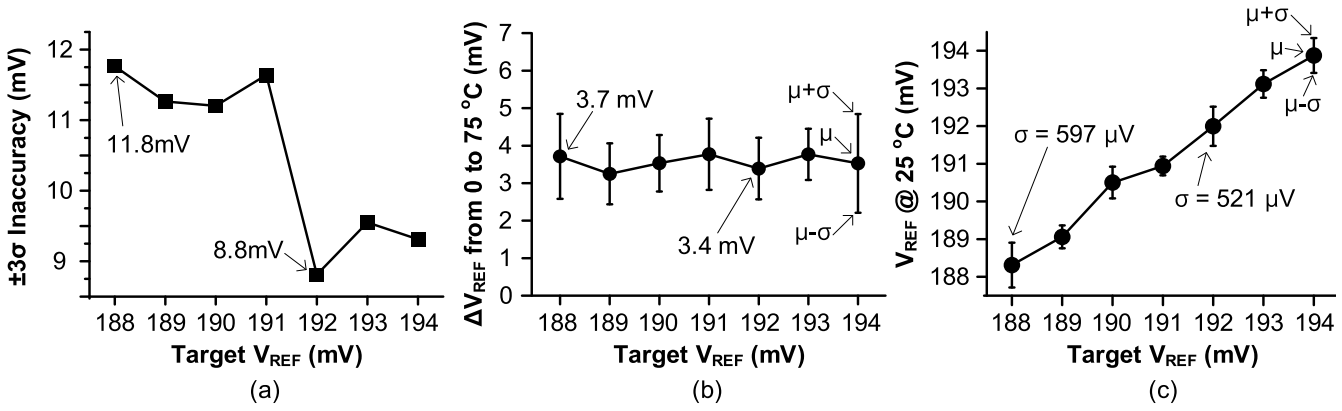

Fig. 19. Measured V_{REF} for different target V_{REF} levels from ten samples. (a) $\pm 3\sigma$ inaccuracy. (b) V_{REF} variation from 0 °C to 75 °C. (c) V_{REF} at 25 °C.

below 75 °C. It is important to note that the circuit's TC increases significantly below 0 °C and above 75 °C due to reduced subthreshold current and increased leakage current at those extremes.

Fig. 18 shows the measured V_{REF} data from ten samples, highlighting the effects of calibration. Before calibration, V_{REF} has a $\pm 3\sigma$ inaccuracy of 26.2 mV across the temperature range [Fig. 18(a)], with an average temperature variation of 58 mV [Fig. 18(b)] and a σ of 3 mV at 25 °C [Fig. 18(c)]. After the two-point calibration, the $\pm 3\sigma$ inaccuracy increases to 59.5 mV due to sample variation [a 2.3× increase, Fig. 18(d)], but the average temperature variation drops significantly to 4 mV [a 14.5× reduction, Fig. 18(e)], while σ at 25 °C rises to 8.9 mV [a 3× increase, Fig. 18(f)]. Following SEL adjustment, the $\pm 3\sigma$ inaccuracy improves to 8.8 mV [a 6.8× reduction, Fig. 18(g)], and temperature sensitivity improves by a 25% [Fig. 18(h)] and σ at 25 °C decreases to 0.5 mV [a 17.8× improvement, Fig. 18(i)]. Overall, the calibration technique reduces the $\pm 3\sigma$ inaccuracy, temperature sensitivity, and σ at 25 °C by 3×, 19.3×, and 6×, respectively, across the 0 °C to 75 °C range.

Fig. 19 shows the measured V_{REF} data after calibration for different target values ranging from 188 to 194 mV across ten samples. In the worst case, with a target V_{REF} of 188 mV, the $\pm 3\sigma$ inaccuracy of 11.8 mV, with an average temperature variation of 3.7 mV and a σ of 597 μV at 25 °C.

Fig. 20 presents the measured LS performance, achieving 0.42%/V as V_{DD} varies from 0.6 to 3.0 V. This stability is due to zero-V_{th} nMOS transistors buffering against power supply variations, allowing a wide V_{DD} range. LS remains stable even beyond 3.3 V, differing from simulation predictions, likely because GIDL is modeled weaker than in the fabricated chip. As seen in the simulation results (Fig. 10), V_{REF} remains stable as V_{DD} decreases, but only down to 0.6 V due to the use of high-V_{th} transmission gates in the analog mux.

The measured low-frequency PSRR is −39 dB, significantly lower than the simulated value of −61 dB (Fig. 14). This degradation is likely due to the higher leakage current in the mux of the fabricated device compared to the simulation. Additional factors, such as layout issues (e.g., pads and dummy fill), instrument connections, and chip packaging, may also contribute to the lower PSRR.

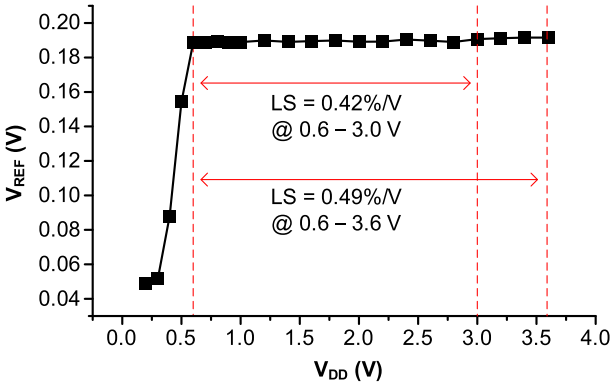

Fig. 20. Measured V_{REF} across V_{DD}.

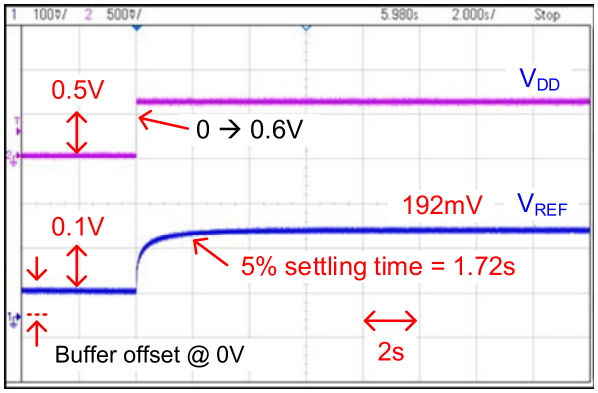

Fig. 21. Measured start-up waveform.

Fig. 21 shows the start-up waveform with a 5% settling time of 1.7 s. Fig. 22(a) illustrates the current consumption as V_{DD} increases from 0.6 to 3.6 V at 25 °C, rising by 1.3×. However, this increase is less significant compared with the temperature-induced variations in Fig. 22(b), as the subthreshold biasing current remains stable when V_{DS} of N0–N4 exceeds 3–4V_T [6].

Table II shows the comparison of our proposed voltage reference with state-of-the-art CMOS references that use calibration techniques. Using our proposed calibration method, the circuit achieves the lowest inaccuracy over a temperature range

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH THE PREVIOUS LOW-POWER CMOS VOLTAGE REFERENCES EMPLOYING CALIBRATION

Parameters		This work	[7] JSSC 2017	[8] ASSCC 2017	[15] TCAS-I 2017	[16] ESSCIRC 2018	[17] TCAS-II 2018	[18] TCAS-II 2021	[19] TVLSI 2018
Process (nm)		180	180	180	180	180	180	180	180
V_{REF} (V)		0.19	1.25	1.17	0.23	0.21	0.76	0.99	0.76
Supply Voltage (V)		0.6 – 3.6	1.4 – 3.6	1.8 – 3.6	0.45 – 3.3	0.5	1.0	1.5 – 6.0	1.1
Operating Temp. (°C)		0 – 75	0 – 100	0 – 170	0 – 120	-40 – 125	-40 – 125	-40 – 85	-15 – 140
V_{REF} Variation (mV) @ Temp. Range w/ Multiple Sample	±3σ	8.8	25.0	40.0	N/A	N/A	N/A	N/A	N/A
	Max – Min	5.5	N/A	N/A	17.8	6.0	36.1	64	23
TC (ppm/°C)		128 – 304	11 – 73	32 – 106	72	11	74	61	34
#Samples		10	60	40	5	6	63	6	15
Power (pW)		35.8	33.6	137	147	650	23,000	63,000	4,600
Line Sensitivity (%/V)		0.49	0.31	0.09	0.15	0.03	0.52	0.003	0.28
PSRR (dB)		-39	-41	-38	-44	-62	-52	-93	-9
Active Area (mm^2)		0.052	0.003	0.008	0.002	0.001	0.016	0.015	0.060

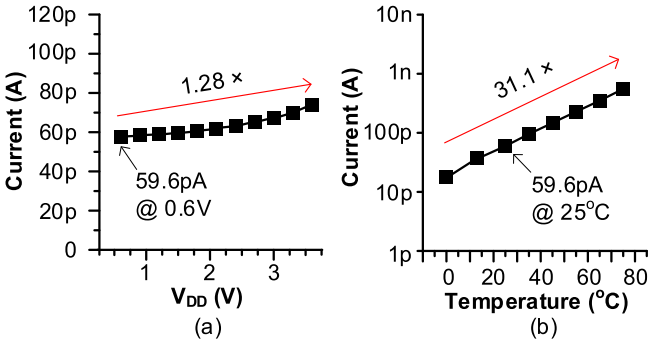

Fig. 22. Measured current consumption. (a) Across V_{DD} from 0.6 to 3.6 V at 25 °C. (b) Across temperatures from 0 °C to 75 °C with 0.6-V V_{DD}.

of 0 °C–75 °C, common in typical applications. Specifically, it attains a ±3σ inaccuracy that is 4.5× lower than [8] and a "max–min" value 1.1× smaller than [16]. V_{REF} variation across the range includes both TC and chip-to-chip variation, and our design excels in minimizing both, while maintaining competitive LS. It also consumes less power than most designs, except for [7], where the difference is minimal (6.5%). The proposed output-level selection scheme (P0–P399) provides additional calibration options without significantly affecting TC. While this increases the active area, it remains comparable to [19].

Our design, like [6] and [7], leverages the threshold voltage difference between two transistors, but with comprehensive optimization to address both process and temperature variations. Unlike [15] and [16], which rely on stacked diode-connected nMOS transistors and trimming circuits to compensate for process variations, our approach uses a single nMOS transistor, decoupling current and voltage control. This enables independent mitigation of process and temperature variations, resulting in a "max–min" value 3.2× smaller than [15] and 1.1× smaller than [16].

V. CONCLUSION

We present a low-power CMOS voltage reference that independently adjustable temperature sensitivity and reference voltage. To ensure stable output voltage across varying temperatures without affecting reference voltage distribution, the design uses 400 diode-connected pMOS transistors and an analog mux for fine output level adjustment. It also includes bias current control for improved temperature performance. In a prototype of ten samples fabricated in a 180-nm CMOS process, the reference shows a ±3σ inaccuracy of 8.8 mV and a maximum deviation of 5.5 mV from 0 °C to 75 °C, while consuming just 35.8 pW at 0.6 V and 25 °C.

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