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A Continuously-Scalable-Conversion-Ratio SC Energy-Harvesting Interface with Exponential DCO for Wide Range Output Power Tracking

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***Abstract* — This paper presents an energy harvesting interface circuit utilizing a continuously-scalable-conversion-ratio (CSCR) switched-capacitor (SC) converter. The circuit integrates an exponential digital control oscillator (DCO) and a compact capacitive divider to facilitate maximum power point tracking (MPPT) across a wide power spectrum, ranging from 30 to 6,056 μW, which is 20 times broader than previous approaches. Fabricated using a 180 nm CMOS process, the prototype chip achieves a peak power conversion efficiency of 91.5% and can deliver a maximum output power of 6.05mW.**

Keywords* — *Continuously-scalable-conversion-ratio (CSCR), energy harvesting, switched capacitor DC-DC converter, maximum power point tracking (MPPT).

I. Introduction

Energy harvesting (EH) offers significant benefits to small-scale systems by prolonging battery life or directly powering the system. This makes it an invaluable solution for enhancing the sustainability and autonomy of portable and remote devices. Photovoltaic (PV) sources are widely used in EH for small-scale systems due to their ability to generate substantial power from a small area, aligning with the trend towards sustainable energy usage. In energy harvesting interface (EHI), the DC-DC converter plays a crucial role in transferring voltage generated from EH sources to batteries or loads, ensuring efficient utilization of harvested energy according to the system's power requirements or charging needs. Ideally, these converters should use minimal bulky components (e.g., off-chip inductors) to enable broader application with a smaller form factor. Additionally, they should offer continuous voltage conversion ratios (VCR) to accommodate a wide range of EH source output voltages while maintaining high efficiency in power delivery.

Fig. 1 illustrates the difference between conventional DC-DC and Continuously-Scalable-Conversion-Ratio (CSCR) converters for energy harvesting applications. Conventional inductor-based converters require bulky off-chip components, while SC converters, though more compact, are limited by their discrete VCR and tend to have lower power transfer efficiency. In contrast, CSCR converters can be fully integrated, provide a continuous VCR suitable for a wide input voltage range, and exhibit high power transfer efficiency [1]. Previous EHIs utilizing CSCR converters employed SC-based PFM and hill-climbing methods for Maximum Power Point Tracking (MPPT) [2]-[3]. The SC-based PFM method is well-suited for some EH sources like TEGs, but its applicability to other energy sources is limited due to its assumption of a constant open circuit voltage to optimal harvesting voltage ratio [2]. The hill-climbing method, which requires accurate

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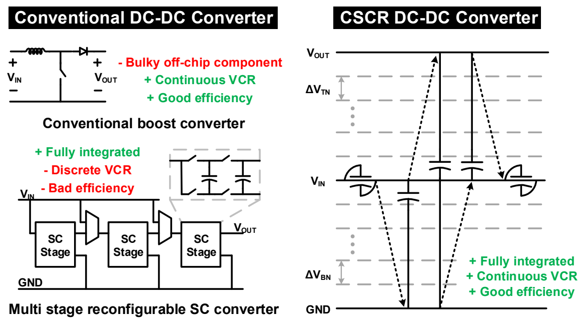

Fig. 1. Conventional DC-DC converter and CSCR DC-DC converter.

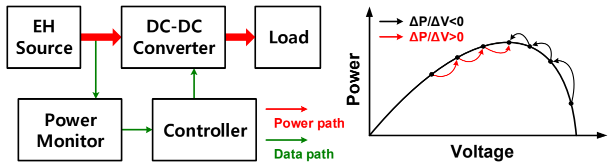

Fig. 2. EHI block diagram and hill-climbing algorithm.

power monitoring for MPPT, can be applied universally, but its effectiveness depends on how power monitoring is implemented. Previous study using the hill-climbing method encountered issues with power monitoring approximation, leading to a limited MPPT range [3].

To overcome the challenges, this paper proposes a new CSCR SC converter-based EHI that performs MPPT through accurate real-time monitoring of output power. Utilizing an innovative power monitor circuit and an exponential Digital Control Oscillator (DCO), it achieves high MPPT efficiency across a wide range. The direct power monitoring method is also unaffected by Process, Voltage, and Temperature (PVT) variations, eliminating the need for post-silicon calibration.

II. Hill-Climbing MPPT for CSCR Converters

Fig. 2 illustrates the MPPT process in EHIs using the hill-climbing algorithm. The power generated by the EH source is transferred to the load through a DC-DC converter. The controller adjusts operating conditions of the converter based on the harvested power estimated by power monitor circuit. The hill-climbing algorithm optimizes harvested power by iteratively comparing the performance of adjacent converter configurations. It enables the EHI to adapt to environmental changes like brightness fluctuations, by consistently selecting the most efficient converter configuration to maximize efficiency.

A. Prior art MPPT with approximated power estimation

In previous research that employed the hill-climbing method for MPPT, power monitoring was conducted using a

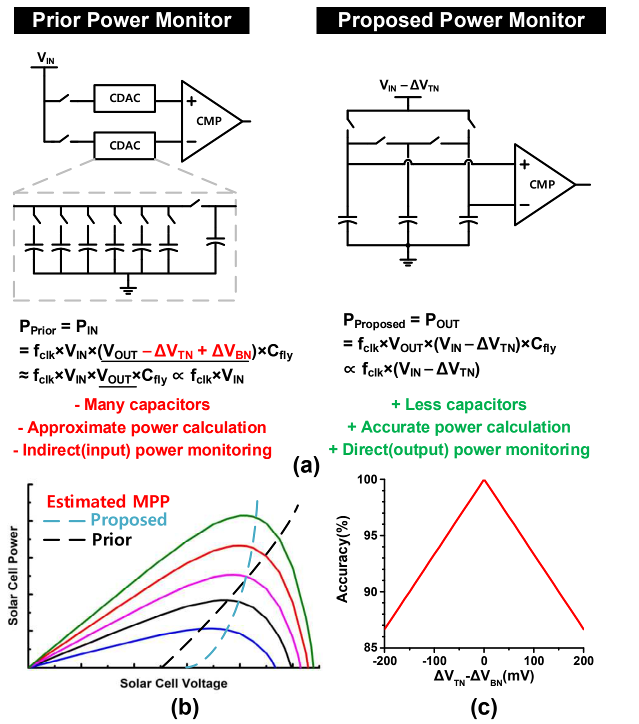

Fig. 3. (a) Prior and proposed power monitor for CSCR EHIs (b) MPPT accuracy vs solar cell voltage from different light intensities (c) Accuracy of power monitor across different ΔV_{TN} - ΔV_{BN}.

capacitive digital-to-analog converter (CDAC) [3]. When the CDAC is utilized for power estimation, the CDAC's resolution significantly impacts MPPT accuracy, necessitating the use of large number of capacitors, increasing circuit area. The steady-state input power of a CSCR SC converter can be expressed as [4]:

$$P_{IN} = f_{clk} \times V_{IN} \times (V_{OUT} - \Delta V_{TN} + \Delta V_{BN}) \times C_{FLY}. \quad (1)$$

where the V_{IN} and V_{OUT} are the input and output voltages of the converter, respectively. P_{IN} indicates that the input power is monitored by the power monitor in this approach. C_{FLY} represents the flying capacitance per stage, and f_{clk} is the switching frequency. ΔV_{TN} and ΔV_{BN} denote the unit step voltage changes per stage at the top and bottom nodes of C_{FLY}, respectively. Assuming $\Delta V_{TN} = \Delta V_{BN}$, P_{IN} can be approximated as [3]:

$$P_{IN} \cong f_{clk} \times V_{IN} \times V_{OUT} \times C_{FLY}. \quad (2)$$

Since V_{OUT} and C_{FLY} remain unchanged during an MPPT cycle, P_{IN} was further simplified as:

$$P_{IN} \propto f_{clk} \times V_{IN}. \quad (3)$$

However, the assumption that $\Delta V_{TN} = \Delta V_{BN}$ does not hold for all V_{IN} values, as ΔV_{TN} and ΔV_{BN} are influenced by V_{IN} and V_{OUT}. This incorrect assumption results in inaccuracy of the input power estimation, reducing the precision of MPPT. Furthermore, this approach measures input power instead of directly monitoring the harvested output power. It overlooks the power loss from the DC-DC converter itself, which may exacerbate power estimation errors, particularly in conditions with low input power.

B. *Proposed MPPT with C_{FLY} unit step voltage (ΔV_{TN})*

To overcome the limitations observed in previous studies, a new MPPT technique is introduced that accurately estimates

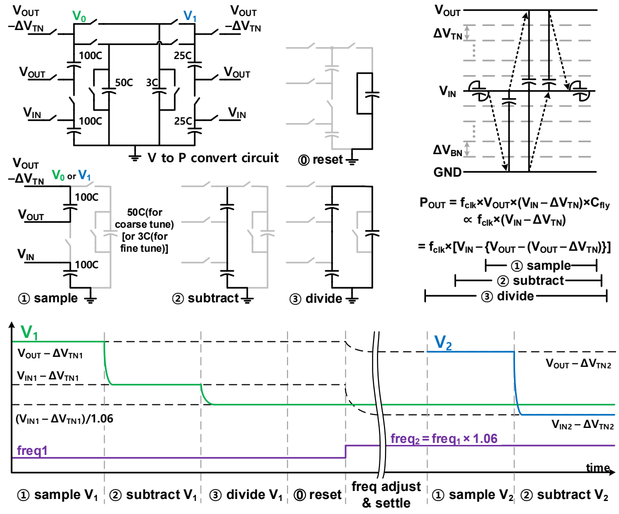

Fig. 4. Proposed power monitor circuit and its operation details

harvested power at the output, factoring in the precise unit step voltage ΔV_{TN} of top flying capacitor. The steady-state output power of a CSCR SC converter can be represented as [3]:

$$P_{OUT} = f_{clk} \times (V_{IN} - \Delta V_{TN}) \times V_{OUT} \times C_{FLY} \quad (4)$$

Given that V_{OUT} and C_{FLY} remain constant during an MPPT cycle, P_{OUT} can be simplified as:

$$P_{OUT} \propto f_{clk} \times (V_{IN} - \Delta V_{TN}) \quad (5)$$

The proposed technique offers precise output power estimation even under fluctuating V_{IN} conditions. Fig. 3(b) conceptually illustrates how the new estimation scheme enhances the accuracy of MPPT compared to previous methods. The earlier estimation technique incorrectly identified the MPP during intense brightness levels - either very dark or very bright - due to power estimation errors. Fig. 3(c) shows the calculated accuracy drop due to the 'ΔV_{TN} - ΔV_{BN}' error, which was previously assumed to be 0. A 200 mV discrepancy results in significant 14% reduction in power monitor accuracy at an output voltage of 1.5 V. In contrast to prior methods, proposed monitoring scheme can accurately track MPP if the unit step voltage ΔV_{TN} of top flying capacitor can be properly accounted during output power estimation.

C. *Circuit implementaion of power monitor*

According to (5), the estimated powers with two different f_{clk} values can be expressed as:

$$P_{OUT,\,t1} \propto f_{clk,\,t1} \times (V_{IN,\,t1} - \Delta V_{TN,\,t1}) \quad (6)$$

$$P_{OUT,\,t2} \propto f_{clk,\,t2} \times (V_{IN,\,t2} - \Delta V_{TN,\,t2}) \quad (7)$$

where the subscripts t1 and t2 represent parameters from the initial and subsequent f_{clk} values. The proposed circuit adjusts f_{clk} using a constant multiplication factor (M), unlike previous method that update it linearly. The constant M allows for direct comparison of harvested powers at different f_{clk} values without involving f_{clk}. For instance, if $M \times f_{clk,\,t1} = f_{clk,\,t2}$, the circuit compares $P_{OUT,t1}$ and $P_{OUT,t2}$ by evaluating '$V_{IN,\,t1}$ - $\Delta V_{TN,\,t1}$' and '$(V_{IN,\,t2} - \Delta V_{TN,\,t2}) / M$'.

Fig. 4 illustrates the proposed power monitor circuit in detail. Since 'V_{IN} - ΔV_{TN}' cannot be directly obtained from the CSCR converter, the circuit indirectly samples 'V_{OUT} - ΔV_{TN}' and estimates P_{OUT} using the modified expression:

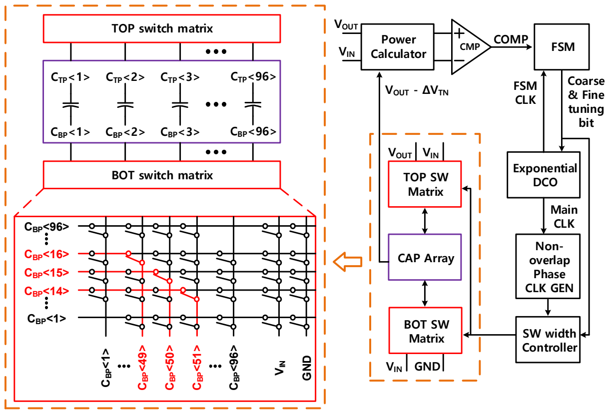

Fig. 5. Overall system diagram of the proposed EH system.

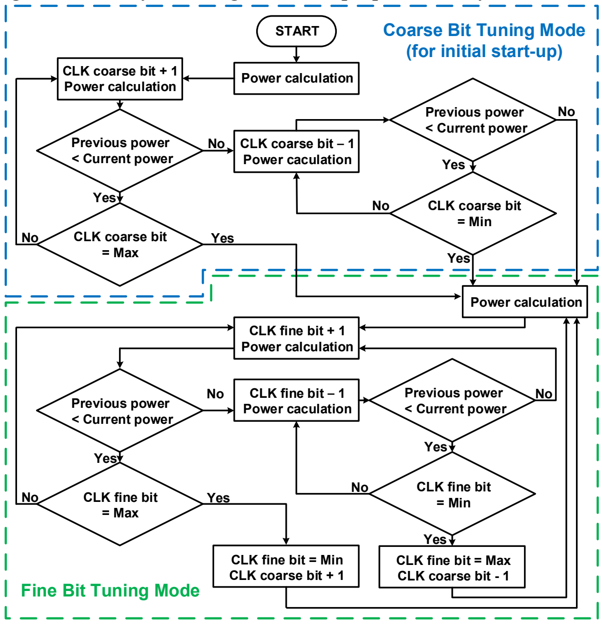

Fig. 6. Algorithm flowchart of FSM to control MPPT.

$$P_{OUT} \propto f_{clk} \times [V_{IN} - \{V_{OUT} - (V_{OUT} - \Delta V_{TN})\}]. \quad (8)$$

The top left of Fig. 4 illustrates the operations of the power monitor circuit. During the first sample phase, two sample capacitors capture the voltage difference across their terminals, sampling $-\Delta V_{TN}$ and V_{IN}, respectively. In the subtract phase, these capacitors are connected in series to form 'V_{IN} - ΔV_{TN}'. For power monitoring at t2, a divide phase follows, where the voltage is divided by a predetermined frequency multiplication ratio (M). The bottom of Fig. 4 illustrates the process over time for an example where f_{clk} increases. The harvested power with the initial f_{clk} (freq1) is estimated and stored as V_1 first, and then the power with a faster f_{clk} (freq2) is calculated and stored as V_2. Comparing these two voltages determines the frequency at which more power can be harvested.

III. System Architecture and Circuit Details

A. System Architecture

Fig. 5 illustrates the overall architecture of the proposed EHI. A comparator compares the two voltages from the power monitor that estimates the harvested power from the current and previous f_{clk}s. A Finite State Machine (FSM) takes the comparator output (COMP) and controls the frequency of the exponential DCO's output (Main CLK). Non-overlap Phase

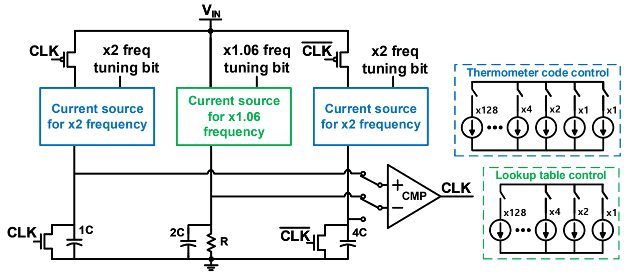

Fig. 7. Proposed DCO to regulate frequency in multiples.

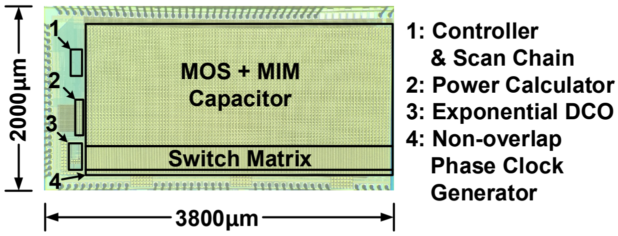

Fig.8. Die micrograph.

CLK GEN and Switch Width Controller convert the Main CLK to 96 phase signals, which drive the CSCR SC converter. The designed converter consists of a 96 parallel capacitor array and a switch matrix connecting all capacitors.

B. FSM for MPPT

Fig. 6 shows the operation of the proposed MPPT, showcasing its FSM functionality that adjusts frequency in multiplicative steps. Larger multiplication factors enable quicker reaching of the Maximum Power Point (MPP) albeit with reduced accuracy. Conversely, smaller factors enhance accuracy but prolong the time to reach MPP. The FSM employs two modes to balance these trade-offs: initially, the Coarse Bit Tuning Mode doubles the frequency for rapid MPP approximation. It then transitions to Fine Bit Tuning Mode, fine-tuning the frequency with a factor of 1.06. If further adjustment is required when the fine bits are set to maximum, it increments the coarse bit and resets the fine bit to its minimum value, and vice versa for decreases. Power comparison is only performed for identical coarse bit configurations.

C. Exponential DCO

Fig. 7 presents the proposed DCO, which plays a pivotal role in the operation of the power monitor. The DCO operates on a relaxation oscillator design, where augmenting the current flowing into the capacitor doubles the frequency. It employs a thermometer code control mechanism to incrementally adjust the current. To finely adjust the frequency by a factor of 1.06, the method regulates the current source responsible for setting the reference voltage. This regulation capitalizes on the inverse correlation between the size of the reference voltage and the frequency. This block is administered by managing codes that correspond to required current sizes via a pre-established lookup table.

IV. Measurement

The prototype chips were fabricated using a 180 nm CMOS process as shown in Fig. 8. A total 96 of 204.8 pF capacitors, comprising both MOS and MIM capacitors, are utilized as flying capacitors.

Fig. 9 illustrates the measured tracking efficiency, which is calculated as the ratio of the output power to the maximum

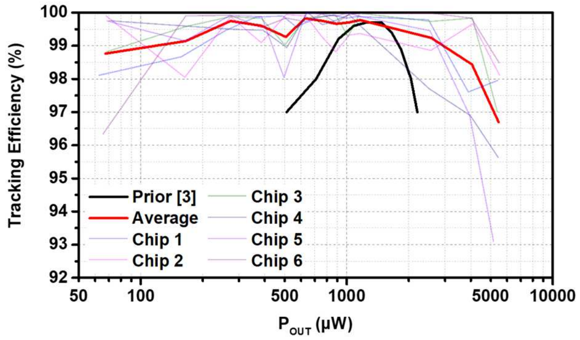

Fig. 9. Measured MPP tracking efficiency.

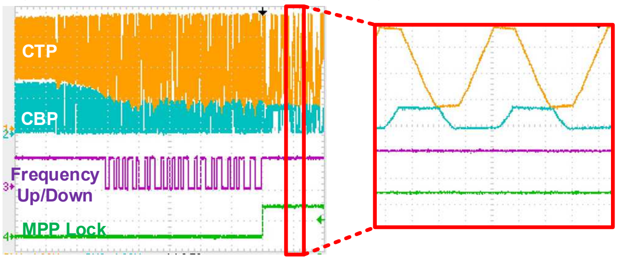

Fig. 10. MPP locking operation waveform of proposed EHI

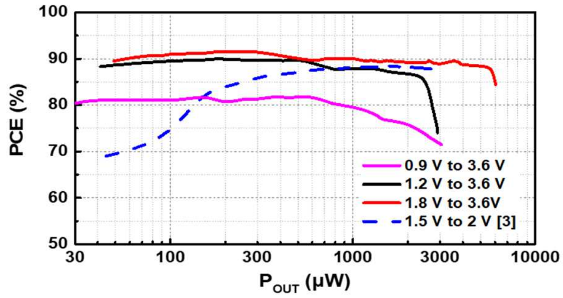

Fig. 11. Measured power conversion efficiency.

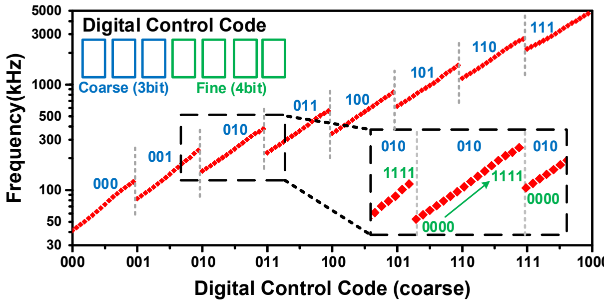

Fig. 12. Measured output frequency of exponential DCO.

potential output power. A mm-scale, commercial solar cell (KXOB25-03X4F-TR) is used as the harvesting source, and an adjustable light source, along with a lux meter, is used to control the environmental condition. Compared to prior-art [3], the range of harvested power with a tracking efficiency above 97% has been increased twentyfold, thanks to the improved power monitoring at output. Fig. 10 shows the operation waveform of the proposed EHI, highlighting a successful MPP locking sequence. Voltages at the top/bottom plate of the C_{FLY} (CTP/CBP) shows the gradual soft charging operation of the CSCR converter. When the frequency up/down signal is high, the frequency increases, and when low, it decreases, allowing the system to track the optimal frequency. As the frequency up/down signal fluctuates around a specific configuration for a preset number of times, the system identifies this as the MPP, and locks the frequency for a predetermined period. This action conserves power by

TABLE I: Comparison with state-of-the-art SC harvesters

	This Work	JSSC 21 [2]	TCAS1 22 [3]	TCAS1 18 [5]	JSSC 16[6]
Tech (nm)	180	180	28(FD-SOI)	180	180
Converter Type	CSCR	CSCR	CSCR	Reconfig SC	Reconfig SC
EH Source	PV	TEG	PV	DC	DC
V_{IN} (V)	0.9 - 1.8	0.1-0.5	0.65 - 1.5	0.5-1.8	0.45-3
V_{OUT} (V)	3.6	0.75	<2	1.2-1.8	3.3
VCR	CSCR	CSCR	CSCR	1~4	1.3-8
MPPT Scheme	Hill-climbing	PFM	Hill-climbing	Hill-climbing	Hill-climbing
Monitoring Power	P_{OUT}	P_{IN}	P_{IN}	P_{OUT}	P_{OUT}
MPPT Implementation	Cap divider & exponential DCO	V_{IN}-connected bias circuit	Frequency-mapped CDAC	V_{OUT}-hysteretic Control & DCO	V sensor
Post-slicon Calibration	Not Required	Required	Not Required	Not Required	Not Required
Continous MPPT	Yes	Yes	Yes	No	No
V_{MPP}/V_{OC} Ratio	Adaptable	Fixed	Adaptable	Adaptable	Adaptable
P_{OUT} Range for Tracking Efficiency > 97% (μW)	63-5500	N/A	510 - 2200	N/A	N/A
Peak Conv. Efficiency (%)	91.5	85.4	88.9	72	81
P_{OUT} (μW)	30 - 6056	1-176	60-2794	1-35	1-50
Freq Range (kHz)	41 - 4709	15-67.1	54 - 3400	35-1370	20-1000
Flying Capacitor (nF)	19.66	7.8	15	N/A	0.5
Area (mm^2)	7.6	3.56	4.8	0.552	4

preventing unnecessary frequency adjustments. Fig. 11 shows the DC-DC converter's Power Conversion Efficiency (PCE). The PCE exhibits efficiencies greater than 85% for wide power ranges, illustrating the high performance and effectiveness of the CSCR SC converter. Fig. 12. demonstrates the exponential DCO's output frequency, showing effective control from 41kHz to 4.709MHz. The proposed DCO is controlled by 3 coarse bits and 4 fine bits. When the coarse bit changes, the frequency doubles; when the fine bit changes, frequency increases by 1.06 times. The power monitor suspends power comparison during discontinuities in the fine bit adjustments, ensuring that accurate frequency adjustments are made only during periods of consistent fine bit intervals.

Table I presents a comparison between the proposed EHI and existing state-of-the-art technologies. The proposed EHI excels in monitoring output power and efficiently tracks the maximum power delivered to the battery without requiring post-silicon calibration. It measures power in real-time, allowing continuous operation of the converter. Employing the hill-climbing method, the EHI adapts flexibly to various energy sources by not fixing the ratio of the maximum power point to open-circuit voltage. It has significantly broadened the power range with a tracking efficiency over 97%, extending twentyfold across a wider spectrum. Additionally, the integrated CSCR SC converter features a peak PCE of 91.5% and a maximum output of 6.05mW.

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